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Simulation and Modeling of Self-switching Devices

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Abstract

A new type of nanometer scale nonlinear device, called self-switching device (SSD) is realized by tailoring the boundary of a narrow semiconductor channel to break its symmetry. An applied voltage V not only changes the potential profile along the channel direction, but also either widens or narrows the effective channel width depending on the sign of V. This results in a strongly nonlinear I-V characteristic, resembling that of a conventional diode. Because the structure resembles a diode-connected FET (gate and drain shorted), we have modeled the device as a sideways turned FET, so that the trench width t corresponds to insulator thickness t_{ox} and conducting layer thickness Z (inside the semiconductor!) corresponds to channel width W.

1. Introduction

A new type of nanometer scale nonlinear device, called self-switching device (SSD) is realized by tailoring the boundary of a narrow semiconductor channel to break its symmetry, Fig. 1 [1]. An applied voltage V not only changes the potential profile along the channel direction, but also either widens or narrows the effective channel width depending on the sign of V. This results in a strongly nonlinear I-V characteristic, resembling that of a conventional diode but without using a doping junction or any barrier structure. The planar and two-terminal structure of the SSD enables a single step lithography for simply SSD-based circuits.

Because SSD is a passive device, building logic gates and other circuits needs an active device to buffer the circuit blocks and to generate amplification. Side-gated transistors can be made with the same etching techniques without additional process steps, and used for this purpose.

The operation of SSD has been demonstrated using two types of III-V semiconductors: InGaAs/InP and InGaAs/InAlAs based SSDs, Fig. 1. To study the feasibility of the concept on SOI (Silicon On Insulator) – silicon substrate we have done 2D simulations with the ATLAS® simulator.

The test SSDs were fabricated using two different material systems: a modulation-doped $In_{0.75}Ga_{0.24}As$/InP quantum-well wafer grown by metal organic vapour phase epitaxy and two modulation-doped InGaAs/InAlAs heterostructures lattice-matched to InP substrates grown by molecular beam epitaxy.

The key fabrication of SSDs was creating insulating grooves by standard electron beam lithography and wet etching. The continuation of the trenches to the device boundary ensured that the current could flow only via the channel. Apart from the apparent difference in device geometry, the SSD is also based on a very different working principle from a conventional diode since no doping junction or barrier structure was used along the current direction. More importantly, only one step of lithography was needed for the device proper, which may significantly reduce the cost of production as well as the increasingly challenging difficulty in the multiple steps of mask alignment of <100 nm feature size, which requires a precision down to $\sim$20 nm.

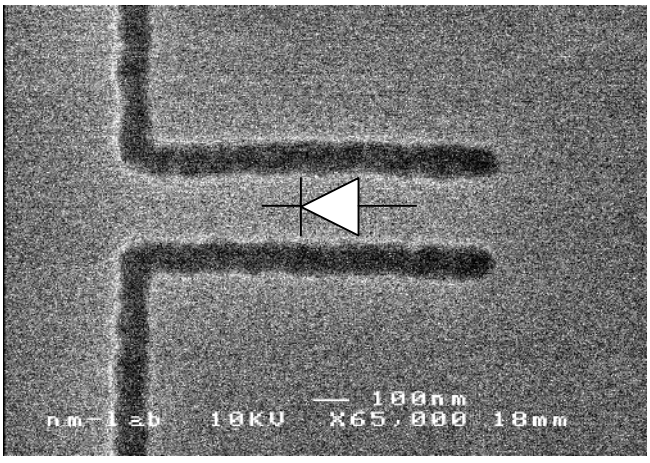

Fig. 1. A scanning electron micrograph of a typical SSD, with the diode direction indicated.

2. SSD and side-gated transistor theory

The SSD can be regarded as a double sided side-gated transistor that is connected as a diode by short circuiting drain and gate together. A side-gated transistor on its side is a horizontal field effect transistor (FET) structure, in which the gates are situated on the sides of the conducting channel, see Figure 2. The gate areas are isolated from the channel and drain and source areas by

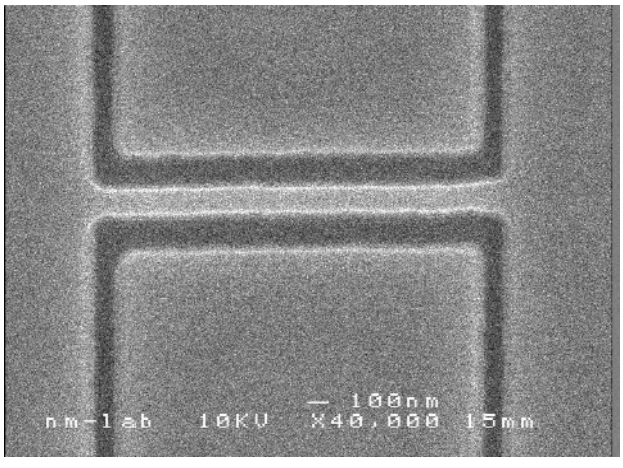

Fig. 2. A scanning electron micrograph of a typical side-gated transistor.

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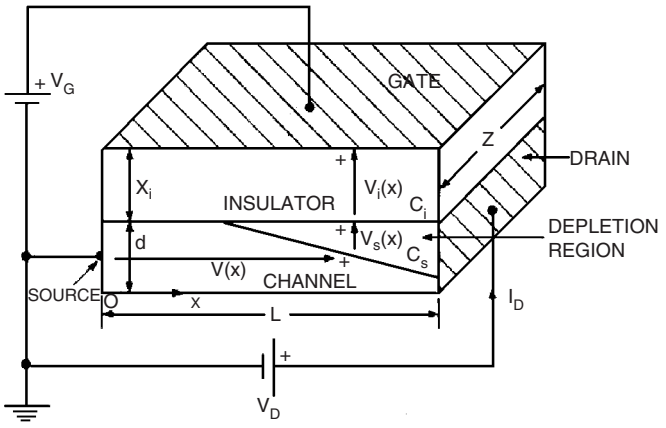

Fig. 3. Simple model of an N-channel depletion mode MOSFET [3].

etched grooves. These grooves can be empty or filled with some dielectric, e.g. SiO_2 in the case of a silicon device. The structure lies on an high resistivity substrate; SiO_2 in a silicon device and semi insulating layer in the case of an III-IV device.

Qualitatively the operation of the side-gated transistor resembles a double sided junction FET (JFET) [2]. In an n-type device, a negative voltage on the gates expands the depletion regions at the channel-groove interface. Eventually with large enough gate voltage the depletion regions reach each other, the channel is pinched off and the current saturates.

We analyse the side-gated transistor, and thereafter the SSD, as a depletion type MOSFET. One can derive for a depletion type MOSFET with uniform doping and with the geometry in Figure 3 the following current equations [3]. Figure 3 represents one half of the structure, with d as half of the channel depth (horizontal channel width in our structure) and L the channel length. Channel width or "depth" d is assumed to be constant in our structures.

The drain current is given by

$$I_D = -\mu_n Z(Q_n + \Delta Q_n)\frac{\mathrm{d}V}{\mathrm{d}x} \tag{1}$$

where μ_n is the mobility, Q_n is the initial charge due to channel doping and ΔQ_n the charge induced by the gate voltage. Notice that in the case of an SSD or a side-gated transistor, Z is the thickness of the semiconductor on the insulating layer. For uniform doping N_D one can derive

$$I_D = \frac{\mu_n Z}{L}\int_0^{VD}[qN_D d + C(V'_G - V)\,\mathrm{d}V] \tag{2}$$

where

$$C = C_i C_s (C_i + C_s),$$
$$C_s \approx 2\varepsilon_s/d \tag{3}$$

and

$$V'_G = V_G + V_{FB}. \tag{4}$$

C_i is the gate insulator and C_s the depletion region capacitance density. V_{FB} denotes the flat band voltage. Two regions of operation can be distinguished: depletion and enhancement mode operation. Integration of (x) with $V'_G < 0$ (depletion mode) gives

$$I_D = \frac{\mu_n ZC}{L}\left[\left(\frac{qN_D d}{C} + V'_G\right)V_D - V_D^2\right] \tag{5}$$

and in saturation

$$I_{DS} = \frac{\mu_n ZC}{2L}\left(\frac{qN_D d}{C} + V'_G\right)^2. \tag{6}$$

In (partial) enhancement mode, $V_D > V'_G$, we get for the current

$$I_D = \frac{\mu_n ZC}{L}\left[\left(\frac{qN_D d}{C} + V'_G\right)V_D - \frac{V_D^2}{2} + \frac{C_i}{2C_s}V_G'^2\right] \tag{7}$$

and in this case in saturation

$$I_{DS} = \frac{\mu_n ZC}{2L}\left[\left(\frac{qN_D d}{C} + V'_G\right)^2 + \frac{C_i}{C_s}V_G'^2\right]. \tag{8}$$

The above analysis is based on the following assumptions, that are not necessarily fullfilled in actual SSDs in question.

A. The equations are based on long channel approximation. No short channel effects are taken into account.
B. No possible fixed charge at the groove-channel interface has been taken into account.
C. The gate voltage is assumed to be low enough not to cause surface inversion.

2.1. *SSD circuit modeling*

A simple model for the SSD was determined having the MOSFET square law as the basis. Using the square law is justified by making $V_D = V'_G$ in a diode connected depletion mode MOSFET and thereafter using the saturation current equations (6) and (8). For the model we used the following equations.

$$I = \begin{cases} -\mu\dfrac{\varepsilon_0}{t}\dfrac{Z}{2L}(V - V_{tn})^2, \text{when } V < V_{tn}, \\ 0, \text{when } V_{tn} < V < V_{tp}, \\ \mu\dfrac{\varepsilon_0}{t}\dfrac{Z}{2L}(V - V_{tp})^2, \text{when } V > V_{tp}; \end{cases} \tag{9}$$

with t as the insulating trench width. The approach is to have as many of the model parameters physically and geometry based as possible. Only two fitting parameters were necessary: threshold voltage for positive and negative directions: V_{tp}, V_{tn}. The mobility μ can be taken from the sheet mobility measurements of the wafers [1], but we treated it as a third free fitting parameter and compared the results with the measured value. Geometry parameters of the simple model were the channel length, etch width and vertical channel width: L, t and Z, respectively. The horizontal width was not considered explicitly, but it is included implicitly in V_t. Let us write Eq. (8), with $K = \mu_n ZC/2L$, in the form:

$$I_{DS} = K\left[V_G^2\left(1 + \frac{C_i}{C_s}\right) + 2\frac{qN_D d}{C}V_G + \left(\frac{qN_D d}{C}\right)^2\right]. \tag{10}$$

With the assumption $C_i/C_s \ll 1$ (reasonable with the used dimensions $t = 40\ldots100$ nm vacuum or air and $d = 60\ldots200$ nm Si, InP/InGaAs or $In_{0.75}Ga_{0.24}As$/InP) Eq. (10) simplifies into

$$I_{DS} = K\left(V_G + \frac{qN_D d}{C}\right)^2 \cong K(V_G - V_t)^2 \tag{11}$$

with $V_t = -qN_D d/C$. Thus the threshold voltage of the SSD in (11) resembles more the pinch-off voltage of a JFET than the threshold voltage of a MOSFET. Equation (11) does not include the effect of trapped charge on the trench-semiconductor surface, that according to the 2D-simulations may have a profound effect on V_t. Inclusion of the trapped charge in (11) would make

the calculations complicated and measuring the interface charge density on the intrinsic device is very difficult. Therefore we have used V_t in whole as a fitting parameter.

3. Results and discussion

Modeling of SSD devices was based on experimental data on InP/InGaAs and $In_{0.75}Ga_{0.24}As$/InP SSDs. In practical modeling μ was also a fitting parameter and the best fit was compared to the value achieved with the sheet resistance measurement. The simulation results looked very promising compared with the measured data of InGaAs/InAlAs SSDs; the fit was rather good in all working measured diodes, and gave the same mobility of $10 * 10^3$ cm^2/Vs as the sheet measurements. An example is shown in Figure 4. InP/InGaAs simulations on the other hand gave a mobility of 5500 cm^2/Vs with the best fit, Figure 5. This is about half of the measured sheet mobility value $12 * 10^3$ cm^2/Vs. The most propable explanation is that the real trench width was wider than the nominal value in this case. To confirm this we have to make additional measurements on the geometry of the trench.

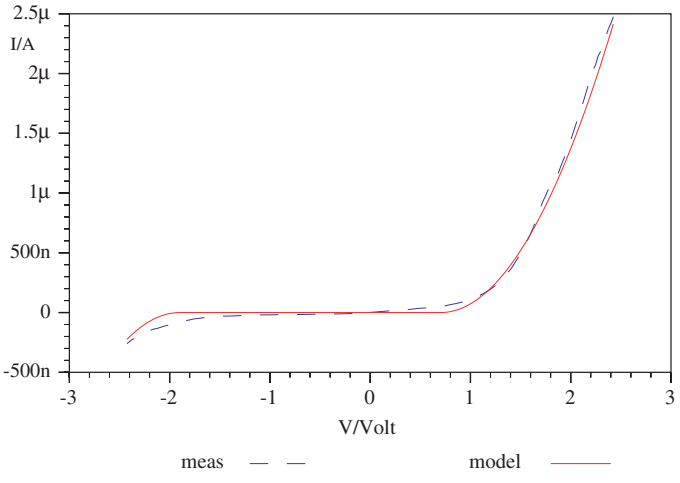

Fig. 4. Measured and Simulated I-V curve of an InGaAs/InAlAs SSD. $Z = 80$ nm, $L = 1.2$ µm, $t = 100$ nm and $N_D = 1 * 10^{12}$ cm^{-3}. Simulated $V_m = 1.6$ V and $\mu = 1.0 * 10^4$ cm^2/Vs.

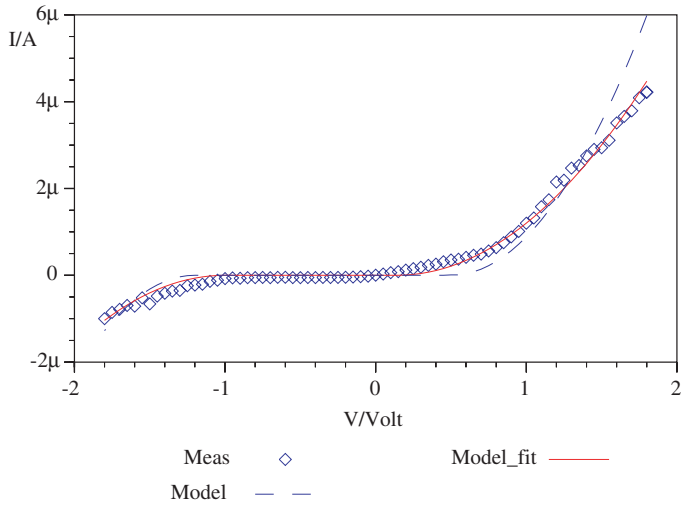

Fig. 5. Measured and simulated I-V curve of an InGaAs/InP SSD. $Z = 80$ nm, $L = 1.2$ µm, $t = 100$ nm and $N_D = 1 * 10^{12}$ cm^{-3}. Simulated $V_m = 1.6$ V and $\mu = 5.5 * 10^3$ cm^2/Vs.

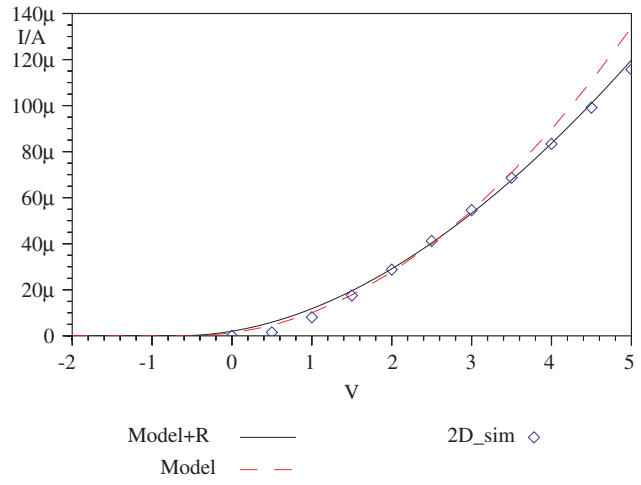

Fig. 6. 2D simulated I-V curves and curves fitted with Eq. (9), without series resistance (– – –) and with 30 kΩ series resistance (——).

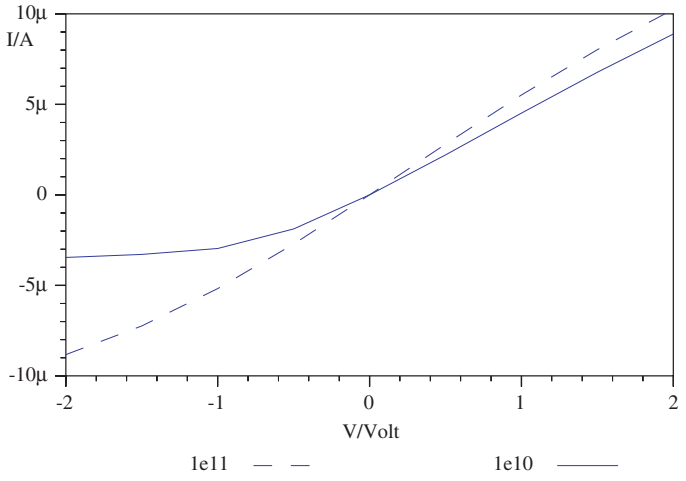

Fig. 7. The effect of surface states on SOI-SSD performance. State density of 10^{10} cm^{-2} (——) and density of 10^{11} cm^{-2} (– – –).

To verify the feasibility of the concept on SOI-silicon substrate we simulated SSD structures on the ATLAS® 2D-simulator. The channel length L was varied between 200 nm . . . 1 µm, trench width 40 nm . . . 100 nm and channel width 60 nm . . . 200 nm. The doping density was from 10^{15} cm^{-3} to 10^{17} cm^{-3}. We also inserted a trapped charge at the trench – semiconductor interface from zero to $5 * 10^{11}$ cm^{-2}.

We fitted Equation (9) with the simulated I-V curves, Figure 6. The 2D-model had some series resistance, 5 to 50 kΩ depending on the doping density, both at anode and cathode. Adding series resistance to the model improved the fit a little, Fig. 6. Basically the simulations demonstrate that the SSD concept is feasible also on SOI-silicon. The structure turned out to be quite sensitive to the concentration of the interface trapped charge. With N_D 10^{15} cm^{-3} a density of 10^{10} cm^{-2} had practically no effect on the performance of the device, but a density of 10^{11} cm^{-2} made the device already almost resistive, Figure 7. The simulated current as a function of trench width t was well in accordance with Eq. (9) over the range simulated: 50 . . . 150 nm. The current dependance on channel length L over the simulated range 0.5 . . . 1.5 µm, however, was less than $1/L$ predicted by Eq. (9). The reason for this is not yet analysed.

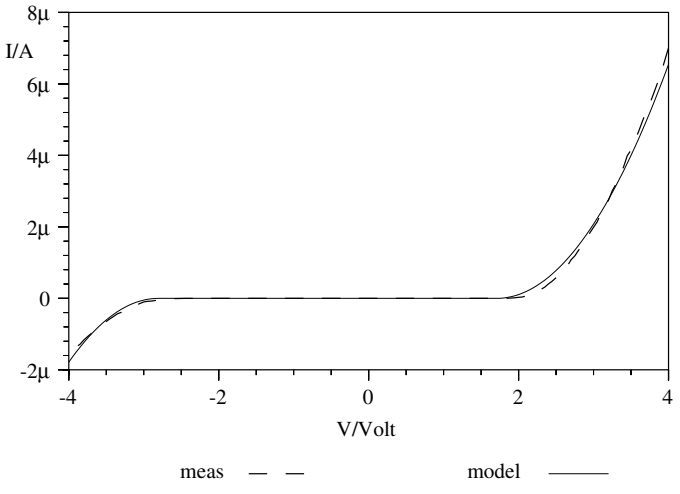

Fig. 8. Measured and simulated *I-V* curve of a p-type SOI SSD. $Z = 140\,\text{nm}$, $L = 370\,\text{nm}$, $d = 56\,\text{nm}$, $t = 46\,\text{nm}$ and $N_A = 5 * 10^{16}\,\text{cm}^{-2}$. Simulated $V_{tp} = 1.71\,\text{V}$, $V_{tn} = 2.80\,\text{V}$ and $\mu = 340\,\text{cm}^2/\text{Vs}$.

We have also some preliminary measurement data with one size of SOI SSD on p-type substrate with $N_A = 5 * 10^{16}\,\text{cm}^{-3}$, $L = 370\,\text{nm}$, $d = 56\,\text{nm}$ and $t = 46\,\text{nm}$, Figure 8. The fit is also with this Si-based example very good, with extracted $V_{tp} = 1.71\,\text{V}$, $V_{tn} = 2.80\,\text{V}$ and $\mu_p = 340\,\text{cm}^2/\text{Vs}$. The extracted mobility corresponds very well with the typical value of $350\,\text{cm}^2/\text{Vs}$ for $N_A = 5 * 10^{16}\,\text{cm}^{-3}$ in silicon [4]. However, we do not yet have enough data to demonstrate the scalability of the model for different device sizes on SOI, as in the case of InP/InGaAs and $In_{0.75}Ga_{0.24}As$/InP.

4. Conclusions

We have made a simple circuit simulation model for III-V semiconductor SSDs, based on depletion mode MOSFET equations. The model gives a reasonably good fit with the measured results, provided that the geometrical device parameters are right. The fit is acceptable with sub-µm devices even when it is based on long channel equations. Taking short channel effects into account could propably improve the model at sub and near-threshold voltages, and taking series resistance into account improves the model with high currents. We have also demonstrated the feasibility of the SSD concept and model on SOI-silicon substrate by simulations and with preliminary measurements.

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