Simulation Based Mask Defect Repair Verification and Disposition

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ABSTRACT

As the industry moves towards sub-65nm technology nodes, the mask inspection, with increased sensitivity and shrinking critical defect size, catches more and more nuisance and false defects. Increased defect counts pose great challenges in the post inspection defect classification and disposition: which defect is real defect, and among the real defects, which defect should be repaired and how to verify the post-repair defects.

In this paper, we address the challenges in mask defect verification and disposition, in particular, in post repair defect verification by an efficient methodology, using SEM mask defect images, and optical inspection mask defects images (only for verification of phase and transmission related defects).

We will demonstrate the flow using programmed mask defects in sub-65nm technology node design. In total 20 types of defects were designed including defects found in typical real circuit environments with 30 different sizes designed for each type. The SEM image was taken for each programmed defect after the test mask was made. Selected defects were repaired and SEM images from the test mask were taken again. Wafers were printed with the test mask before and after repair as defect printability references.

A software tool SMDD—Simulation based Mask Defect Disposition—has been used in this study. The software is used to extract edges from the mask SEM images and convert them into polygons to save in GDSII format. Then, the converted polygons from the SEM images were filled with the correct tone to form mask patterns and were merged back into the original GDSII design file. This merge is for the purpose of contour simulation—since normally the SEM images cover only small area (~1 µm) and accurate simulation requires including larger area of optical proximity effect. With lithography process model, the resist contour of area of interest (AOI-the area surrounding a mask defect) can be simulated. If such complicated model is not available, a simple optical model can be used to get simulated aerial image intensity in the AOI. With built-in contour analysis functions, the SMDD software can easily compare the contour (or intensity) differences between defect pattern and normal pattern. With user provided judging criteria, this software can be easily disposition the defect based on contour comparison. In addition, process sensitivity properties, like MEEF and NILS, can be readily obtained in the AOI with a lithography model, which will make mask defect disposition criteria more intelligent.

Key words: Mask defects, SEM image, simulation, defect repair, verification, disposition

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INTRODUCTION

Lithography process has been the driver of the technology advances in IC manufacturing for several decades and will continue to be so. Masks have been one of the most critical components in image transfer from design to silicon through lithography process since 130nm technology node and below. The cost of mask making has been increasing drastically and the trend is continuing and accelerating. For foundries, it is particularly important to control the costs associated with mask making processes. In this paper, we present a specifically developed, cost-effective software solution—SMDD (Simulation based Mask Defect Disposition) in mask defect handling; including defect printability check and defect post repair verification and disposition to reduce the need for costly hardware solutions.

Although alternative solutions have been actively explored, [1, 2] currently, hardware based, AIMS (Aerial Image Measurement System) like equipment is still the tool of choice for mask defect printability check. However, when moving into sub-65nm technology nodes, a new system is needed to match advanced scanners and the existing systems do not have the resolution to resolve some of the features in sub-65nm masks. Thus, the software-based solution has been developed and tested. Not only this software solution is cost effective (in combination with existing equipments), but also extendable to advanced technology nodes.

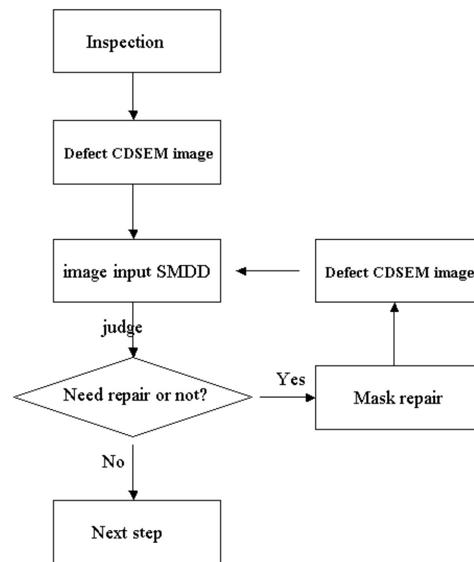


Figure 1: Basic flow used in mask shop

APPLICATION FLOW

SMDD is used in mask making process to judge whether a mask defect needs repair and verify mask defect after repair, as shown in the basic flow chart of Figure 1. SMDD uses mask defect SEM images and the corresponding GDSII design as input data. The software first loads in both design and a mask defect SEM image and places the SEM image in the correct location. Next the software extracts edge contours from the SEM image. The extracted edge contours are then converted to GDSII format polygons—the realistic mask patterns, as in layout designs, with polygon fill and tone adjustment. Due to the size limitation of the SEM images used (normally less than 1μm at wafer scale), converted mask patterns are not suitable for wafer contour simulation. The next step is to merge this converted mask pattern with the corresponding design, so that when simulating wafer image contour, a large enough area of the mask around the defect (larger than optical proximity effect distance) can be included. The optical impact on the defect location decreases from surrounding features farther away. So, replacing the real mask patterns outside of SEM image area with the design patterns (ideal mask patterns) has a minimal effect on the wafer contour in the area of interest (AOI) and the simulation results have confirmed such assumption.

After merging the converted mask patterns with the design layout, it is ready for wafer contour simulation. First, a lithography model is loaded into the software. The same lithography model is used as in OPC or OPC verification steps, created well before mask making step. If such complicated lithography process

model is not available, a simple optical model can be also used. The software can simulate aerial image intensity profiles using the simple optical model with merged mask patterns. With a constant intensity threshold, lithography impact can be analyzed. With availability of lithography process model, much more accurate wafer resist contours can be obtained—which is another advantage that this software solution offers.

Two wafer resist contours can be simulated and compared in the software. One is the resist contour of AOI with the converted mask patterns with the defect; and the other is a converted normal mask pattern without defect as a reference, similar to die-to-die referencing strategy. If it is desirable, the simulated resist contour of an ideal mask (design) can also be used as a reference, in analogy to die-to-database referencing strategy. A simple contour difference check can be performed within AOI and compared with user specified contour tolerances. A disposition judgment is then performed based on simulation contour comparison result and user specified tolerance specification, which then completes the mask defect printability verification and disposition. The above-mentioned flow is shown in Figure 2 in the flow chart. The flow can be used to determine whether a mask defect needs repair, as well as to verify post-repair effectiveness.

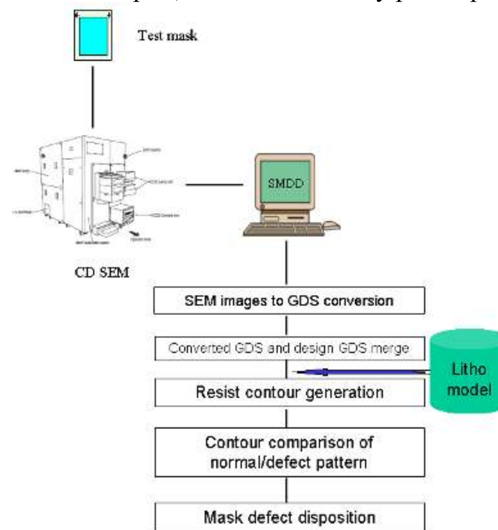


Figure 2: Application flow of mask defect disposition.

In the following sections, we will present test results using a test mask and a real case in production line following the application flow listed above.

SOFTWARE SOLUTION

The software SMDD is GUI based tool, utilizing pattern centric NanoScope platform. The SMDD GUI consists of 4 parts: Layout page, Image input page, layout and image viewer and Analysis and Disposition page. Figure 3 shows SMDD Layout and Image viewing GUI. The wafer contour simulation capability is transferred directly from another product of NanoScope platform, and is done in Layout and Image viewing GUI. [3] For SMDD, only a small area, localized contour simulation is needed. There are other build-in functions can be accessed from Layout and Image viewing GUI, such as MEEF/NILS analysis, Boolean operations and layer loading/saving functions. The software successfully overcomes the key technical challenges in the following areas: 1) accurately extract edges from SEM image; 2) convert these edges (including virtual edges at the boundary of SEM images) into GDSII polygons and 3) merge the converted polygons with design layout GDSII for wafer contour simulation. Due to possible SEM image quality variations, an optional step of SEM image edge enhancement can be inserted before SEM image edge extraction.

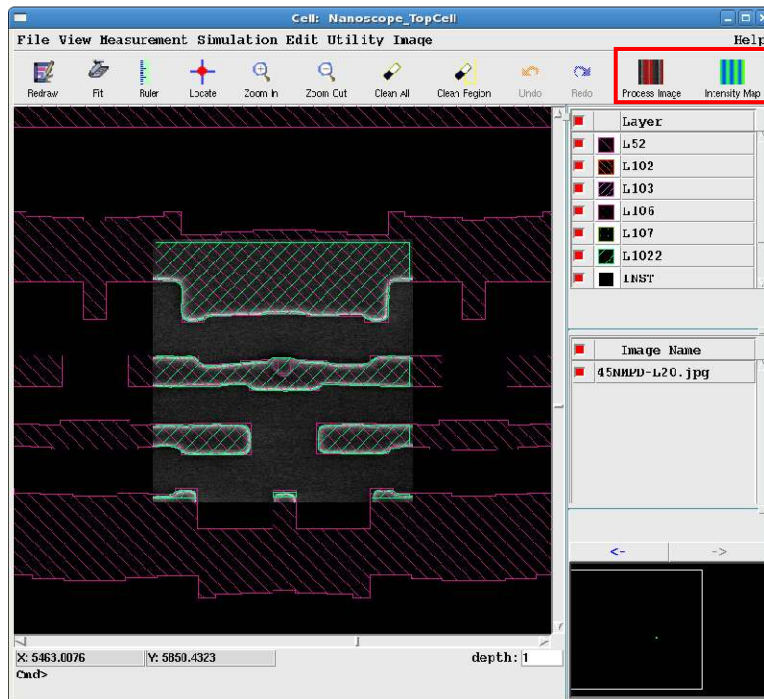


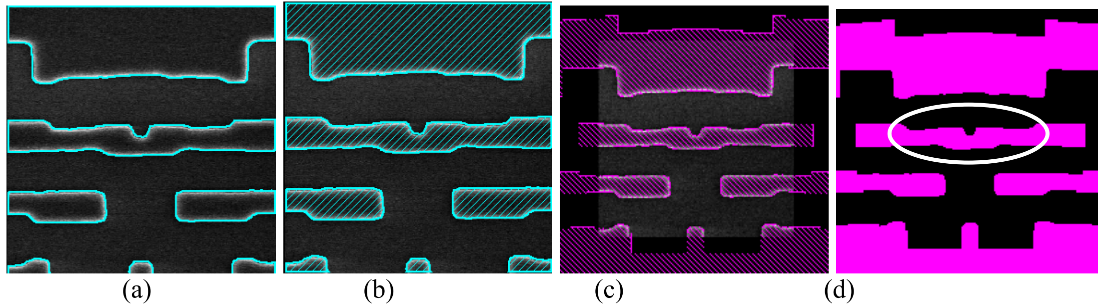
Figure 3: SMDD GUI: layout and image view and image process icons (inside the red box).

TEST MASK

A test mask was designed and fabricated with programmed defects for the software testing and evaluation. The test mask is attenuated phase shift mask and uses sub-65nm design rules with 20 defect types, including defect types in “real design” environment with advanced OPC decoration. The three kinds of main patterns are isolated CD bar, dense CD bars and SRAM features. Each type of programmed defects has 30 defect sizes, varying from 5nm to 150nm, with 5nm incremental step to cover the range from non-printing to printing on wafer. After the test mask was made, a SEM image with FOV (Field of View) 2µm x 2µm was taken for each programmed defect with total 600 SEM images. A wafer is then printed using sub-65nm process for simulation references. Selected defects then go through sub-65nm standard mask repair processes. Again, mask SEM image was taken for each repaired defect. Another wafer is printed using the post-repaired mask and SEM images are taken at post repair defect locations for printability verification.

SEM IMAGE EDGE EXTRACTION

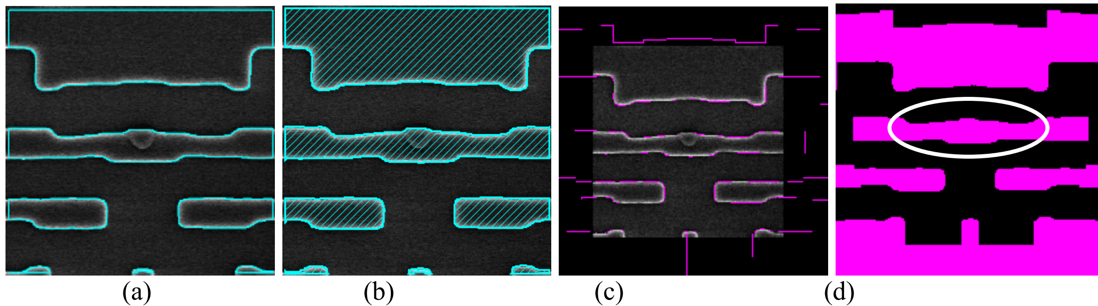
Even though, for test purpose, we have processed all SEM images, we will show only two typical defects in this paper with relatively large defect sizes to show their impact on wafer printing results. In Figure 4, we show the SMDD output results at each step from SEM edge extraction; polygon fill and GDSII merge to the final GDSII and represent the AOI in the real mask for the programmed defect L20. The edge extraction algorithm extracts both inner and outer edges from the white edge band due to enhanced edge emission of secondary electrons in SEM images. Depending on the tone selection, either inner edge or outer edge is used. A constant bias can be applied if user chooses to do so; but in most cases, no bias was needed. After polygon fill as shown in Figure 4 (b), the mask patterns are successfully converted from SEM image to GDSII format patterns, which realistically represent the real mask feature shapes including a mask defect. To prepare for wafer contour simulation, converted mask patterns need to be merged with the corresponding design at the defect location. After merging step, the AOI is represented by the converted mask patterns from SEM and outside of AOI is represented by the ideal mask patterns (the design), as shown in Figure 4 (d). When simulating the wafer contours for AOI, all environment impact is included to maintain the simulation accuracy.



(a) (b) (c) (d)

Figure 4: the programmed defect L20 (a) mask defect SEM image (b) extracted edges with polygon fill (c) converted to GDSII format pattern (d) merged with the design layout.

Figure 5 shows the SEM image to GDSII pattern result for the same-programmed defect L20 after repair.



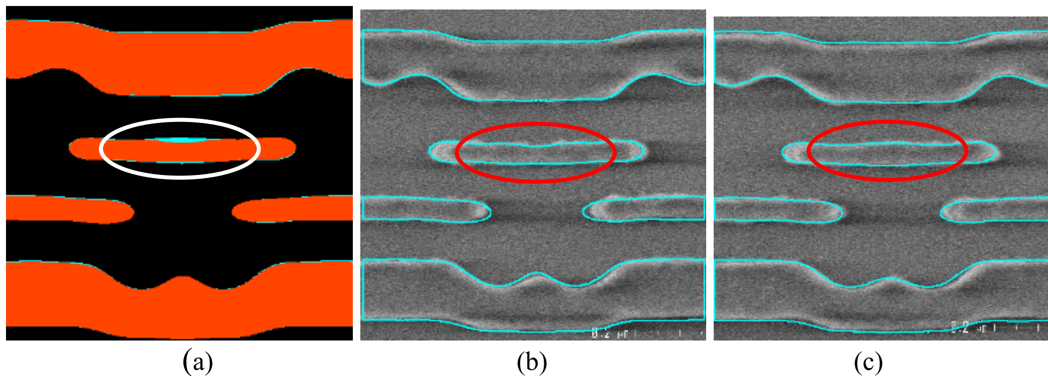
(a) (b) (c) (d)

Figure 5: the programmed defect L20 after repair (a) to (d): from SEM image to GDSII polygons.

WAFER CONTOUR SIMULATION

Lithography process models already exist well before masks are made at OPC or OPC verification step. If such model is available, then wafer resist simulation result of an AOI in a mask can be generated using a converted GDSII mask pattern as shown in Figure 4&5 (d). Figure 6 shows the simulation results from programmed defect L20 before and after mask repair to highlight the impact of defect on wafer printing. The CD difference in the defect location is about 12nm, validating the need for such repair. In this case, the contour from the post repair mask can be viewed as a die-to-die reference. The simulated wafer resist contours from L20 matches well wafer printing well, especially in the AOI.

Figure 7 shows another example from programmed defect R23 before repair. Defect R23 has two scattering bars on its topside. The defect in AOI is well represented by the converted mask contour, as shown in Figure 7 (b) and the simulation result matches the wafer printing result well [Figure 7 (c)]. Figure 8 shows post-repair R23 results and again the simulation result matches well with wafer printing. The wafer resist CD at the defect location changed from 44nm before mask repair to 55nm after mask repair.



(a) (b) (c)

Figure 6: simulation result comparison of pre and post repair of defect L20 (a). The CD difference is about 12nm. Simulation results match well with the wafer printing for defect L20 before (b) and after (c) repair.

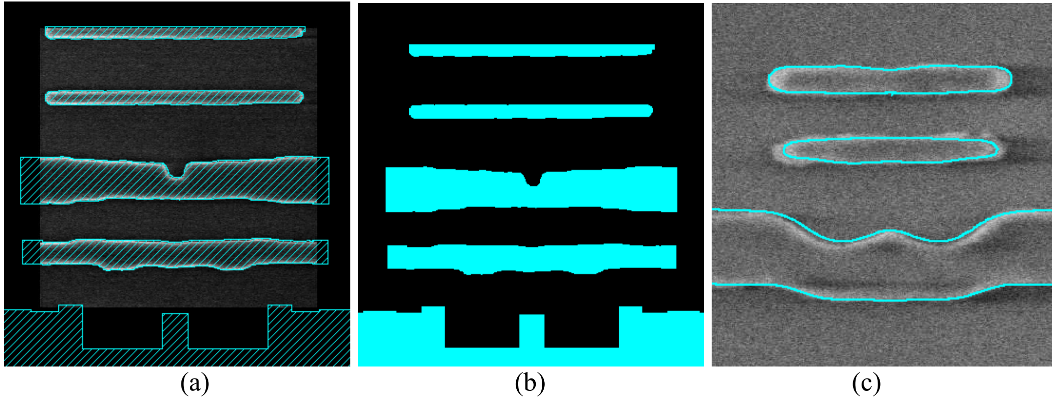

(a) (b) (c)

Figure 7: Programmed defect R23 results before repair.

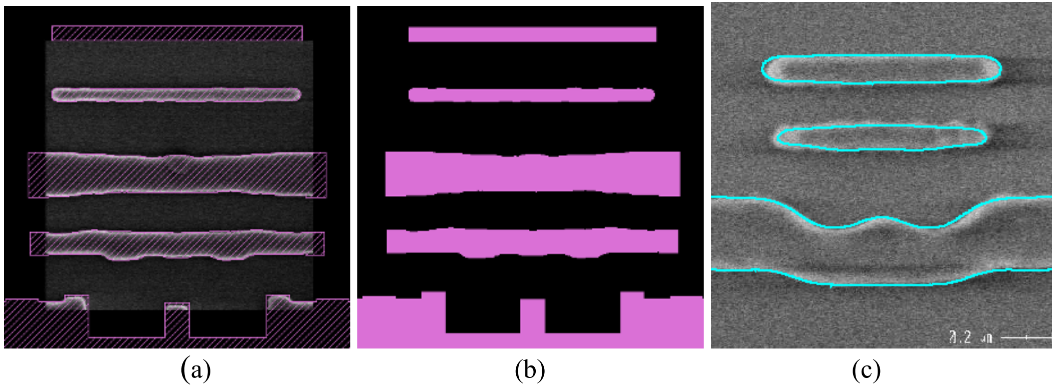

(a) (b) (c)

Figure 8: Programmed defect R23 results after repair.

CD measurements from the printed wafer can be compared to SMDD simulate results directly. Figure 9 shows such comparison from 4 selected defect groups (type B, G, K and L, consist of all three types of patterns). The software simulation shows a good agreement with the wafer CD data with wide range of defect sizes.

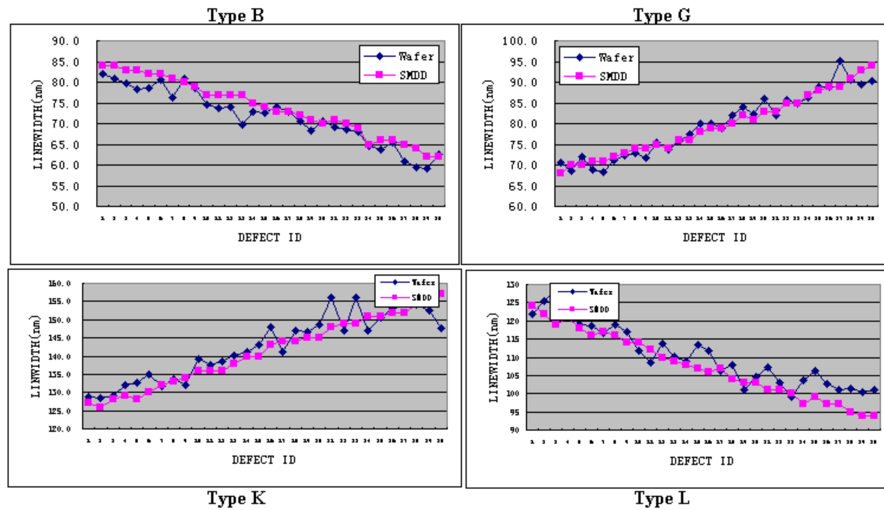


Figure 9: CD data comparison. These data show good agreement between the SMDD simulation's prediction and actual wafer CD measurement.

In our case study, average 3.6% simulation error exists for all the defects including protrusion, intrusion, pin-hole and pin dot and well within our CD tolerance specification of 6% for performing the simulation-based defect analysis considering the wafer process variation and simulation tool's accuracy. Good agreement between the SMDD simulation predictions and the actual wafer CD measurement provides the solid foundation for defect disposition.

The simulation area is localized around the AOI and simulation speed is not an issue. The overall processing time of one defect from loading image in the software tool to the final disposition takes only a few minutes. Currently, the software is semi-automated and full automation is possible, if needed.

In deciding if a repair is needed for a given defect, the same normal pattern around the AOI can be used as a reference to gauge wafer plane CD impact of the defect as shown in Figure 6. Because an ideal mask (design) always exists in SMDD, it is possible to do die-to-database referencing in certain cases. Figure 10 shows an example of such application scenario. In Figure 10 (a), a "real" mask and an "ideal" mask are overlaid together to show the differences. Other than the defect itself, the other differences are minor mask feature smoothing from the mask writer in two scattering bars above the defect and the small line below it. In Figure 10 (b), the simulated wafer contours are overlaid together from the two masks in Figure 10 (a). One can clearly see the impact of the defect on the CD change (~10nm) at defect location. In addition, due to high MEEF of the top edge of the smaller line, the CD change (~4nm) is also visible at its top edge.

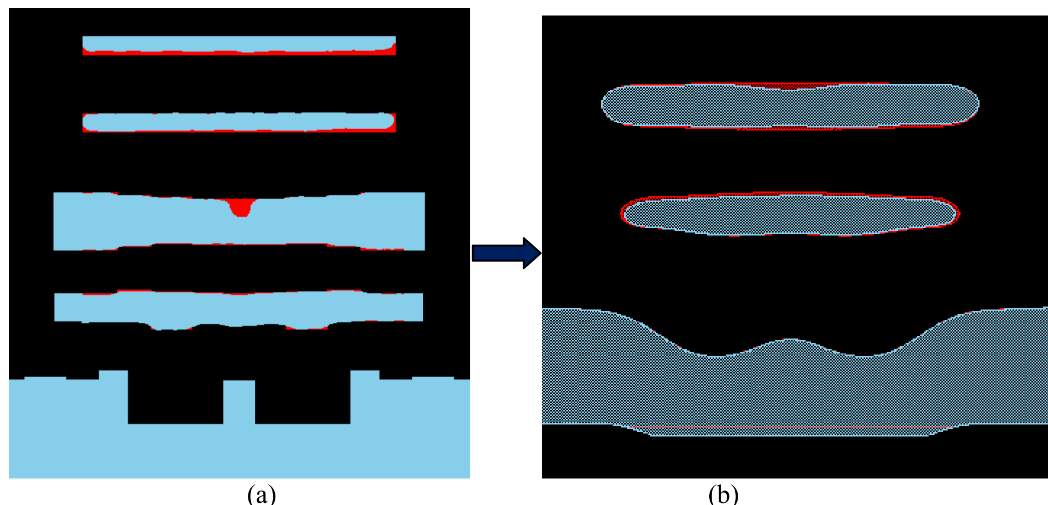


Figure 10: a "real" mask (blue) and an "ideal" mask (red) around AOI (a) and their corresponding wafer resist contours (b). The CD impact at the defect location is clear visible and measurable (~10nm).

ANALYSIS AND DISPOSITION

After simulation, it comes to the final analysis and disposition step. With OPC model, the analysis is straightforward—directly checking feature CD change at the defect location between defective mask pattern and a normal mask pattern. While with simple optical model, the analysis requires additional steps. The analysis starts with aerial image intensity. Figure 11 shows the analysis and disposition GUI. There are 6 sections in the analysis GUI from left to right and top to bottom matrix: Area Intensity Map; Location-Intensity Chart (user selected analysis line); Area Contour Map; Threshold-Width Chart; Focus-NILS Chart (requires defocus model); and Area SEM image (for reference). Area intensity map contains two intensity maps—one from the SEM image converted mask and one from ideal mask. Additional intensity file can be loaded in and displayed in this GUI. After user selects an analysis line (the white line in Figure 11), two intensity curves are shown in the Location-Intensity Chart: one from the SEM images converted mask and another from ideal mask. A constant threshold can be placed in Location-Intensity Chart and corresponding CD vs. Threshold curves are displayed in Threshold-Width Chart window and the CD values at the selected threshold will be highlighted and shown on top of the chart. By clicking on the Delta motif icon on top, the CD delta will be displayed. In Area Contour Map, users have the flexibility to change mask tone through

Mask Type and display wafer resist contour at any given threshold. By connecting any two edges using mouse drag, CD values between the two edges will be shown. Without defocus models, only one point from each masks will displayed in Focus-NILS Chart. With defocus models, a focus-NILS chart will be displayed. The intensity profile can be saved and loaded back later for further analysis. Disposition decision is made on the top of the screen by selecting PASS, FAIL, or PENDING.

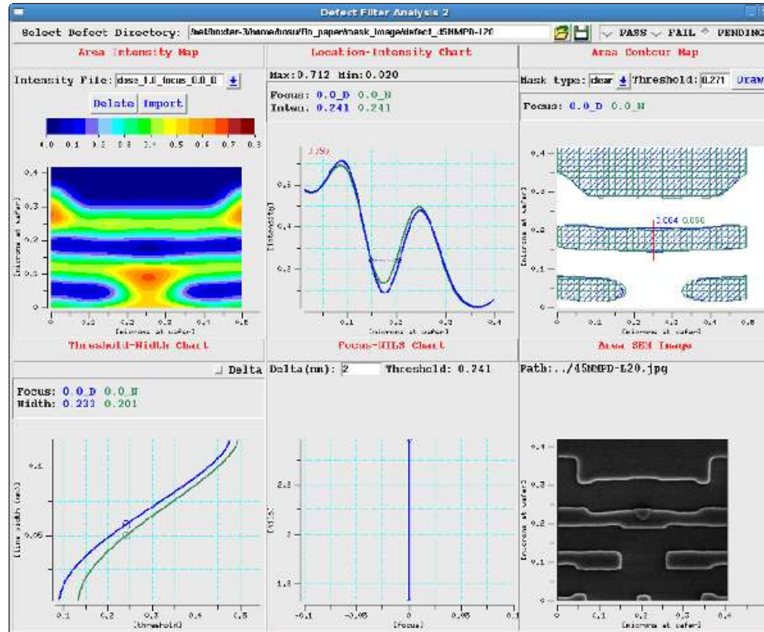


Figure 11: SMDD analysis and disposition screen.

FABRICATION APPLICATION

After fully testing and verifying by test mask, SMDD has been also actively used in fabrication flow. Figure 12 shows such an application case using SMDD to decide whether a small defect found inside a narrow slot needs to be repaired. The simulation result from an optical model indicates that defect repair is needed, since the defect has nearly 20% CD impact near the defect location as shown in Figure 13.

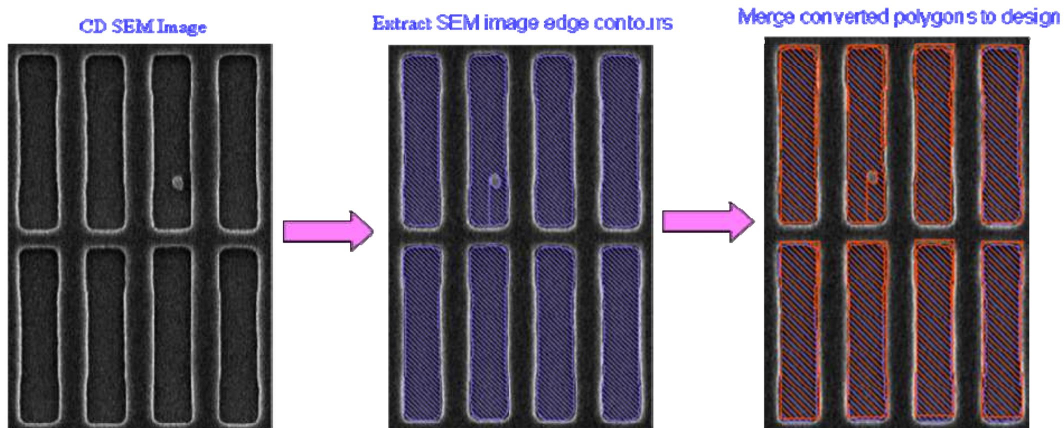


Figure 12: a fabrication application case: a defect inside a dense rectangle box.

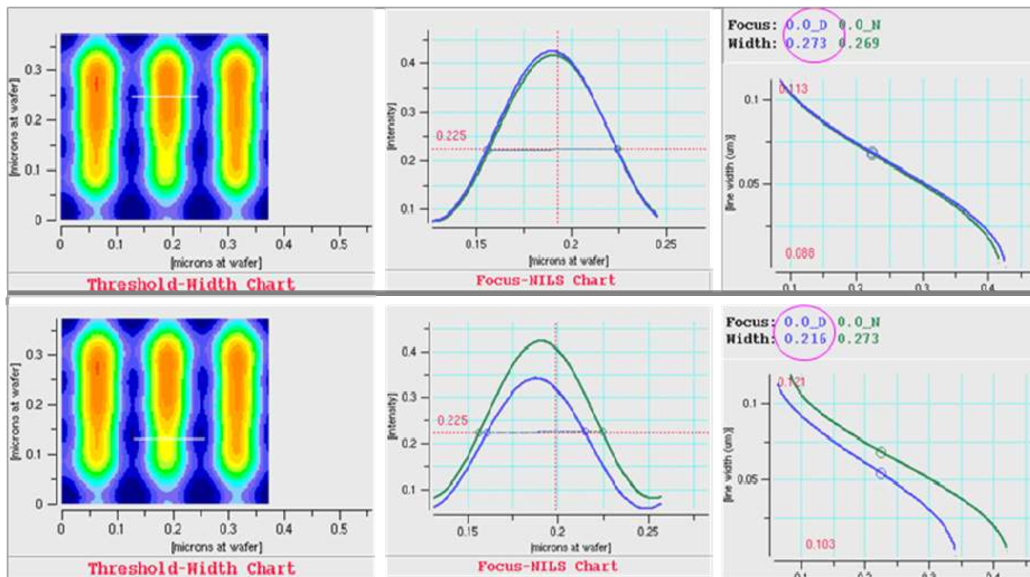


Figure 13: CD analysis using an optical model at normal CD location and defect CD location. The defect causes CD change nearly 20% (at mask scale) and requires to be repaired.

OTHER POSSIBLE APPLICATIONS

The capability of converting SEM image to GDSII patterns is applicable to other areas in mask shop and wafer Fabs; parallel efforts are under way to explore those applications. For example, with SEM image to GDSII pattern conversion, SEM image based mask process monitoring is possible with faster turnaround time than current CD based mask process monitoring by comparing SEM image contours of pre-defined process monitoring patterns. Another possibility is to use trouble-shooting SEM images (which can be mask process related hotspots, or yield related wafer hotspots) and convert them to GDSII format pattern templates. With existing pixel based similar pattern search capability in NanoScope platform, it is quite easy and useful to find out where and how many such hotspot patterns exist in a full chip design.

In addition, as demonstrated in this paper (see Figure 10), it is possible to partition CD error contribution of a given design pattern from a real mask (with corner rounding and mask writer intrinsic biases) as compared to an ideal mask (a design) in R&D environment. Furthermore, by using OPC model and optical model to simulate the same pattern, resist contribution can be isolated.

SUMMARY AND FUTURE WORK

We have demonstrated a working software solution SMDD in mask defect printability check and mask defect post repair verification using SEM image and design as inputs. With the examples from two programmed defects, the results at every step in the whole flow of SMDD were shown. SMDD can accurately convert SEM images to GDSII format polygons, which represents the real mask patterns in AOI. SMDD can then merge the converted mask into the corresponding design, so that wafer resist contour simulation in the AOI can be accomplished with existing OPC model or simple optical model. Finally, SMDD provides easy-to-use analysis and disposition functions for mask defect disposition after the simulation. SMDD has been applied in sub-65nm fabrication application flow. The SMDD simulation tool provides the simulation flexibility and software convenience and makes wafer level printability defect analysis more production-worthy.

The SMDD software was aligned with mask programming defect on wafer printability feedback, using a simulation-based mask defect disposition procedure, mask shop personnel can access data that are important to mask defect disposition criteria without need to actually print by photo stepper and scanner. Such data include wafer CD, the impact of a given defect on linewidth control, the quality of repair, and the degree to which a given feature meet specifications. Mask houses can make good use of the simulated image with good defect printability agreement to analysis the impact of the defect beforehand and also communicate the final result with mask end user to reach consensus.

The phase and/or transmission related defects are also important in mask defects; SEM image capability alone in SMDD limits its completeness in mask defect disposition. SEM images have superior resolution down to nm range, but have no information about phase or transmission related to defects. Extending SMDD to include optical images from inspection system is planned for future. The fundamental difference between SEM images and optical images (transmitted light) is edge profile of those images and so different edge detection algorithm is needed for optical images.

The software SMDD is currently semi-automated. Because the number of defects in production environment is limited and the number of defects to be repaired is even smaller. Thus, the automation requirement of the software is not essential. However, automation improvement is also planned in the future.

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