

Simulation of Correlated Line-Edge Roughness in Multi-Gate Devices

Xiaobo Jiang, Runsheng Wang* and Ru Huang*

Institute of Microelectronics
Peking University
Beijing 100871, China

*E-mail: ruhuang@pku.edu.cn; r.wang@pku.edu.cn

Jiang Chen

Department of Electronics
Peking University
Beijing 100871, China

Abstract—In this paper, the impacts of correlated line-edge roughness (LER) are investigated. Experimental statistics indicate that, the LER of the two edges in Si channel (Fin or nanowire) have strong cross-correlation, depending on the fabrication process. An improved simulation method based on Fourier synthesis is used to generate pairs of LER sequences with certain cross-correlation. The results show that, device V_{th} distribution is strongly dependent on the cross-correlation, and can exhibit non-Gaussian distribution. Dual-peak distribution appears and enlarges the variation of V_{th} significantly. In addition, a new method to extend 2D LER into 3D LER is proposed for future LER investigation.

Keywords—Variability, Line-edge Roughness (LER), Line-width Roughness (LWR), FinFET, Nanowire

I. INTRODUCTION

As the feature size of devices shrinking into nanometer regime, line-edge roughness (LER) is becoming one of critical issues [1-13], especially in multi-gate devices where both gate LER and channel LER have strong impact on device performance. Most previous studies focus on uncorrelated LER [7-9], or LER with a correlation coefficient of 1 or -1 [10]. The impact of correlated LER has been ignored. However, experimental study shows that, channels with Fin or nanowire shapes have correlated LER of the two edges, and is dependent on fabrication processes [5]. Thus, the correlated LER case should be investigated. Based on our theoretical model of cross-correlation in LER [14], the correlated channel LER effect in double-gate (DG) devices is investigated in this paper by statistical simulations, providing helpful guidelines for the design optimization of LER in multi-gate devices. Furthermore, a new method is proposed to extend 2D LER to 3D LER for future LER investigation.

II. CHARACTERIZATION OF CORRELATED LER

The generally accepted model based on the methodology of auto-correlation function [3] uses two parameters for the description of LER: the root mean square (rms) Δ and correlation length λ . In order to describe the cross-correlation of two LERs, correlation coefficient ρ and an additional parameter called translation length ξ are introduced (Fig. 1) as follows:

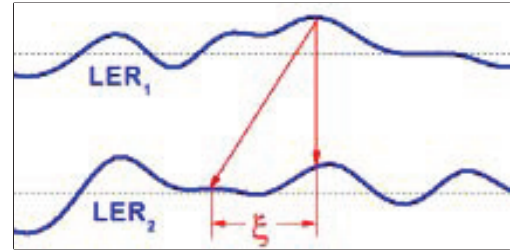
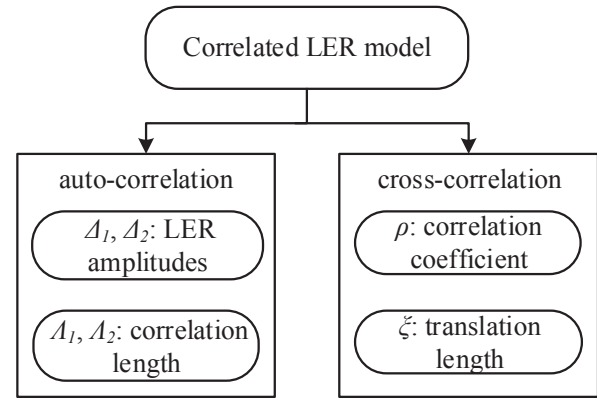


Fig. 1 Characterization of correlated LER.

$$ACF_i(x) = \Delta_i^2 \exp(-x^2/\Lambda_i^2); i=1,2 \quad (1)$$

$$CCF(x) = 2b_0r(x) + b_1[r(x+\xi) + r(x-\xi)] + b_2[r(x+2\xi) + r(x-2\xi)] + \dots \quad (2)$$

$$r(x) = IFT\left[\sqrt{FT(ACF_1)FT(ACF_2)}\right] \quad (3)$$

where

ACF denotes the auto-correlation function;

CCF denotes the cross-correlation function;

FT denotes Fourier transform;

IFT denotes inverse Fourier transform.

ρ reflects how strong the cross-correlation is, and ζ reflects how vast the cross-correlation is. The cross-correlation information was extracted from experimental results [5], in which the Fin channel was patterned by three different techniques, and the nanowire was achieved by self-limiting oxidation of the initial patterned silicon bar [15-21]. The results indicate that cross-correlation differs from one process to another, and strong cross-correlation (large ρ and large ζ) exists in both Fin and nanowire LERs.

III. STATISTICAL SIMULATION

A. Simulation Method

The pioneering work adopted Fourier synthesis to generate uncorrelated random LER sequences [3], which is not able to produce correlated pair-LER sequences. In this work, linear transform is used to induce certain cross-correlation into random sequences, as shown in Fig. 2. The correlation coefficient of wn_1 and wn_2 is decided by the constant a . By

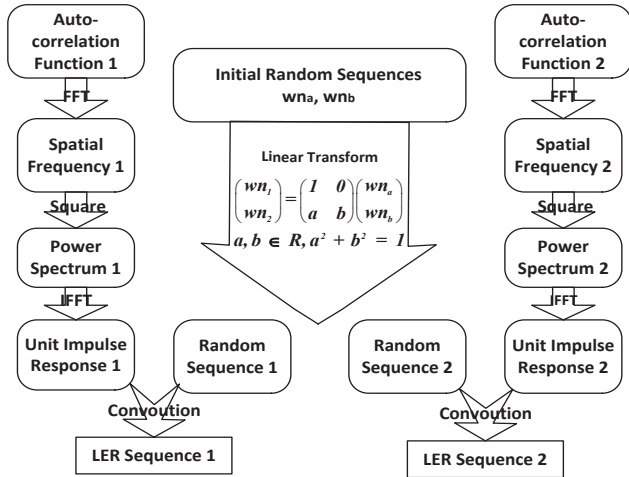


Fig. 2 Flow chart of the improved simulation method.

TABLE I. SIMULATION SPECIFICATIONS

Parameter	Value
Channel Thickness	8 nm
Oxide Thickness	1 nm
Gate length	20 nm
S/D extension	25 nm
Channel Doping	intrinsic
SDE Doping	$1e20 \text{ cm}^{-3}$
LER \mathcal{L}	0.7 nm
V_{dd}	0.8V

convolution with unit pulse response generated from auto-correlation function, the cross-correlation is extended to the final LER sequences. Actually, the final correlation coefficient ρ is affected by both the constant a and the two LER auto-correlation functions. Certain corresponding relations can be found between a and ρ when the auto-correlation functions are set.

2-D statistical device simulation is performed with Synopsys Sentaurus [22]. The device parameters are listed in Table I. Different types of cross-correlation are considered. For each type, 500 samples are simulated for $\mathcal{L}/L_g = 0.5$, and 200 samples are simulated for $\mathcal{L}/L_g = 1.5$.

B. Results and Discussions

Fig. 3 shows the electron density distribution in the devices with different correlation coefficient, and the statistical transfer characteristics are demonstrated in Fig. 4. Both cases share similar $\langle I_{on} \rangle$ and $\langle I_{off} \rangle$, but the variation is much larger when ρ is negative. The distributions of V_{th} without considering cross-correlation are plotted in Fig. 5. Then, four types of typical

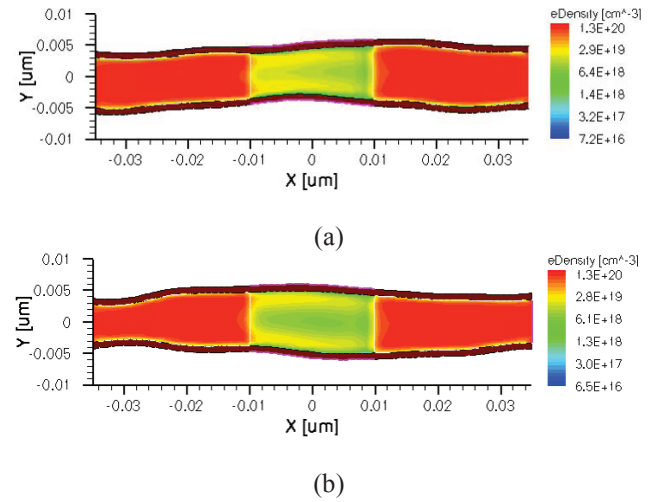


Fig. 3 Electron Density distributions of DG devices with $\mathcal{L} = 10 \text{ nm}$, $\zeta = 0$, and (a) $\rho = 0.5$; (b) $\rho = -0.5$.

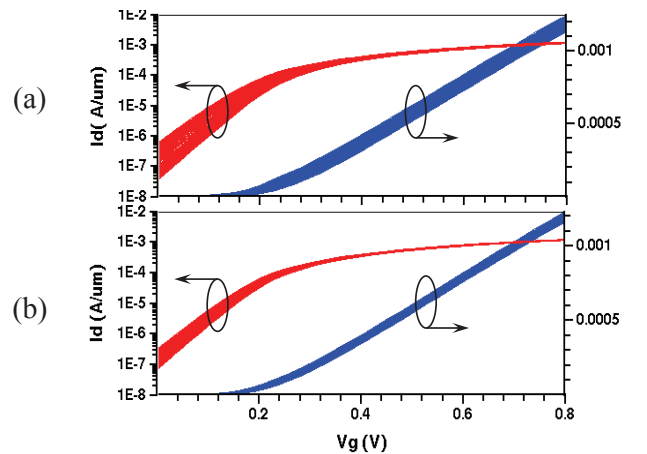


Fig. 4 Transfer characteristics of DG devices with different cross correlation properties: (a) $\rho = -0.5$ and (b) $\rho = 0.5$.

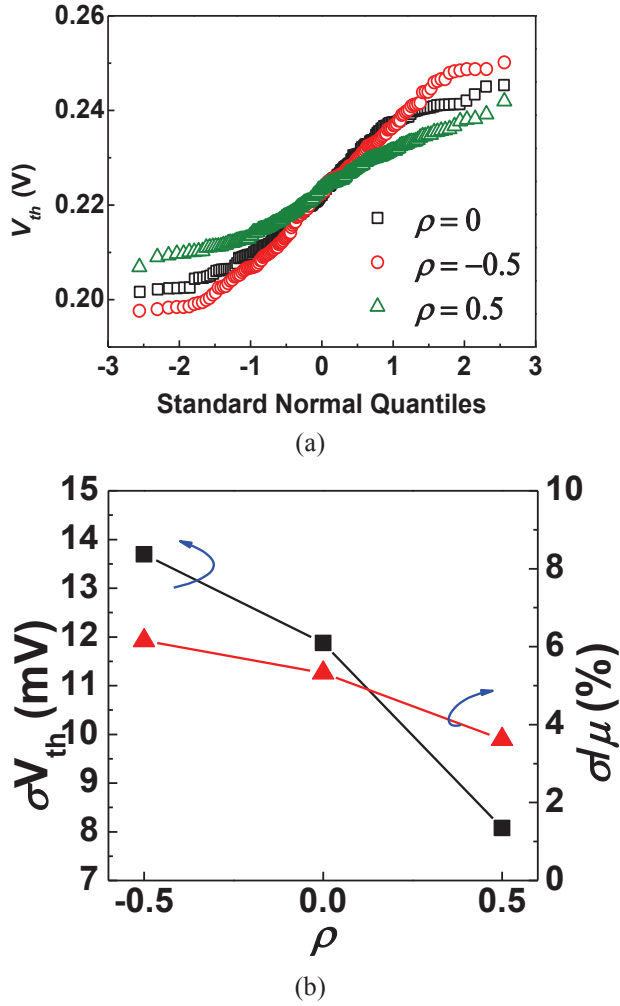


Fig. 5 V_{th} distribution from conventional simulation: (a) the Q-Q test shows that conventional V_{th} distributions fit well with Gaussian distribution; (b) normalized deviation of V_{th} is smaller than 6%.

cross-correlation are taken into account, as shown in Fig. 6. Conventional simulation (Fig. 5) shows Gaussian-like distributions under different correlation coefficients, while new simulation shows that non-Gaussian distribution can be observed depending on cross-correlation type. And due to the appearance of dual-peak, the variation becomes much larger than conventional situation. As shown in Fig. 7, $\Delta\mu/\mu$ reaches up to 19%, while conventional normalized standard deviation is only 6%. Furthermore, as indicated in section II, cross-correlation depends on the fabrication process. According to our experimental results, channels patterned by hard mask trimming technique, are likely to have cross-correlation type (c) and (d), those by spacer define technique are similar to type (b) and (d), while those by e-beam lithography are likely to have type (a), (c) and (d).

IV. FROM 2D LER TO 3D LER

Due to the unique feature of device structure, nanowire devices have more complicated LER. A new method to form 3D nanowire structure with correlated LER edges is proposed,

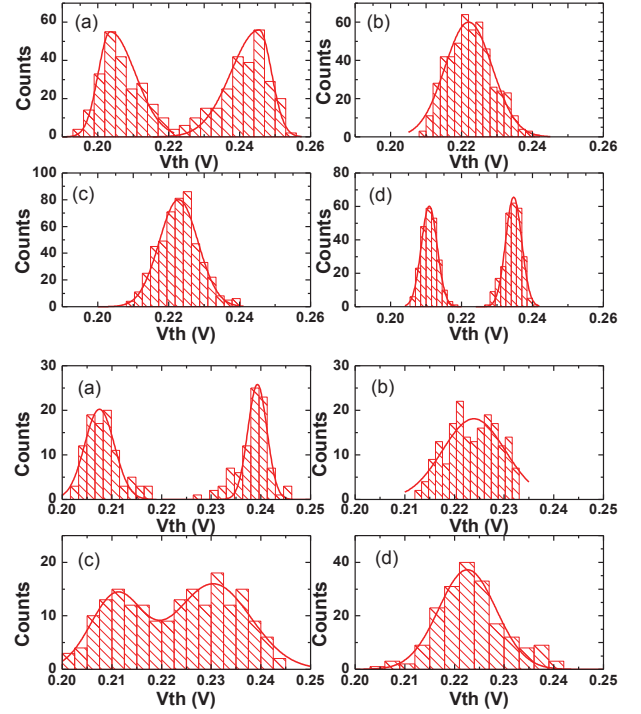


Fig. 6 Distributions of threshold voltage under four types of cross correlation: (a) $\rho = -0.5$, $\zeta/\Lambda = 0\sim 0.2$; (b) $\rho = 0.5$, $\zeta/\Lambda = 0\sim 0.2$; (c) $\rho = -0.5$, $\zeta/\Lambda = 0.4\sim 0.6$; (d) $\rho = 0.5$, $\zeta/\Lambda = 0.4\sim 0.6$, with $\Lambda/L_g = 0.5$ (up) and $\Lambda/L_g = 1.5$ (down).

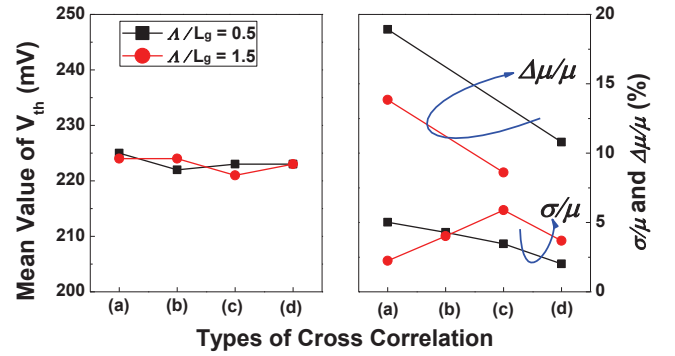


Fig. 7 Four types of cross correlation share similar mean V_{th} (left); σ/μ is smaller than 10% in four cases while $\Delta\mu/\mu$ is up to 19% (right).

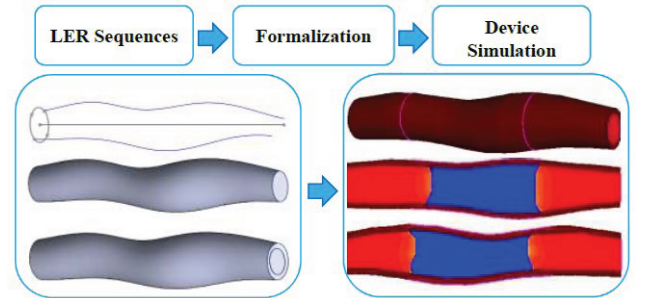


Fig. 8 Formalization of nanowire transistor with correlated LER edges (left), and the cross-sectional shapes with showing the doping concentration of the device (right).

as shown in Fig. 8. The formalization of the structure is done by 3D CAD software, and the output boundary file can be inputted to Sentaurus for the following device simulation. By this method, the cross-sectional shape of nanowire can be kept as round as it can be, but with correlated 3D LER, which is close to the real fabricated case.

V. SUMMARY

In this paper, the effect of correlated LER is studied based on DG devices. The results indicate V_{th} distribution has strong dependence on the cross-correlation of LER, which was missing in previous studies. Multi-peak distribution is observed, and the variation is much larger than conventional method, which indicates that the LER effect could be underestimated if without considering the cross-correlation of LERs. In addition, a new method is proposed to extend 2D LER into 3D LER for future LER investigation.

ACKNOWLEDGMENT

This work was partly supported by the 973 Projects (2011CBA00601), NSFC (61106085 and 60625403), and National S&T Major Project (2009ZX02035-001).

REFERENCES

- [1] ITRS 2011 (<http://www.itrs.net>)
- [2] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya, and G. Slavcheva, "Simulation of intrinsic parameter fluctuations in decanometer and nanometer-scale MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1837–1852, Sept., 2003.
- [3] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuations in decanometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254-1260, May 2003.
- [4] K. Patel, T.-J. King, and C. J. Spanos, "Gate line edge roughness model for estimation of FinFET performance variability," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3055-3063, Dec. 2009.
- [5] R. Wang, T. Yu, R. Huang, Y. Ai, S. Pu, Z. Hao, J. Zhuge, Y. Wang, "New Observations of Suppressed Randomization in LER/LWR of Si Nanowire Transistors: Experiments and Mechanism Analysis," in *IEDM Tech. Dig.*, 2010, pp. 792-795.
- [6] R. Wang, J. Zhuge, R. Huang, T. Yu, J. Zou, D.-W. Kim, D. Park, and Y. Wang, "Investigation on variability in metal-gate Si nanowire MOSFETs: Analysis of variation sources and experimental characterization," *IEEE Trans. Electron Devices*, vol. 58, pp. 2317-2325, Aug. 2011.
- [7] D. Reid, C. Millar, S. Roy, and A. Asenov, "Understanding LER-induced MOSFET VT variability-part I: three-dimensional simulation of large statistical samples," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2801-2807 Nov. 2010.
- [8] D. Reid, C. Millar, S. Roy, and A. Asenov, "Understanding LER-induced MOSFET VT variability-part II: Reconstructing the distribution," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2808-2813 Nov. 2010.
- [9] X. Wang, A. R. Brown, B. Cheng, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *IEDM Tech. Dig.*, 2011, pp. 103-106.
- [10] T. Yu, R. Wang, R. Huang, J. Chen, J. Zhuge, and Y. Wang, "Investigation of nanowire line-edge roughness in gate-all-around silicon nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2864-2871, Nov. 2010.
- [11] E. Baravelli, A. Dixit, R. Rooyackers, M. Jurczak, N. Speciale, and K. De Meyer, "Impact of line-edge roughness on FinFET matching performance," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2466–2474, Sep. 2007.
- [12] E. Baravelli, M. Jurczak, N. Speciale, K. De Meyer, and A. Dixit, "Impact of LER and random dopant fluctuations on FinFET matching performance," *IEEE Trans. Nanotechnol.*, vol. 7, no. 3, pp. 291–298, May 2008.
- [13] E. Baravelli, L. D. Marchi, and N. Speciale, "Fin shape fluctuations in FinFET: Correlation to electrical variability and impact on 6-T SRAM noise margins," *Solid State Electron.*, vol. 53, no. 9, pp. 1303–1312, Sep. 2009.
- [14] X. Jiang, M. Li, R. Wang, J. Chen, and R. Huang, "Investigations on the Correlation between Line-edge-roughness (LER) and Line-width-roughness (LWR) in Nanoscale CMOS Technology," *ICSICT*, pp. 684-686, 2012.
- [15] Y. Tian, R. Huang, Y. Wang, J. Zhuge, R. Wang, J. Liu, X. Zhang, Y. Wang, "New self-ligned silicon nanowire transistors on bulk substrate fabricated by epi-free compatible CMOS technology: process integration, experimental characterization of carrier transport and low frequency noise," in *IEDM Tech. Dig.*, 2007, pp. 895-898.
- [16] J. Fan, R. Huang, R. Wang, Q. Xu, Y. Ai, X. Xu, M. Li, Y. Wang, "Two-dimensional self-limiting wet oxidation of silicon nanowires: experiments and modeling," *IEEE Trans. Electron Devices*, submitted for publication.
- [17] N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, C. H. Tung, K. M. Hoe, S. R. Omampuliyur, D. Tripathi, A.O. Adeyeye, G. Q. Lo, N. Balasubramanian, D. L. Kwong, "Ultra-Narrow Silicon Nanowire Gate-All-Around CMOS Devices: Impact of Diameter, Channel-Orientation and Low Temperature on Device Performance," in *IEDM Tech. Dig.*, 2006, pp. 1-4.
- [18] C. C. Buttner and M. Zacharias, "Retarded oxidation of Si nanowires," *Appl. Phys. Lett.*, vol. 89, no. 26, p. 263 106, Dec. 2006.
- [19] H. Cui, C. X. Wang, and G. W. Yang, "Origin of Self-Limiting Oxidation of Si Nanowires," *Nano Lett.* vol. 8, no. 9, pp. 2731–2737, Aug. 2008.
- [20] F. J. Ma, S. C. Rustagi, G. S. Samudra, H. Zhao, N. Singh, G. Q. Lo, and D. L. Kwong, "Modeling of stress-retarded thermal oxidation of nonplanar silicon structures for realization of nanoscale devices," *IEEE Electron Device Lett.* vol. 31, no. 7, pp. 719–721, July 2010.
- [21] F. Fazzini, C. Bonafos, A. Claverie, A. Hubert, T. Ernst, and M. Respaud, "Modeling stress retarded self-limiting oxidation of suspended silicon nanowires for the development of silicon nanowire-based nanodevices," *J. Appl. Phys.*, vol. 110, p. 033 524, 2011.
- [22] Sentaurus TCAD User's Manual, Synopsys, Mountain View, CA, 2012.