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Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance

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ABSTRACT: CMOS pixel sensors with a small collection electrode combine the advantages of a small sensor capacitance with the advantages of a fully monolithic design. The small sensor capacitance results in a large ratio of signal-to-noise and a low analogue power consumption, while the monolithic design reduces the material budget, cost and production effort. However, the low electric field in the pixel corners of such sensors results in an increased charge collection time, that makes a fully efficient operation after irradiation and a timing resolution in the order of nanoseconds challenging for pixel sizes larger than approximately forty micrometers. This paper presents the development of concepts of CMOS sensors with a small collection electrode to overcome these limitations, using three-dimensional Technology Computer Aided Design simulations. The studied design uses a 0.18 µm process implemented on a high-resistivity epitaxial layer.

KEYWORDS: Charge induction; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc); Radiation-hard detectors; Solid state detectors

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1 Introduction

Monolithic pixel-detector technologies reduce the production effort and cost while reducing the material budget in tracking systems of detectors of high-energy physics experiments. Integrated CMOS pixel sensors with a small collection electrode offer a small sensor capacitance, a favourable signal-to-noise ratio and power consumption, and the potential for excellent spatial and timing resolution [1]. Such sensors have been developed and adopted for the ALICE ITS upgrade using a standard 0.18 μ m CMOS imaging sensor process on a high-resistivity epitaxial layer [2]. Modifying the process to achieve full depletion in the sensor [3] improves the radiation tolerance, of importance for the ATLAS ITk High-Luminosity upgrade [4], as well as the timing resolution, relevant for the CLIC tracking system [5-7]. However, the electric field in the sensor reaches a minimum in the pixel corners resulting in a degraded timing resolution and efficiency loss after irradiation [8-10]. This is more pronounced for larger pixel sizes, and achieving full efficiency and a few ns timing resolution has been proven to be challenging for pixel sizes around 40 µm or larger. This paper presents a study of two improvements of the pixel design in this modified process, a mask change and an additional implant, to further reduce the charge collection time, and therefore improve radiation tolerance and timing resolution while maintaining the small collection electrode and its benefits. The two approaches have been studied using three-dimensional self-consistent transient Technology Computer Aided Design simulations (TCAD [11]) both for non-irradiated and irradiated sensors, and have been implemented in prototype run for the ATLAS experiment [8, 9].

2 Standard and modified process

A $0.18\,\mu m$ CMOS imaging process with a small collection electrode has been studied, as sketched in figure 1.



Figure 1. Schematic cross section (not to scale) of the CMOS standard (left) and modified (right) process with a small collection electrode. The implants of the CMOS circuitry are not shown. The yellow lines indicate the junctions.

Full CMOS circuitry is placed inside p-wells and n-wells shielded by a deep p-well implant. All implants are placed on a high resistivity epitaxial layer that is grown on a low resistivity backside substrate to maximise the depleted region in the sensor. In this standard process (see left side of figure 1), it is difficult to make the depletion layer extend from the junction around the small collection electrode laterally in the epitaxial layer between deep p-well and substrate, especially if the readout circuitry occupies a large fraction of the pixel area. With a deep low-dose n-type implant to create a planar junction under the existing implants (see right plot of figure 1), full depletion of the epitaxial layer is much easier to achieve as the depletion starts at the junction and therefore extends over the full pixel area even with low reverse bias [3, 12].

The concept of moving the junction from a small area around the collection electrode to a larger area deeper in the sensor has been pursued in developments to combine full depletion with a small collection electrode in monolithic sensors, both for bulk or epitaxial layer technologies [13, 14], as well as for Silicon on Insulator (SOI) technologies [15].

3 Low electric field sensor regions

In the fully depleted sensitive layer of the modified process charge collection is governed by drift, and hence by the direction and magnitude of the electric field. However, as will be shown by the three-dimensional TCAD simulations, these sensors with a small collection electrode exhibit a very non-uniform electric field, dropping to zero at the pixel corners.

For the simulation constant voltages were applied to the different electrodes (collection electrode, p-well, substrate) in the silicon structure using ideal contacts and ideal voltage sources. Using this approach, the signal current produced by the sensor is absorbed by these voltage sources without charging up the capacitance associated with these electrodes. This is an ideal or best case allowing to study ultimate limitations on sensor timing performance. In practice, a real front end circuit does not have a zero input impedance like an ideal voltage source, and some charging of the sensor capacitance will happen. Noise contributions from sensor (shot noise) and readout circuit will also degrade timing performance as these effectively introduce random signal fluctuations.

If not mentioned otherwise, the simulations discussed in the following have been performed with a voltage of 0.8 V on the collection electrode and -6 V on the p-wells and backside substrate. Cuts through the pixel centre of the simulated three-dimensional pixel cell are presented.

As shown in figure 2 for a pixel size of $36.4 \times 36.4 \,\mu\text{m}^2$, the lateral electric field is due to symmetry zero at the pixel corners and the electric field along the sensor depth reaches a zero value close to the depth of the deep planar junction, resulting in a zero overall electric field at the pixel corners, a constant electrostatic potential, indicated by a star symbol in the figure. As visualised by the black arrows, the direction of the electric field along the sensor depth results in a push of charge carriers created at various sensor depth at the pixel corner into this electric field minimum. For the propagation of the charge out of this minimum the lateral component of the electric field is crucial.



Figure 2. Results of the electrostatic simulation for the modified process with a pixel size of $36.4 \,\mu\text{m} \times 36.4 \,\mu\text{m}$. The black arrows mark the electric field stream lines, the star symbol indicates the electric field minimum and the white lines mark the edges of the depleted regions.

As shown in figure 3, the size of the lateral field around the electric field minimum depends strongly on the pixel size: the smaller the pixels, the larger the potential gradient and the electric field along the lateral dimension, that helps to push the charge carriers out of this minimum and towards the collection electrode.



Figure 3. Electrostatic potential for the modified process for different pixel sizes. The black arrows mark the electric field stream lines and the white lines mark the edge of the depleted regions.

The importance of considering the direction of the electric field can be understood by inspecting different backside bias voltages for the modified process (see figure 4). For lower backside voltages the potential gradient and thus the electric field along the sensor depth are decreased. At the pixel corner, this results in a change of the direction of the electric field towards the collection electrode and thus a shorter drift path.



Figure 4. Electrostatic potential for different backside voltages for the modified process with a pixel size of $36.4 \,\mu\text{m} \times 36.4 \,\mu\text{m}$. The black arrows mark the electric field stream lines and the white lines mark the edges of the depleted regions.

The electric field minimum results in a slower charge collection, creating a higher probability of charge trapping after irradiation. The resulting dependency of the efficiency after irradiation on the pixel size has been observed in test-beam measurements [8-10, 16]. Moreover, results with different p-well layouts have shown a higher efficiency in pixel regions where the p-well layout leads to a higher lateral field [8, 9].

Overall, the experimental results as well as the TCAD simulations indicate that increasing the lateral field is the key to increasing the charge collection to make CMOS sensors with a small collection electrode radiation hard and achieving precise timing resolution. While the pixel size is limited by the requirement to fit all needed circuitry, a change of the sensor concept is pursued in the following simulation studies to enhance the lateral field while only minimally changing the manufacturing process.

4 Sensor concepts for a faster charge collection — three-dimensional electrostatic simulations

Figure 5 shows two different approaches to increase the lateral electric field at the pixel borders: creating a gap in the deep n-implant, requiring only a mask change, and introducing an additional p-type implant at the pixel border. Additional implants to accelerate the charge collection have also been pursued for image sensors for visible light detection [14] as well as for SOI sensors [15].



Figure 5. Proposed concepts (not to scale) to increase the lateral electric field at the pixel borders: an additional p-implant (left) and gap in the deep n-implant (right). The yellow lines indicate the junctions.

Both approaches proposed here introduce a junction along the sensor depth, significantly increasing the lateral electric field, but also shifting the minimum of the electric field deeper into the silicon compared to the original approach shown in the right side of figure 1. As a result the electric field starts to bend towards the collection electrodes already deeper in the silicon, reducing the drift path and hence the charge collection time. This is illustrated in figure 6 and figure 7 for the gap in the low-dose n-implant and the additional p-type implant, respectively. Cuts through the pixel centre of the simulated three dimensional pixel cell are presented for a simulation with 0.8 V collection electrode bias and -6 V bias on p-wells and substrate with a pixel size of $36.4 \,\mu\text{m} \times 36.4 \,\mu\text{m}$.



Figure 6. Results of the electrostatic simulation for the concept with the gap in the deep n-implant with a pixel size of $36.4 \,\mu\text{m} \times 36.4 \,\mu\text{m}$. The black arrows mark the electric field stream lines, the star symbol indicates the electric field minimum and the white lines mark the edges of the depleted regions.



Figure 7. Results of the electrostatic simulation for the concept with the additional p-implant with a pixel size of $36.4 \,\mu\text{m} \times 36.4 \,\mu\text{m}$. The black arrows mark the electric field stream lines, the star symbol indicates the electric field minimum and the white lines mark the edges of the depleted regions.

5 Transient three-dimensional TCAD simulations

In the previous section the influence of the pixel size and two additional pixel modifications on the electric field was illustrated using electrostatic simulations. To compare the timing response for different cases, three-dimensional transient TCAD simulation results are presented for a Minimum Ionising Particle (MIP) traversing the pixel corner, the worst case in terms of charge collection time. Results are shown both, for non-irradiated sensors and for sensors irradiated with a fluence of 10^{15} neq/cm². To model the effect of radiation damage, defect levels have been introduced, as described in [17]. In the following the influence of the pixel modifications, of the pixel size, and of the sensor reverse backside bias are discussed. The voltage on the collection electrode and p-wells has been set to 0.8 V and -6 V, respectively.

5.1 Pixel modifications

The current induced on a single pixel is presented versus time in figure 8 for the different sensor concepts before (left) and after (right) irradiation for a backside voltage of -6 V. The charge collection time is reduced by a factor of at least two for the proposed concepts. The same general trends can be observed after irradiation. However, the overall pulse heights are significantly reduced, as explained by trapping and recombination of the charge carriers.



Figure 8. Current versus time for different sensor concepts with a pixel size of $36.4 \,\mu\text{m} \times 36.4 \,\mu\text{m}$, simulating a MIP incident at the pixel corner. A significantly faster charge collection has been simulated for the additional p-implant and the gap in the deep n-implant (coloured lines) compared to the modified process (black).

The differences in pulse height have been evaluated by integrating the current pulses and calculating the charge. Figure 9 shows the charge versus integration time before (left) and after (right) irradiation. Differences are already observable before irradiation: while most of the charge



Figure 9. Collected charge versus integration time for different sensor concepts with a pixel size of $36.4 \,\mu\text{m} \times 36.4 \,\mu\text{m}$ before (left) and after (right) irradiation.

is collected for the concept with the additional p-implant and the gap in the deep n-implant, not all charge is collected for the modified process within 25 ns. This illustrates the need of a process modification for faster charge collection even without irradiation for applications with a short integration time. Both proposed pixel improvements increase the collected charge after irradiation by at least a factor of three.

5.2 Pixel size

Moving towards smaller feature sizes will allow smaller pixel sizes while maintaining functionality. Thus, to evaluate the future prospects of the proposed sensor design concepts, the modified process and the concept with the additional p-implant are compared for smaller pixel sizes after irradiation.

Current pulses are presented for a backside voltage of -6 V for different pixel sizes in figure 10, comparing the original modified process from figure 1, with the concept with the additional p-implant in figure 5. Even for small pixel sizes of $20 \,\mu\text{m} \times 20 \,\mu\text{m}$ the additional p-type implant



Figure 10. Current pulses simulating a MIP incident at the pixel corner for the modified process (black) and the concept with the additional p-implant compared for different pixel sizes after irradiation with a fluence of 10^{15} neq/cm². Note the different scale of the x-axis for a pixel size of $20 \,\mu\text{m} \times 20 \,\mu\text{m}$

significantly accelerates the charge collection, resulting in sub-nanosecond peaking times. The charge versus integration time for different pixel sizes presented in figure 11, shows that the charge lost after irradiation can be recovered by going to smaller pixel sizes as well as by the proposed sensor modifications.



Figure 11. Collected charge versus integration time for the modified process (black) and the concept with the additional p-implant (red) compared for different pixel sizes after irradiation with a fluence of 10^{15} neq/cm².

5.3 Sensor reverse bias

The maximal reverse bias voltage applicable to the p-wells is limited by the CMOS circuitry to -6 V [18]. The deep low-dose n-implant isolates the p-wells from the backside substrate and allows for a higher reverse bias on the substrate. The two pixel improvements weaken this isolation, resulting in a high current flow between the p-wells and the backside substrate (punch-through). This is further investigated here by fixing the collection electrode and p-well bias to 0.8 and -6 V respectively, and sweeping the substrate bias from 0 V to -20 V.

For each step of the backside voltage the current flow between the backside and the p-wells has been calculated, as presented in figure 12. A high current flow is observable for absolute backside

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voltages below the 6 V applied to the p-wells, since the small depletion of the epitaxial layer does not sufficiently isolate the p-wells from the backside, resulting in punch through between the p-wells and the backside substrate. For absolute backside voltages higher than the 6 V applied to the p-wells, the modified process shows the expected isolation. For the additional p-implant and the gap in the deep n-implant this isolation is reduced to a smaller voltage range and minimal for the sensor concept with the gap in the deep n-implant, leading to punch-through at lower absolute bias voltages.

A simulation of a MIP traversing the pixel corners has been performed for the modified process applying higher backside voltages, to investigate the impact on the charge collection time. The current pulses after irradiation are presented in figure 13.

2e-09



Le-09 0 5e-09 1e-08 2e-08 2e-08 2e-08 Time [s]

Figure 12. Current flow between the p-wells and the backside for the different sensor concepts with a size of $36.4 \,\mu\text{m} \times 36.4 \,\mu\text{m}$.

Figure 13. Current pulse simulating a MIP incident at the pixel corner for different backside voltages for the modified process with a pixel size of $36.4 \,\mu\text{m} \times 36.4 \,\mu\text{m}$.

In the pixel corners a slight improvement can be noted for a backside voltage of -15 V. An even higher backside voltage of -20 V reduces the pulse height and thus the amount of collected charge, as explained by the higher electric field along the sensor depth that results in a longer drift path, a slower charge collection and a higher recombination probability after irradiation (see figure 4).

6 Summary

By combining the advantages of a small sensor capacitance and a fully monolithic technology, CMOS pixel sensors with a small collection electrode address the requirements of future experiments. However, experimental evidence showed that after irradiation signal charge was lost at the pixel corners causing severe detection inefficiencies even after a process modification to fully deplete the epitaxial layer. Three-dimensional electrostatic TCAD simulations identified an electric field minimum at the pixel corners increasing the charge collection time and thus the probability of charges to be trapped after irradiation. Two different further sensor modifications were presented to reduce this electric field minimum and accelerate the collection of signal charge from the pixel edge towards the collection electrode. This not only reduces the probability of the signal charge to be trapped but simultaneously improves the precision of the time stamping capability. Three dimensional transient TCAD simulations show these sensor modifications indeed accelerate the charge collection time by approximately a factor four. This gives confidence that the post irradiation performance will be improved, and the post-irradiation simulations confirm this: the amount of collected charge after irradiation with a fluence of 10^{15} neq/cm² has been increased by a factor of approximately three in simulations for a 36.4 µm pixel pitch, with an additional further improvement for smaller pixel pitches. The post-irradiation models taken from literature have not been specifically developed and tuned for epitaxial material limiting the quantitative precision of post-irradiation predictions. However, the underlying concept of accelerating the charge collection and thereby decreasing the recombination probability is not dependent on the irradiation model.

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