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ABSTRACT

Single-electron transistors (SETs) have been extensively used as charge sensors in many areas, such as quantum computations. In general, the signals of SETs are smaller than those of complementary metal–oxide–semiconductor (CMOS) devices, and many amplifying circuits are required to enlarge the SET signals. Instead of amplifying a single small output, we theoretically consider the amplification of pairs of SETs, such that one of the SETs is used as a reference. We simulate the two-stage amplification process of SETs and CMOS devices using a conventional SPICE (Simulation Program with Integrated Circuit Emphasis) circuit simulator. Implementing the pairs of SETs into CMOS circuits makes the integration of SETs more feasible because of direct signal transfer from the SET to the CMOS circuits.

Single-electron transistors (SETs) have been intensively investigated owing to their advantages of low-power operation, which is desirable for application to logic and memory elements.[1,2] Since the Tucker's proposal,[3] many approaches have been developed to replace the elements in complementary metal–oxide–semiconductor (CMOS) circuits.[4–9] SETs were also investigated after they were directly embedded in CMOS circuits.[8–10] Currently, conventional Si transistors are much smaller than SETs. SETs have attracted attention as charge sensors,[11–13] which have been used for the readouts of silicon qubits[14–16] or as current standards.[17–19]

The SET consists of a small metallic island or a degenerated semiconductor island surrounded by a source and drain via tunneling junctions with low capacitances. The SET yields periodic outputs referred to as Coulomb oscillations, which vary as a function of the gate voltage, and the oscillation period corresponds to the change in the number of electrons in the island. The maximum signal change in a SET is the difference between the peak and the trough of the Coulomb oscillation. The SET current is sensitive to electric potential variations on the SET island.[11] The standard readout process of a spin qubit [spin in localized states, such as a single impurity or quantum dot (QD)] is a spin-to-charge conversion, and the change in charge of the localized state is detected by the SET current.[14,15,20,21]

There are many methods for the detection of charges, such as the use of radio frequency SETs (rf-SETs)[15,20,21] and the direct measurement of the SET by a single GaAs amplifier.[22,23] Inokawa *et al.* showed that a Coulomb oscillation is effectively outputted by directly connecting the SET to an MOS field-effect transistor. They experimentally demonstrated multiple-valued logic by SETs operating at 27 K. The effectiveness of the series coupling of the SET with MOS transistors was also experimentally investigated by Uchida *et al.*[10] Scalable SET sensing systems require scalable circuits. However, previous SET sensors[14–19] did not explicitly consider the array of SETs as part of CMOS circuits.

In this study, we theoretically consider a scalable detection circuit based on the implementation of many SETs in CMOS circuits. Our basic concept of the amplification of the SET signals consists of two stages, as shown in Fig. 1. The first amplification stage of the process is conducted by direct connection of the SET to p-channel MOS (pMOS) transistors. In the second stage, we introduce a reference and a target SET and amplify the difference between two SETs using standard amplifier circuits, such as the differential amplifier (DA) circuits and the static random-access memory (SRAM) cells.

For smooth connection to the digital circuits, the output of the sensing circuit should be a digital signal (either a "0" or a "1"). For this purpose, it is better to compare the relative output of the target SET with that of the reference SET. In our application of the SRAM cell, the relative voltage difference between the target SET and the reference SET is found to be quickly latched to 0 or 1. This is in contrast to the

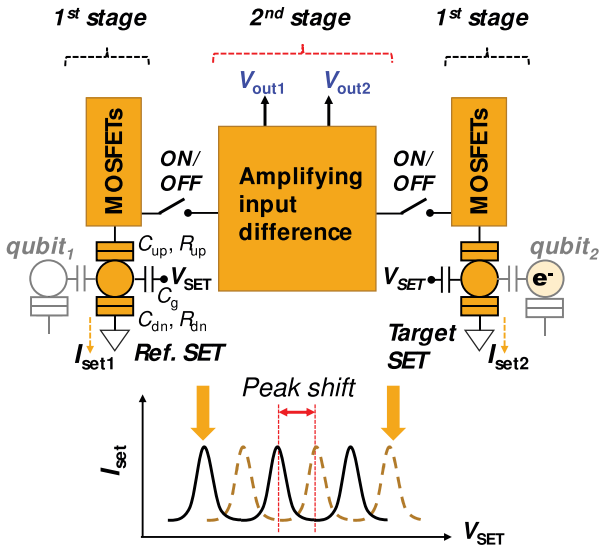

FIG. 1. Concept of our two-stage amplification circuit of the charge-sensing single-electron-transistor (SET). Instead of amplifying one SET sensor, we consider amplifying pairs of SETs that have different states with each other. Depending on the existence of the extra electron in the quantum dot (QD) outside the SETs, the electric potential of the island of the SETs changes. Throughout this paper, we model the effects of the electric potential of the QDs and V_{SET} by the gate voltages V_{G1} and V_{G2} of the SETs. The pairs of SETs are selected by the switches between the first and second stages.

measurements in Refs. 14–16, wherein the results were obtained after the analysis of a series of time-dependent SET currents. Our CMOS circuits are assumed to be close to the SETs. In addition, the target and the reference SETs are chosen by switching on the wordline transistors between the pairs of SETs and amplifiers. Then, the circuit using the pairs of SETs becomes more compact than the amplifying circuit of a single SET. Accordingly, our proposal is suitable for an array of sensing SETs.

In this study, we implement the current characteristics of the orthodox theory of the SET[24] into the SPICE (Simulation Program with Integrated Circuit Emphasis) circuit simulator based on the BSIM4 (Berkeley short-channel transistor model, level = 54) by using the standard modeling language of the Verilog-A. We considered two types of SETs: one of which is operated at low (4.2 K) and the other is operated at high temperatures (243 K). At low temperatures (LT), such as 4.2 K, the threshold voltage of the MOS transistors becomes higher because of the incomplete ionizations. Many studies regarding cryo-CMOS[25–28] have been conducted to determine the model parameters at low temperatures. However, the general compact model is not available for such low temperature. In addition, the basic CMOS operations are basically the same as that at room temperature (RT). Thus, we applied the CMOS parameters that are available in the conventional SPICE models to the CMOS parts for both types of the SETs. In the following, circuit calculations are mainly conducted at $T = 243$ K, which is in the range of the conventional models.

We consider CMOSs with gate lengths of $L = 90$ nm and $L = 65$ nm, whose drain voltages V_D are 1.2 and 1.0 V, respectively. We also consider the effects of small variations in the SETs and CMOS transistors. The purpose of the comparison of pairs of SETs is to detect the changes in the Coulomb oscillations of the target SET. Thus, given that the voltage difference between the peak and trough currents of the Coulomb oscillations can be distinguished, we will be able to detect the changes of the target SET even if there are variations in the devices.

Herein, we consider four SETs, as listed in Table I. The LT-SET*t* (target) and LT-SET*r* (reference) are operated at 4.2 K, and RT-SET*t* and RT-SET*r* can operate at 243 K. The parameters of the LT-SET*t* (RT-SET*t*) exhibit 10% variations compared with those of the LT-SET*t* (RT-SET*r*). The calculated current–voltage characteristics (I_D–V_D) are listed in the supplementary material. The charging energy is given by $E_c \equiv e^2/[2(C_{up} + C_{dn} + C_g)]$, where C_{up} and C_{dn} are the capacitances of the upper and under tunneling barrier of the left and right SETs, respectively, and C_g is the gate capacitance (Fig. 1). The magnitude between the peak and trough currents is on the order of pA, and its voltage change estimated by pA $\times$ 25.9 k Ω = 25.9 μV is very small (25.9 kΩ is a quantum resistance[1]). On the other hand, the variations in the threshold voltage V_{th} of conventional CMOSs are generally on the order of millivolts. Therefore, we need to amplify the SET outputs before connecting the SETs to conventional CMOS circuits.

We start from the first amplification stage in which the SET is directly connected to the CMOS transistors, as shown in Fig. 2(a). By a series connection, the low SET current value increases with CMOS.[8] Figure 2(b) shows that the amplification of the SET signal becomes prominent at $V_{Gp} \gtrsim 0.9$ V. The distortions of the waveforms compared with the original Coulomb oscillations originate from the nonlinearity of the I_D–V_D characteristics of the pMOS transistors. We analyze the amplification mechanism based on the standard long-channel model.[29] The I_D–V_D of CMOS transistors depend on the triode region $|V_{DS}| < |V_{GS} - V_{th}|$ or the saturation region $|V_{DS}| > |V_{GS} - V_{th}|$. At present, amplification is observed in $|V_{DS}| = |V_{out} - V_D| \approx 1.05$ V $> |V_{GS}| = |V_{Gp} - V_D| = 0.15$ V (saturation region). The SET current I_{SET} under large source–drain voltage is approximately described by $I_{SET} \propto V_{SET}$ (see the supplementary material). More explicitly, we assume that $I_{SET} \approx V_{SET}/R_D$. Thus, we can write the I_D–V_D characteristics in the saturation region; furthermore, the SET given by

$$I_D = \frac{1}{2}\beta_p (V_{Gp} - V_D - V_{thp})^2 (1 + \lambda(V_D - V_{out})), \quad (1)$$

$$V_{out} \approx R_D I_D, \quad (2)$$

where $\beta_p \equiv \mu_p C_{ox} \frac{W}{L}$ and $\lambda (< 1)$ are the channel length modulation coefficients (L, W, C_{ox}, and μ_p are the length, width, gate capacitance,

TABLE I. The four SETs we use here. C_{up} (R_{up}) and C_{dn}(R_{dn}) are the capacitances (resistances) of the upper and under tunneling barrier of the SETs, respectively. C_g is the gate capacitance.

	Capacitance (aF)			Resistance (Ω)		Temp (K)	
SET	C_{up}	C_{dn}	C_g	R_{up}	R_{dn}	T	E_c (meV)
LT-SET*r*	1	10	2	100k	1M	4.2	6.16
LT-SET*t*	1.1	0.9	2.2	110k	0.9M	4.2	6.51
RT-SET*r*	0.1	0.5	0.5	100k	500k	243	72.8
RT-SET*t*	0.11	0.45	0.45	110k	450k	243	79.3

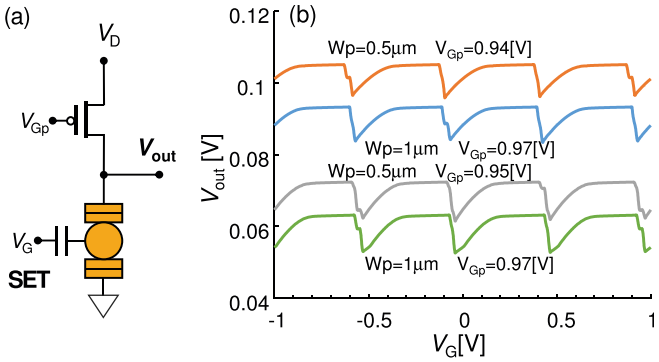

FIG. 2. (a) First-stage amplification circuits, where the LT-SET*t* (see Table I) and pMOS are directly connected. The output voltage V_{out} is amplified depending on the gate voltage V_{Gp} of the pMOS. (b) Numerical results of V_{out} as the function of V_G. Depending on the width of the pMOS ($W_p = 0.5\,\mu$m and $W_p = 1\,\mu$m), the optimal points change. The Coulomb oscillation is amplified up to approximately 10 mV ($V_D = 1.2$ V). Hereafter, we use $W_p = 0.5\,\mu$m pMOS at the first stage.

and mobility of the pMOS, respectively). The solution of these equations is given by

$$V_{\text{out}} = \frac{1 + \lambda V_{\text{D}}}{1 + \lambda I_{D0} R_{\text{D}}} I_{D0} R_{\text{D}}, \tag{3}$$

where $I_{D0} \equiv \frac{1}{2}\beta_p (V_{\text{Gp}} - V_{\text{D}} - V_{\text{thp}})^2$. Because $I_{D0}R_{\text{D}} < V_{\text{D}}$, the SET output is enhanced by $\frac{1+\lambda V_{\text{D}}}{1+\lambda I_{D0} R_{\text{D}}} > 1$. Note that λ is conspicuous in both the $L = 90$ nm and $L = 65$ nm pMOS transistors (see the supplementary material), and we can see that the output voltage oscillates around ~10 mV in Fig. 2(b).

The second-stage amplification is conducted using standard amplifier circuits. Figure 3 shows the results obtained from a basic DA circuit. Note that the gate voltages V_{G1} and V_{G2} represent the shifted electrical potential V_{SET} by the additional sensing QD in Fig. 1. Conventional DAs amplify two inputs with opposite phases. In the case of SETs, two different phases of Coulomb oscillations are input. We consider that the two SET signals possessing different current peaks mimic the two input signals of the conventional DA with different phases. In Fig. 3(b), we show the results for the output voltage difference of $V_{\text{out2}} - V_{\text{out1}}$ for a fixed $V_{G1} = 0$. The voltage difference $V_{\text{out2}} - V_{\text{out1}}$ increases by approximately 50 mV for $L = 90$ nm (the results for $L = 65$ nm are shown in the supplementary material) and can be detected by conventional CMOS amplifier circuits (the following circuits after V_{out2} and V_{out1} are not shown). This enhancement of the Coulomb oscillations is the result of the two-stage amplification of SET signals.

The magnitude of the enhancement of the Coulomb oscillation in Fig. 3(b) changes depending on the threshold voltage variations of the eight MOS transistors. In Fig. 3(c), we provide the distribution of the difference in the peak and trough of $V_{\text{out2}} - V_{\text{out1}}$ obtained through over 300 Monte Carlo simulations of the threshold variations with LT-SET*t* and LT-SET*r* at $V_{G1} = 0$ and $V_{G2} = 0.2$ V. The number of small amplitudes of $|V_{\text{out2}} - V_{\text{out1}}|$ (<5 meV) is nine out of 300 samples. Small amplitudes of $V_{\text{out2}} - V_{\text{out1}}$ can be avoided by applying different voltages such as V_{Gpi} and WL_i on each part of the DA.

We now consider the application of the standard SRAM cell containing six MOS transistors[30] to detect a pair of SETs, as shown in

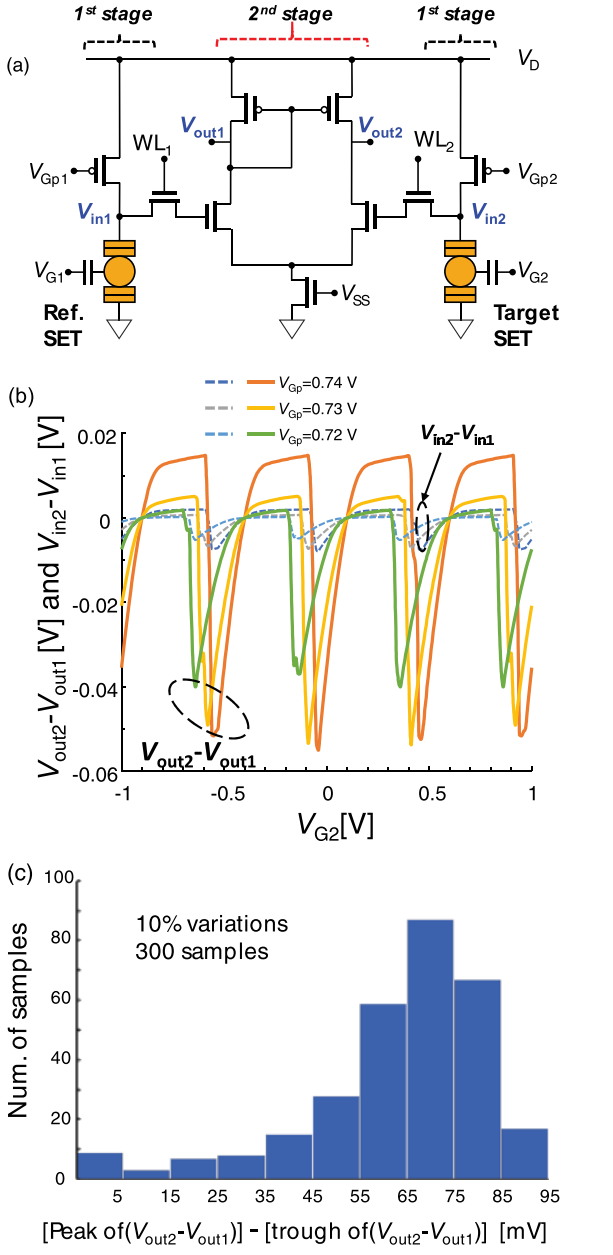

FIG. 3. (a) The differential amplifier (DA) is applied at the second stage amplification of Fig. 1. (b) Numerical results of $V_{\text{out2}} - V_{\text{out1}}$ (enhanced Coulomb oscillations) and $V_{\text{in2}} - V_{\text{in1}}$ for $L = 90$ nm at $V_{G1} = 0$. $V_{Gp1} = V_{Gp2} = V_{Gp}$. The pMOS and nMOS widths of the DA are given by $W_{pa} = 1\,\mu$m and $W_{na} = 10\,\mu$m, respectively. The width of the wordline nMOS is given by $W_n = 5\,\mu$m. $V_D = 1.2$ V. We can see that the amplitude of $V_{\text{out2}} - V_{\text{out1}}$ is approximately 50 mV, which is larger than the amplitude of the input $V_{\text{in2}} - V_{\text{in1}}$. (c) Histogram of the Monte Carlo simulation of the output difference when the V_{th} of all CMOS transistors varies by 10% over 300 simulations.

Fig. 4(a). Figure 4(b) shows the simulation results of the time-dependent SRAM cell outputs V_{out1} and V_{out2} of the two LT-SET*t*s. We can see that $V_{\text{out1}} < V_{\text{out2}}$ for $V_{G2} = 0.1$ V, but $V_{\text{out1}} > V_{\text{out2}}$ for $0.15\,\text{V} \le V_{G2} \le 0.4$ V for $L = 90$ nm devices. This implies that the

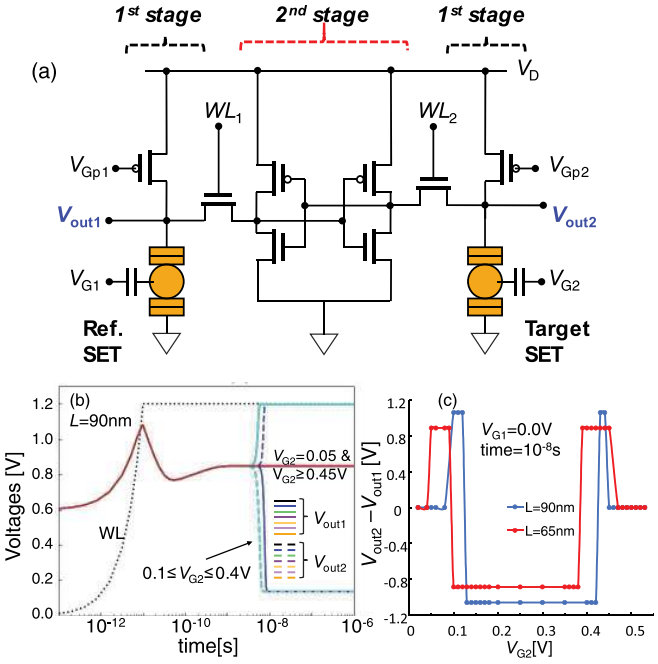

FIG. 4. (a) Six transistor static random-access memory (SRAM) cells applied in the second-stage amplification of Fig. 1. (b) Time-dependent voltage behaviors of the SRAM setup of $L = 90$ nm for widths $W_n = 0.5$ μm and $W_p = 1.2W_n$. The width of the *WL* transistor is 0.4 μm. $V_{Gp} = 0.55$ V and $V_{G1} = 0.0$ V using the LT-SET*t*s. The change in V_{out1} and V_{out2} is in the range of $V_{G2} = \{0, 0.05, 0.1, 0.15, 0.2, 0.25\ 0.3, 0.35, 0.4, 0.45, 0.5\}$ V. (c) Replotting of (b) as a function of V_{G2} of (b) and the result for $L = 65$ nm.

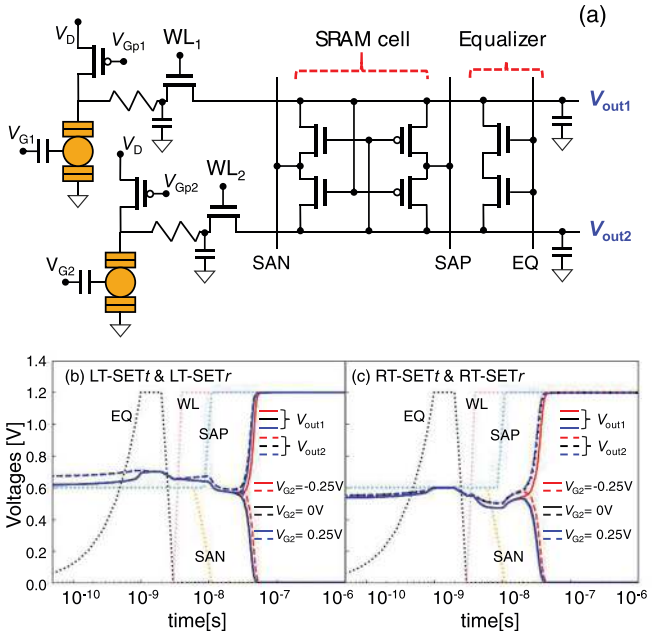

FIG. 5. (a) Dynamic RAM(DRAM)-like detection circuits are applied at the second stage amplification of Fig. 1. The stray capacitance of 1 pF is added to the nodes V_{out1} and V_{out2}, inputs of the SETs, and equalizer circuits, and the wire resistor of 100 Ω is also added. The signal EQ equilibrates the voltages of the two output lines. The WL_1 and WL_2 show the signals for the access transistors that connect the SET to the output lines. The bistable state of the output pair is realized by activating the SAN and SAP signals. (b) and (c) Time-dependent characteristics of the different SET pairs [the LT-SET pair in (b) and RT-SET pair in (c)] in (a) with 10% threshold voltage variations in the MOS transistors. The pulse sequence is constituted following the standard DRAM sequence of Refs. 32 and 33. $V_{G1} = 0$ is fixed and V_{G2} changes. Depending on whether $V_{G1} > V_{G2}$ or $V_{G1} < V_{G2}$, the outputs V_{out1} and V_{out2} change from $V_{out1} > V_{out2}$ to $V_{out1} < V_{out2}$. The widths of the nMOS and pMOS are 0.5 and 0.6 μm, respectively. The width of the equalizer nMOS is 20 μm. The width of the access transistors is 0.6 μm ($V_{Gp1} = V_{Gp2} = 0.87$ V, $L = 90$ nm).

shift in the electric potential of the sensing QD from $V_{G2} = 0.1$ V to $V_{G2} = 0.15$ V changes the electric potential of the target SET island, resulting in a change in the relative magnitude between V_{out1} and V_{out2}. Figure 4(c) replots $V_{out2} - V_{out1}$ in Fig. 4(b) as a function of V_{G2} with the results for $L = 65$ nm at time 10^{-8} s. Thus, we can detect the change in the target SET represented by V_{G2} by measuring the relative outputs of the SRAM cell. Herein, the initial voltage at the SRAM cell input is set to $V_D/2$, and stray capacitances of 0.2 pF are included at the input nodes of the SRAM cell (figures not shown). As the stray capacitance increases, the time to split increases.

In general, SRAM cells undergo initial threshold voltage V_{th} variations,[31] and we have to consider these variations in the MOS transistors as well as the two SETs. Here, we extend the SRAM cell circuit to a dynamic random-access memory (DRAM)-like structure[32,33] in Fig. 5(a), where it is considered that the equalizer circuit mitigates the voltage difference of the wordlines between the two SETs. Figures 5(b) and 5(c) show two types of readouts for the two types of SETs. The equalizer signal EQ (EQualizer) is activated at 1 ns and stopped after 2 ns. The SAN (Sense-Amplifier N-Fet Control) and SAP (Sense-Amplifier P-Fet Control) signals are activated after the equalizer at $t = 6$ ns and $t = 8.5$ ns. The wordlines WL_1 and WL_2 (WL = WL_1 = WL_2) are activated at 4 ns. We can see that the change in the gate voltage V_{G2}, which corresponds to the existence of the charge sensor QD, causes the outputs V_{out1} and V_{out2} to change from $V_{out1} > V_{out2}$ to $V_{out1} < V_{out2}$.

In a realistic situation, it is possible that the temperature changes. Therefore, we also calculated the temperature dependence of the amplifier response. It is desirable that the relative magnitude of V_{out1} to V_{out2} does not change even when the operating temperature changes. The temperature dependencies of the characteristics of the DA (Fig. 3) and DRAM (Fig. 5) are robust against temperature changes as long as the temperature change is sufficiently small on the order of several tens of degrees (see the supplementary material).

Considering that there are variations in SETs and MOS transistors, we may have to check and record the basic characteristics of each device at the first calibration stage of the chip. The *I*–*V* characteristics of each SET should be clarified before using the charge-sensing SET. This information is stored in the extra SRAM or other memories and becomes the overhead of the system. An effective method for determining the optimal biases automatically is a future issue. It is possible that the applied voltages destroy the SET charge states. However, herein, we neglected the effects of the backaction from the CMOS circuits. Hence, the assessment of the backaction remains a future issue.

In conclusion, we proposed two-stage amplification circuits for SETs. Based on serial connections with MOS transistors and a

comparison with the reference SET, we numerically show that the readout of the charge-sensing SET is greatly enhanced. We also considered the effects of variations in the MOS transistors and SETs and show that as long as the variations are small, the two SETs can be compared effectively.

See the supplementary material for the complete derivation process of the equations.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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