

Home Search Collections Journals About Contact us My IOPscience

Single-crystalline $\rm Ni_2Ge/Ge/Ni_2Ge$ nanowire heterostructure transistors

This article has been downloaded from IOPscience. Please scroll down to see the full text article. 2010 Nanotechnology 21 505704 (http://iopscience.iop.org/0957-4484/21/50/505704)

View the table of contents for this issue, or go to the journal homepage for more

Download details: IP Address: 164.67.26.22 The article was downloaded on 07/01/2011 at 02:39

Please note that terms and conditions apply.

Single-crystalline Ni₂Ge/Ge/Ni₂Ge nanowire heterostructure transistors

Jianshi Tang^{1,4}, Chiu-Yen Wang^{2,4}, Faxian Xiu¹, Augustin J Hong¹, Shengyu Chen², Minsheng Wang¹, Caifu Zeng¹, Hong-Jie Yang³, Hsing-Yu Tuan³, Cho-Jen Tsai², Lih Juann Chen² and Kang L Wang¹

 ¹ Device Research Laboratory, Department of Electrical Engineering, University of California, Los Angeles, CA 90095, USA
² Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, 30013 Taiwan, Republic of China
³ Department of Chemical Engineering, National Tsing Hua University, Hsinchu, 30013 Taiwan, Republic of China

E-mail: tjianshi@ucla.edu and ljchen@mx.nthu.edu.tw

Received 9 September 2010, in final form 21 October 2010 Published 22 November 2010 Online at stacks.iop.org/Nano/21/505704

Abstract

In this study, we report on the formation of a single-crystalline Ni₂Ge/Ge/Ni₂Ge nanowire heterostructure and its field effect characteristics by controlled reaction between a supercritical fluid–liquid–solid (SFLS) synthesized Ge nanowire and Ni metal contacts. Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) studies reveal a wide temperature range to convert the Ge nanowire to single-crystalline Ni₂Ge by a thermal diffusion process. The maximum current density of the fully germanide Ni₂Ge nanowires exceeds 3.5×10^7 A cm⁻², and the resistivity is about 88 $\mu\Omega$ cm. The *in situ* reaction examined by TEM shows atomically sharp interfaces for the Ni₂Ge/Ge/Ni₂Ge heterostructure. The interface epitaxial relationships are determined to be Ge[011] || Ni₂Ge[011] and Ge(111) || Ni₂Ge(100). Back-gate field effect transistors (FETs) were also fabricated using this low resistivity Ni₂Ge as source/drain contacts. Electrical measurements show a good p-type FET behavior with an on/off ratio over 10³ and a one order of magnitude improvement in hole mobility from that of SFLS-synthesized Ge nanowire.

S Online supplementary data available from stacks.iop.org/Nano/21/505704/mmedia

(Some figures in this article are in colour only in the electronic version)

One-dimensional semiconductor material has attracted a great deal of attention for its unique electrical transport property, which shows promise for constructing many nanoscale devices, such as field effect transistors, logic units, memory devices and sensors [1–5]. Group IV materials are of particular interest due to their compatibility to the existing CMOS technologies [1–3]. For further device scaling and miniaturization, Ge nanowire, being complementary to silicon, has high mobilities, particularly for holes [1]. Moreover, many germanides, such as Mn_5Ge_3 and Ni_3Ge , exhibit ferromagnetism above room temperature [6, 7], and thus offer many advantages over silicides for future applications in spintronics. Particularly, nickel silicides and germanides were

evaluated to be the most favored contact materials in CMOS technology due to their low resistivity and good thermo-kinetic quality [8, 9]. Recently, intense work has been focused on the thermal diffusion of metal into Si nanowire to form nanowire heterostructures with a sharp interface between silicides and a silicon nanowire [10–15]. Likewise, metal–germanium nanowire is also drawing more and more interest [16]. Metal–germanium contacts, however, often have typical Schottky characteristics due to Fermi level pinning, which is claimed to originate from high density interface states due to native defects on the Ge surface [17, 18]. Therefore, a high-quality interface for the Ge contact is highly desirable to avoid the Fermi level pinning effect [18]. In this paper, we present well-controlled formation of Ni₂Ge/Ge/Ni₂Ge

⁴ Authors with equal contribution.

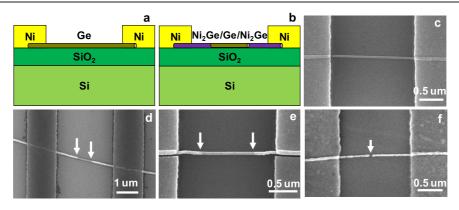


Figure 1. Formation of Ni₂Ge/Ge/Ni₂Ge heterostructure. Schematic illustration showing before (a) and after (b) the diffusion process of Ni into the Ge nanowire forming a Ni₂Ge/Ge/Ni₂Ge heterostructure. (c) SEM image of the Ge nanowire device with EBL defined Ni electrodes. (d) SEM image of the Ni₂Ge/Ge/Ni₂Ge heterostructure after 500 °C RTA for 60 s in which the length of the Ge region can be easily controlled to be less than 1 μ m. The arrows indicate the growth tips of the Ni₂Ge nanowire. (e) SEM image of the Ni₂Ge/Ge/Ni₂Ge heterostructure after 400 °C annealing for 40 s. The arrows indicate the growth tips of the Ni₂Ge nanowire. (f) SEM image of a broken nanowire after further annealing. The arrow highlights the broken region due to volume expansion.

heterostructure nanowires prepared in a wide temperature range with an atomically sharp interface. The process promises to minimize the Fermi level pinning effect. Furthermore, the heterostructure shows a good transition property.

Single-crystalline Ge nanowires were synthesized with a $\langle 111 \rangle$ growth direction by the SFLS process developed by Tuan et al, in which the Ge nanowire reaction was carried out in a 10 mL titanium-grade 2 reactor [19]. In short, the reactant solution composed of 0.1 M concentration in Ge moles and dodecanethiol-capped Au nanocrystals (Au/Ge molar ratio of 1:1000) in anhydrous toluene was prepared in a nitrogen-filled glovebox. After the titanium cell was heated to 420 °C and pressurized to 700 psi, the prepared reactant was removed from the glove box, injected into a 0.5 mL injection loop, and then injected into the reactor by a HPLC pump at a flow rate of 0.5 mL min⁻¹ until it reached a final pressure of 1300 psi. After the reaction (\sim 5 min), the reactor was cooled by submerging the it in a water bath for 2 min. The Ge nanowires collected from the reaction were then used for further device fabrication. Compared with the vapor-liquid-solid (VLS) method, the SFLS method provides better nanowire size control and higher product yields [20, 21], although the reported mobility of SFLS-synthesized Ge nanowires is lower. The typical diameter of as-synthesized Ge nanowires is around 40-50 nm and the length could be more than 10 μ m. As-synthesized Ge nanowires are undoped, however, unintentional doping usually exists [22, 23].

To obtain metal germanide/Ge nanowire heterostructures, Ge nanowires were transferred onto a SiO₂/Si substrate. The top thermal SiO₂ is about 300–330 nm thick. The Si substrate is heavily doped with a resistivity of 1– 5 m Ω cm which serves as a back-gate for further device characterization. Ge nanowires diluted in isopropyl alcohol (IPA) were dispersed on the substrate with the desired density. E-beam lithography (EBL) was used to define Ni electrodes on Ge nanowires. Before Ni e-beam evaporation (Ni 99.995% at less than 10⁻⁶ Torr), the sample was dipped into diluted hydrofluoric acid (HF) for 15 s to fully remove native oxide

in the contact region. Then the sample was annealed with rapid thermal annealing (RTA) in ambient N₂ to allow Ni thermal intrusion into the Ge nanowires and subsequent formation of Ni2Ge/Ge heterostructures along the nanowire. A field emission scanning electron microscope (JEOL JSM-6700 FESEM) was used to examine the morphology of the grown products. Figure 1 illustrates the formation of the Ni₂Ge/Ge/Ni₂Ge heterostructure. Schematics are shown in figure 1(a) before and (b) after the thermal diffusion process of Ni into the Ge nanowire. The SEM image of the device structure in figure 1(c) shows the uniform contrast of the Ge nanowire before RTA. Different annealing temperatures ranging from 400 to 700 °C were used to optimize the formation of nanowire heterostructures. It was found that the phase of the formed germanide nanowire depends on the annealing temperature, which was also observed in thin-film structures [24]. At 650 °C, Ni₃Ge was developed, which was claimed to be a ferromagnetic phase with a Curie temperature above room temperature (support information figure S1 available at stacks.iop.org/Nano/21/ 505704/mmedia) [6]. This ferromagnetic phase is favorable for spintronics applications [15, 25], such as spin injection into germanium. However, Ge nanowires are easily broken at high annealing temperatures (>550 °C) due to the significant reduction of the melting point for Ge nanowires [26]. When the temperature decreased to 400-500 °C, clear diffusion of Ni into the Ge nanowires was also observed and the formed germanide was identified to be Ni2Ge (refer to the TEM analysis later). After 500 °C RTA for 60 s, a clear contrast was observed between the Ge nanowire and the formed nickel germanide nanowire due to the conductivity difference Since the total growth length of Ni₂Ge is (figure 1(d)). about 1 μ m, the remaining Ge region can be easily controlled down to 650 nm. A similar contrast was also observed after 400 °C RTA for 40 s (figure 1(e)). The volume expansion and segregation of the nickel germanide were noticed at the same time (support information figure S2 available at stacks.iop.org/ Nano/21/505704/mmedia). It is noted that the nanowire could be broken after further annealing due to excessive Ni diffusion (figure 1(f)).

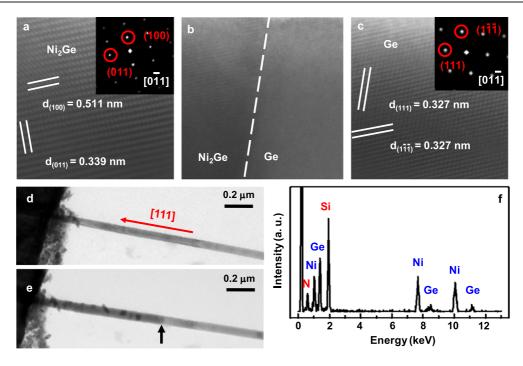


Figure 2. Epitaxial relationship at the Ni₂Ge/Ge interface. (a) Lattice-resolved TEM image of the formed Ni₂Ge nanowire. The inset shows the fast Fourier transform (FFT) pattern. (b) TEM image of the Ni₂Ge/Ge heterostructure. (c) Lattice-resolved TEM image of the unreacted Ge nanowire. The inset shows the FFT pattern. (d) Low magnification TEM image of the as-fabricated device with the Ni pad and the Ge nanowire. (e) Low magnification TEM image after annealing at 500 °C. The arrow indicates the interface of the Ni₂Ge/Ge nanowire. (f) EDAX spectrum of the Ni₂Ge, showing a relatively 2:1 concentration ratio of Ni and Ge atoms.

In order to identify the phase of the formed germanide and the epitaxial relationship of the germanide-germanium interface, in situ TEM was used to study the formation process and reaction kinetics. To prepare TEM samples, single-crystalline germanium nanowires were dispersed on TEM grids with a square opening of a Si₃N₄ thin film. The thickness of the Si₃N₄ film is about 30-50 nm thin in order to assure it is transparent to the electron beam without interference with images of the nanowires. EBL defined Ni pads were employed as the Ni diffusion source. A transmission electron microscope (JEOL-2010 TEM) attached to an energy dispersive spectrometer (EDS) was used to investigate the microstructures and to determine the compositions of the samples. To observe the reactions of the Ni electrodes with the Ge nanowires in situ, the samples were heated with a heating holder (Gatan 652 double tilt heating holder) in the TEM. Figures 2(a)–(c) show high-resolution TEM (HRTEM) images of the formed germanide-germanium interface after 500 °C annealing. According to the lattice-resolved HRTEM analysis, the formed germanide was identified to be singlecrystalline Ni2Ge with an orthorhombic lattice structure and lattice constants a = 0.511 nm, b = 0.383 nm, and c = 0.726 nm (space group 62). In figure 2(b), a clean and sharp interface between Ni2Ge/Ge was observed with an approximately 1 nm germanium oxide shell surrounding both the Ge and Ni₂Ge regions. The insets in figures 2(a)and (c) illustrate the fast Fourier transform (FFT) of Ni₂Ge and Ge HRTEM images, respectively. The crystallographic epitaxial relationships between Ge and Ni2Ge are shown to be: $Ge[011] \parallel Ni_2Ge[011]$ and $Ge(111) \parallel Ni_2Ge(100)$. Figures 3(d) and (e) show the low magnification TEM images of Ge NWs before and after annealing at 500 °C, respectively. Figure 3(f) shows the energy dispersive x-ray spectroscopy (EDAX) of the formed germanide nanowire region, showing that the ratio of Ni to Ge concentration is about 2:1, which further supports the fact that the formed germanide phase is Ni₂Ge. Signals of the Si and N peaks are contributed from the Si₃N₄ window. It is also noticed that a large strain exists at the Ni₂Ge–Ge interface (supporting information figure S3 available at stacks.iop.org/Nano/21/505704/mmedia), which offers an opportunity for engineering the bandgap and developing high-performance devices [27].

The real-time observation of Ni2Ge growth in the Ge nanowires was performed using in situ TEM video. This allows us to obtain lattice images of the epitaxial interface in progression and thus to estimate the growth velocity. Figure 3(a) shows the relation of Ni₂Ge nanowire length versus the reaction time at 400 and 500 °C illustrating a potentially linear growth behavior of Ni₂Ge in the Ge nanowires, while the detailed growth mechanism requires further study. Figures 3(b), (c) and (d), (e) show the in situ TEM images of Ni₂Ge nanowire growth at 400 and 500 °C, respectively. The growth length of the Ni₂Ge nanowire is 138.9 nm for 455 s at 400 °C and 357.5 nm for 340 s at 500 °C, respectively. Based on the data collected on more than three nanowires, the extracted growth velocities are about 0.31 nm s^{-1} and 1.05 nm s⁻¹ at 400 and 500 °C, respectively. Using the Arrhenius plot [11], the activation energy of the Ni_2Ge growth in the Ge nanowire is estimated to be 0.55 ± 0.05 eV/atom.

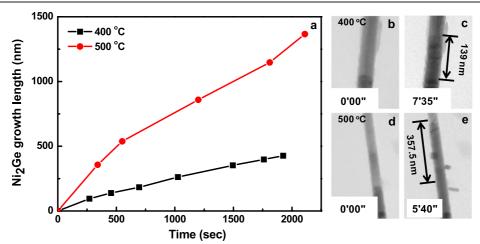


Figure 3. Kinetic analysis of the Ni₂Ge epitaxial growth within Ge nanowires. (a) Real-time record of the Ni₂Ge nanowire growth length versus the reaction time at 400 and 500 °C, illustrating a potentially linear growth rate. (b) and (c) *In situ*TEM images of the Ni₂Ge growth within a Ge nanowire at 400 °C. The arrow indicates a corresponding growth length of 138.9 nm in 7 min 35 s. (d) and (e) *In situ* TEM images of the Ni₂Ge growth within a Ge nanowire at 500 °C. The arrow indicates a corresponding growth length of 357.5 nm in 5 min 40 s.

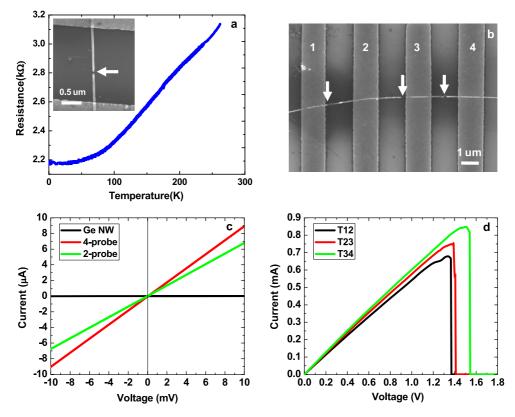


Figure 4. Electrical characterizations of Ni₂Ge nanowire. (a) Temperature dependent measurement of resistance for a fully germanided nanowire, showing a reduced resistance as the temperature decreases as the result of the formed metallic phase germanide. The inset shows a SEM image after electrical breakdown. The arrow points to the broken region. (b) SEM image of the Ni₂Ge nanowire after fully germanidation with four Ni pads for 4-probe measurement. The arrows indicate the broken region after electrical breakdown. (c) 4-probe and 2-probe *I*–*V* measurements of the formed Ni₂Ge nanowire compared with the Ge nanowire. (d) *I*–*V* recorded with a large applied bias voltage. The rapid drops indicate electrical breakdown at around 1.5 V corresponding to a breakdown current density above 3.5×10^7 A cm⁻².

To explore the electrical properties of the formed Ni₂Ge nanowires, the Ni thermal diffusion time was carefully controlled to fully convert Ge nanowires to Ni₂Ge nanowires. Figure 4(a) shows the temperature dependent I-V

measurement performed on a 2-probe Ni_2Ge nanowire. The inset of figure 4(a) shows a SEM image of the 2-probe Ni_2Ge nanowire after electrical breakdown. The measured resistance exhibits a metallic behavior, which monotonically decreases

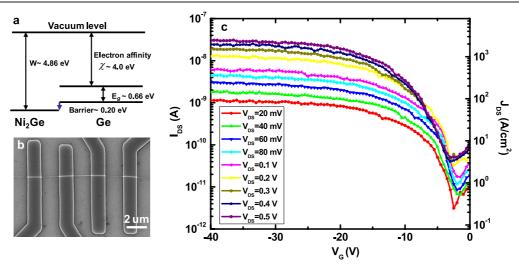


Figure 5. As-fabricated Ge nanowire field effect transistor at 300 K. (a) Energy band diagram showing that Ni₂Ge is an Ohmic contact to p-type Ge nanowire. (b) SEM image of the as-fabricated back-gate Ge nanowire transistor with four Ni electrodes defined by EBL. (c) $I_{ds}-V_{g}$ curves of the as-fabricated back-gate Ge nanowire transistor showing p-type MOSFET behavior.

from 3.14 k Ω at 262 K to 2.18 k Ω below 50 down to 1.54 K. This behavior verifies that the generated phase in the fully germanided nanowire is metallic [28]. In order to exclude the contribution from contact resistance when estimating the resistivity of the formed Ni2Ge nanowire, a 4-probe setup was performed (see figure 4(b)). In a standard 4-probe setup, a sweeping DC current was applied between two outer terminals (1 and 4) and the potential difference across two inner terminals (2 and 3) was recorded at the same time. Figure 4(c) shows the I-V characteristics of 4-probe and 2-probe measurements on a fully germanided nanowire compared with the partially germanided nanowire. The extracted resistance of a 1.6 μ m long Ni₂Ge nanowire is 1.48 k Ω and 1.12 k Ω from 2probe and 4-probe measurements, respectively, which gives a resistivity value of 88 $\mu\Omega$ cm at room temperature. Taking into account the volume expansion and diameter variation along the nanowire after germanidation, the resistivity of the formed Ni₂Ge nanowires is in the range of 88–137 $\mu\Omega$ cm. This value for a one-dimensional Ni2Ge nanowire is larger than previous reported values for single-crystalline Ni2Ge thin films (in the range of 20–50 $\mu\Omega$ cm) [29], which is similar to those of Ni₂Si nanowires and Cu₃Ge nanowires [16, 28]. To further explore the Ni2Ge nanowire as an interconnect material, it is desirable to characterize the maximum current density that it can conduct. Figure 4(d) records the I-V characteristics of three Ni₂Ge nanowires before and after electrical breakdown. The highest measured current that an individual Ni₂Ge nanowire of diameter 50 nm can carry is in the range of 0.68–0.85 mA, which gives a current density exceeding 3.5×10^7 A cm⁻². This value is comparable to that of the reported germanide and silicide nanowires, e.g., Cu₃Ge and PtSi [12, 16]. Figure 4(b) shows the SEM image of the measured three Ni₂Ge nanowires after electrical breakdown.

The formed atomically sharp interface in the Ni₂Ge/Ge/Ni₂Ge nanowire heterostructure can be used to explore promising applications in nanoscale devices. In the SEM studies of Ni diffusion into Ge nanowire, the remaining Ge

nanowire region can be easily controlled to be less than 1 μ m, which can be used as a channel for a Ge nanowire FET. Based on the estimated diffusion velocity, the Ge nanowire channel can be well controlled to sub-100 nm using an easily accessible RTA process. Clearly this process has great advantages over traditional photolithography technology. More importantly, the atomically sharp interface offers the opportunity to avoid the Fermi level pinning effect, which is commonly observed in metal-germanium contacts. Recently, Yamane et al, have demonstrated the epitaxial growth of high-quality Fe₃Si on Ge(111) with an atomically controlled interface, which successfully de-pinned the Fermi level of Fe₃Si/Ge contacts [18]. This result along with the reported work function of Ni₂Ge of 4.86 eV [30], which is 0.20 eV below the Ge valance band, suggests it can be used as an Ohmic contact to p-type germanium as shown in figure 5(a).

To study the electrical transport property of the Ni₂Ge/Ge/Ni₂Ge nanowire heterostructure, a back-gate field effect transistor has been fabricated on SiO₂/Si substrate. The Si substrate is degenerately doped to serve as a back-gate. A typical device structure with multiple Ni electrodes is showed in figure 5(b). Electrical measurements were performed using a home-made probe station connected to a Keithley 4200 semiconductor parameter analyzer. A typical $I_{\rm ds}-V_{\rm g}$ curve of the as-fabricated Ge nanowire FET without annealing is shown in figure 5(c). These FETs show typical p-type behavior in nature mainly due to the surface states induce hole accumulation rather than unintentional doping [22, 23]. The maximum current measured at $V_{\rm ds} = 0.5$ V is about 30 nA, corresponding to a current density of 2.4×10^3 A cm⁻². The current is relatively small due to a large Schottky barrier at the source/drain contacts before annealing. Using the cylinder-onplate model [31], the gate capacitance coupling between the Ge nanowire and the back-gate oxide is estimated to be

$$C_{\rm ox} = \frac{2\pi\varepsilon_{\rm ox}\varepsilon_0 L}{\cosh^{-1}(\frac{r+t_{\rm ox}}{r})}$$

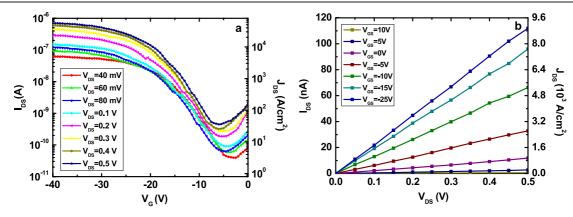


Figure 6. Electrical measurement of Ge nanowire FET after annealing. (a) $I_{ds}-V_g$ curves of the back-gate Ge nanowire transistor after 400 °C RTA for 15 s, forming a Ni₂Ge/Ge/Ni₂Ge heterostructure. The Ge nanowire channel length is 3 μ m. (b) $I_{ds}-V_{ds}$ curves of the back-gate Ge nanowire transistor after 400 °C RTA for 15 s.

where $\varepsilon_0 = 8.85 \times 10^{-14}$ F cm⁻¹ is the vacuum dielectric constant and $\varepsilon_{ox} = 3.9$ is the relative dielectric constant for SiO₂, r = 20 nm is the radius of the Ge nanowire, $L = 3 \mu m$ is the length of the Ge nanowire channel, and $t_{ox} = 330$ nm is the thickness of the back-gate dielectric. Then the estimated gate capacitance is $C_{ox} = 1.83 \times 10^{-16}$ F. The field effect hole mobility can be extracted from the $I_{ds}-V_g$ curves using the transconductance (g_m) at a fixed drain bias V_{ds} :

$$\mu = \frac{g_{\rm m}L^2}{V_{\rm ds}C_{\rm ox}}.$$

Using the maximum transconductance extracted from the $I_{ds}-V_g$ curves, the typical hole mobility is in the range of 3–8 cm² V s⁻¹. This is consistent with previously reported values (less than 10 cm² V s⁻¹) for SFLS-synthesized Ge nanowires [21].

After RTA at 400 °C for 15 s, however, electrical transport measurements on the device show much improved transistor characteristics. Figure 6(a) gives a logarithm plot of the drain current I_{ds} versus gate voltage V_g relations at various drain voltages. The gate bias was scanned from 0 V to -40 V, corresponding to a maximum vertical electrical field of $1.2 \times$ $10^3 \text{ V} \,\mu\text{m}^{-1}$. The $I_{\rm ds}$ - $V_{\rm g}$ curve shows p-type behavior with an on/off ratio larger than 10^3 . The maximum current measured at $V_{\rm ds} = 0.5$ V is about 0.7 μ A corresponding to a current density of 5.6×10^4 A cm⁻². The current has been increased more than one order after annealing and the formation of the Ni₂Ge/Ge/Ni₂Ge heterostructure after annealing is verified by SEM. The perfectly linear relationship between the drain current I_{ds} versus drain voltage V_{ds} in figure 6(b) implies good Ohmic contact between Ni2Ge and the Ge nanowire. The maximum transconductance extracted from the $I_{ds}-V_{g}$ curves at drain bias $V_{\rm ds} = 0.1$ V is 13.3 nS. Then the estimated hole mobility is about $65.2 \text{ cm}^2 \text{ V s}^{-1}$. Although this mobility is still lower than the reported value in VLS-grown Ge nanowires [16], it shows about a one order improvement among SFLS-synthesized Ge nanowires [21], which is believed to be attributed to the atomically sharp Ni2Ge contact to the Ge nanowire. In addition, when the gate capacitance was estimated using the cylinder-on-plate model, we assumed the Ge nanowires were completely embedded in the gate dielectric materials. However, in our back-gate transistor, the Ge nanowires are attached onto the SiO₂ surface instead of embedded in the SiO₂. So the calculated gate capacitance using this model is the upper limit. This factor could be taken into account by using an effective dielectric constant of 2.2 for SiO₂ within an analytical model [32], and then an effective hole mobility is estimated to be 116 cm² V s⁻¹ in our SFLS-synthesized nanowires, comparable with the hole mobility of VLS-grown Ge nanowires.

In summary, a Ni₂Ge/Ge/Ni₂Ge nanowire heterostructure with an atomically sharp interface has been formed by the thermal intrusion of Ni into a Ge nanowire at a wide temperature range of 400–500 °C. Both SEM and TEM studies show a well-controlled diffusion process with a diffusion velocity of 0.31 nm s⁻¹ at 400 °C and 1.05 nm s⁻¹ at 500 °C. The resistivity of the formed Ni₂Ge nanowire is extracted to be 88 μ Ω cm with a maximum current density of about 3.5 × 10⁷ A cm⁻². Back-gate field effect transistors were fabricated using the formed Ni₂Ge region as source/drain contacts to the Ge nanowire channel. The electrical measurement shows an on/off ratio over 10³ and a field effect hole mobility of about 65.4 cm² V s⁻¹, which are superior to the reported values from SFLS-synthesized Ge nanowires.

Acknowledgments

This work was supported by the Western Institution of Nanoelectronics (WIN) and National Science Council through grants no. NSC 98-2221-E-007-104-MY3 and NSC 99-2221-E-007-096.

References

- Wang D, Wang Q, Javey A, Tu R, Dai H, Kim H, McIntyre P C, Krishnamohan T and Saraswat K C 2003 *Appl. Phys. Lett.* 83 2432
- [2] van der Meulen M I, Petkov N, Morris M A, Kazakova O, Han X, Wang K L, Jacob A P and Holmes J D 2009 Nano Lett. 9 50
- [3] Huang Y, Duan X, Cui Y, Lauhon L J, Kim K-H and Lieber C M 2001 Science 294 1313

- [4] Thelander C, Nilsson H A, Jensen L E and Samuelson L 2005 Nano Lett. 5 635
- [5] Cui Y, Wei Q, Park H and Lieber C M 2001 Science 293 1289
- [6] Izumi T, Taniguchi M, Kumai S and Sato A 2004 Phil. Mag. 84 3883
- [7] Jamet M et al 2006 Nat. Mater. 5 653
- [8] Nemouchi F, Mangelinck D, Lábár J L, Putero M, Bergman C and Gas P 2006 Microelectron. Eng. 83 2101
- [9] Chen L J 2004 Silicide Technology for Integrated Circuits (London: The Institution of Electrical Engineers)
- [10] Weber W M *et al* 2006 *Nano Lett.* **6** 2660
- [11] Lu K-C, Wu W-W, Wu H-W, Tanner C M, Chang J P, Chen L J and Tu K N 2007 *Nano Lett.* **7** 2389
- [12] Lin Y-C, Lu K-C, Wu W-W, Bai J, Chen L J, Tu K N and Huang Y 2008 Nano Lett. 8 913
- [13] Hu Y, Xiang J, Liang G, Yan H and Lieber C M 2008 Nano Lett. 8 925
- [14] Chou Y-C, Wu W-W, Cheng S-L, Yoo B-Y, Myung N, Chen L J and Tu K N 2008 Nano Lett. 8 2194
- [15] Lin Y-C, Chen Y, Shailos A and Huang Y 2010 Nano Lett. 10 2281
- [16] Burchhart T, Lugstein A, Hyun Y J, Hochleitner G and Bertagnolli E 2009 Nano Lett. 9 3739
- [17] Zhou Y, Han W, Wang Y, Xiu F, Zou J, Kawakami R K and Wang K L 2010 Appl. Phys. Lett. 96 102103

- [18] Yamane K, Hamaya K, Ando Y, Enomoto Y, Yamamoto K, Sadoh T and Miyao M 2010 Appl. Phys. Lett. 96 162104
- [19] Tuan H-Y and Korgel B A 2008 Chem. Mater. 20 1239
- [20] Hanrath T and Korgel B A 2003 Adv. Mater. 15 437
- [21] Schricker A D, Joshi S V, Hanrath T, Banerjee S K and Korgel B A 2006 J. Phys. Chem. B 110 6816
- [22] Hanrath T and Korgel B A 2005 J. Phys. Chem. B 109 5518
- [23] Zhang S, Hemesath E R, Perea D E, Wijaya E, Lensch-Falk J L and Lauhon L J 2009 Nano Lett. 9 3268
- [24] Hsieh Y F, Chen L J, Marshall E D and Lau S S 1988 Thin Solid Films 162 287
- [25] Zwanenburg F A, van der Mast D W, Heersche H B, Kouwenhoven L P and Bakkers E P A M 2009 Nano Lett.
 9 2704
- [26] Wu Y and Yang P 2001 Adv. Mater. 13 520
- [27] Ieong M, Doris B, Kedzierski J, Rim K and Yang M 2004 Science 306 2057
- [28] Song Y, Schmitt A L and Jin S 2007 Nano Lett. 7 965
- [29] Dhar S, Som T and Kulkarni V N 1998 J. Appl. Phys. 83 2363
- [30] Zaima S, Nakatsuka O, Kondo H, Sakashita M, Sakai A and Ogawa M 2008 *Thin Solid Films* **517** 80
- [31] Ramo S, Whinnery J R and Duzer T V Fields and Waves in Communication Electronics 3rd edn (New York: Wiley) p 1994
- [32] Wunnicke O 2006 Appl. Phys. Lett. 89 083102