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Single-electron-based flexible multivalued logic gates

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Single-electron transistor (SET)-based multivalued (MV) not-AND (NAND) and not-OR (NOR) logic cells were implemented on a silicon-on-insulator chip. Depending on the ways of connecting two SETs with a field-effect transistor, the voltage transfer characteristics show typical NAND or NOR gate functions for various input voltages, which are binary, MV, and binary-MV mixed. Moreover, the switching functionality of our NAND (NOR) can convert to OR (AND) operation by simply adjusting their initial input voltages. These flexible two-input logic gates are expected to provide four basic arithmetic cells for the SET MV logic gate family. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2888164]

The basic philosophy of single electronics is a manipulation of one electron charge and how to apply it to the digital electronics.[1] The single-electron multivalued (MV) memory or MV logic reflects such capability of controlling the discrete charge of an individual electron. The MV memory can be implemented by utilizing the threshold quantization in nanoscale floating dot-based memory,[2] while multiple switching of a single-electron transistor (SET) enables us to realize the MV logic schemes,[3–6] which have higher functionality with lower hardware complexity. Degawa *et al.*[5] has recently proposed a SET MV logic gate family which are quite usable as a fast arithmetic circuit operation with a small number of device elements. Here, we report on an implementation of Si SET-based flexible MV not-AND (NAND) and not-OR (NOR) gates which play a crucial role as essential device elements for the SET MV logic gate family. Depending on the ways of connecting two SETs with a field-effect transistor (FET), its voltage transfer characteristics displays typical NAND or NOR gate functions for various two SET input voltages, which are binary, MV and binary-MV mixed mode.

Combining SETs with a FET, two-input NAND and NOR gates were fabricated on silicon-on-insulator chips. The resulting SET/FET circuit comprises of two identical SETs [connected in series (parallel) for the NAND (NOR)], a FET, and a constant-current (CC) load, which are seen in Figs. 1(a) and 1(b) with their corresponding circuit layouts. The FET connected in series with the combination of two SETs was to attain the SET bias voltage under a range of Coulomb blockade. In the SET part, a Coulomb channel and a side gate for each SET were both defined in the same plane of the top Si with 50 nm thickness, as seen in Fig. 2(a). The Coulomb channel of 15 nm width/50 nm length for each SET was first designed by electron-beam lithography and finally formed by pattern-dependent oxidation.[7,8] A selective doping on only the side gates was followed with a nanopatterned e-beam resist as a mask to prevent the active channel from being highly doped.[9] The Coulomb channel of our SET is thus a standard low-doped region, and is free from possible strong electrostatic fluctuations rising from the randomly distributed high dopants.

Figure 2(b) shows typical Coulomb oscillations for a SET element of the logic cells. Control of the phase of Coulomb current peaks of SET by using its side gate is seen in Fig. 2(c). Applying incremental side-gate voltage allows the phase of Coulomb peaks to shift, which enables to optimize the flexible multifunctionality of the devices. Drain current at 4.2 K, seen in Fig. 2(b), displays a large conductance peak value of $G_p \sim 3\ \mu S$ with a high peak-to-valley current ratio. This large current leads to $R_j \sim 1/2G_p \sim 166\ k\Omega$, for the junction resistance, which is within an order of magnitude of the theoretical quantum limit for displaying a clear Coulomb blockade. Typical value of the gate capacitance C_g is deduced from the Coulomb peak spacing ΔV_g using the relationship $C_g = e/\Delta V_g$, which yields $C_g \sim 2.1$ aF. By using the tunnel junction capacitance $C_j \sim 0.6$ aF directly deduced from a measured charge stability diagram [an inset in the Fig. 2(b)], we can estimate the intrinsic speed of the SET, which is $\sim R_j C_t = 166\ k\Omega \times 3.3$ aF ~ 0.6 ps, yielding to ~ 1.7 THz speed, where C_t is the total capacitance of $C_g + 2C_j$. This high RC value was also evaluated in our previous SETs with similar geometry.[8] Note that this ultrafast intrinsic speed of the SET element is not the directly measured operating speed of its logic circuits. The actual operating frequency becomes far reduced mainly by the RC_L cutoff due to inevitable capacitance loading the SET output.

Figure 3 shows the data of the NOR gate; gray scale contour plot of the voltage output V_{out} measured at 4.2 K versus two SET input voltages of V_{in_1} and V_{in_2} and its voltage swing waveforms. The CC load current is set to 100 pA by a current-mode output of HP4155 with a compliance (voltage limit) of 30 mV, and the V_{gg} of the FET is set to 1.670 V. As seen in Fig. 3(a), V_{out} displays a periodic high/low mosaic pattern as a function of two SET input voltages, corresponding to Coulomb-blockaded/tunneling current regimes; high for both SETs blockaded, while low for one or both SETs tunneled through. The voltage transfer characteristics are seen in Figs. 3(b)–3(d). The offset zero values of V_{in_1} and V_{in_2} for each mode can be selected from an operating point (low, low) in any periodic regions of the contour plot of V_{out}, for an instance, as seen by dot-lined areas in Fig. 3(a). The voltage transfer characteristics for NOR gate is seen in Fig. 3(b), for which the two-input voltages, V_{in_1} and V_{in_2}, were switched between the two points corresponding to 0 (low) and 1 (high), as shown in Fig. 3(a) with circles. Note

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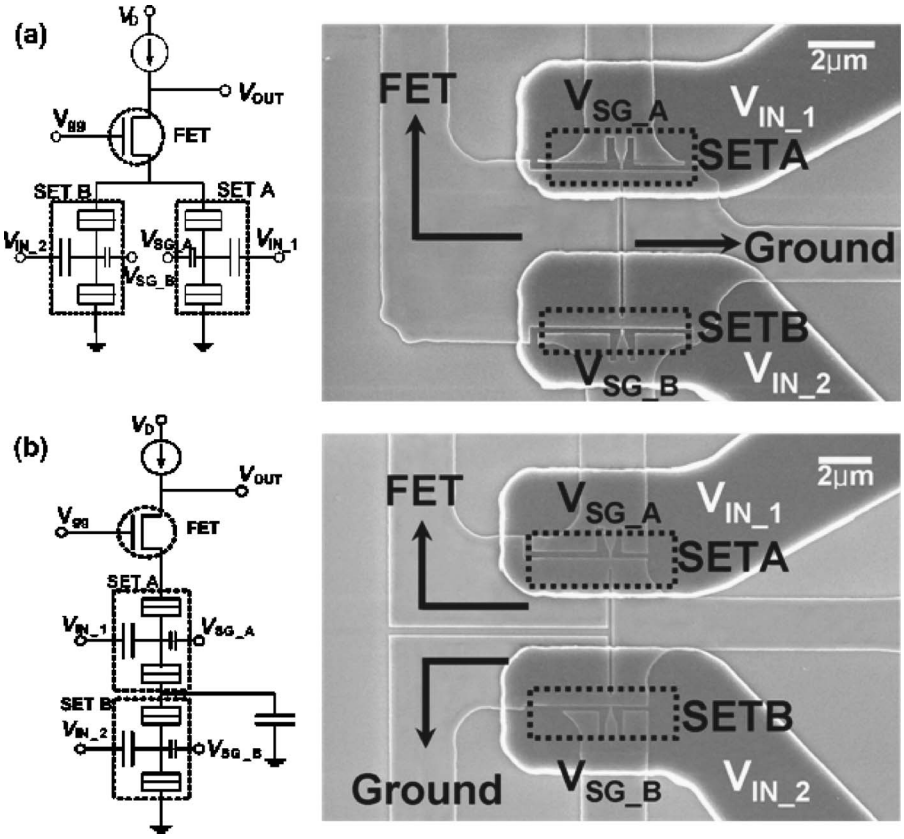

FIG. 1. Schematics and scanning electron micrograph (SEM) images of the SET/FET hybrid circuits, each comprising of a FET with CC and two identical SETs which are connected in parallel for (a) NOR and in series for (b) NAND gate, respectively.

that the NOR function can be switched to AND function by simply shifting two initial SET input voltages down to one-step lower levels, as seen by points with squares in Fig. 3(a). Its voltage swing waveform is seen in Fig. 3(c). For the multilevel logic functionality, Fig. 3(d) shows the voltage transfer characteristics for a 2×3 binary-MV mixed mode, for which $V_{\text{in\_1}}$ was switched between the two values (0 and 1; binary input) and the other input voltage of $V_{\text{in\_2}}$ was switched among the three values (0, 1, and 2; MV input). They were selected from operating points with triangles, as shown in Fig. 3(a). It is noted that the circuit always produces binary outputs even for MV inputs. For MV output signal, we need to employ the additional components such as inverting adder or latched quantizer.[5] The number of multilevels was observed to decrease with increasing CC load. For

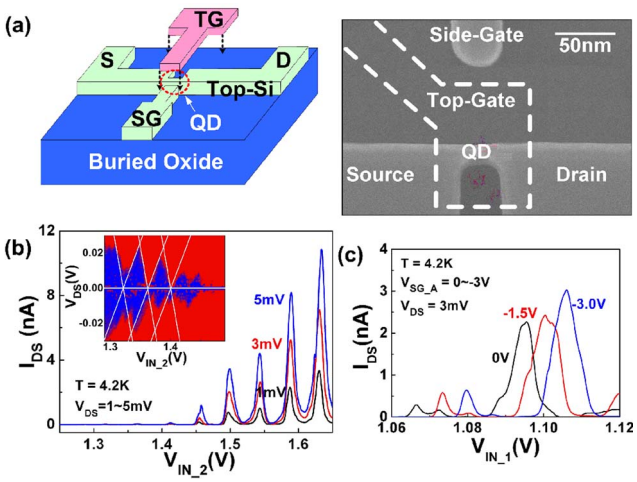

FIG. 2. (Color online) (a) Schematic and SEM image of the SET element. (b) Coulomb oscillations of the SET for NOR gate measured at 4.2 K. Its charge stability diagram is shown in the inset. (c) Control of the phase of Coulomb current peaks by a side-gate voltage attached to each SET element of NAND gate.

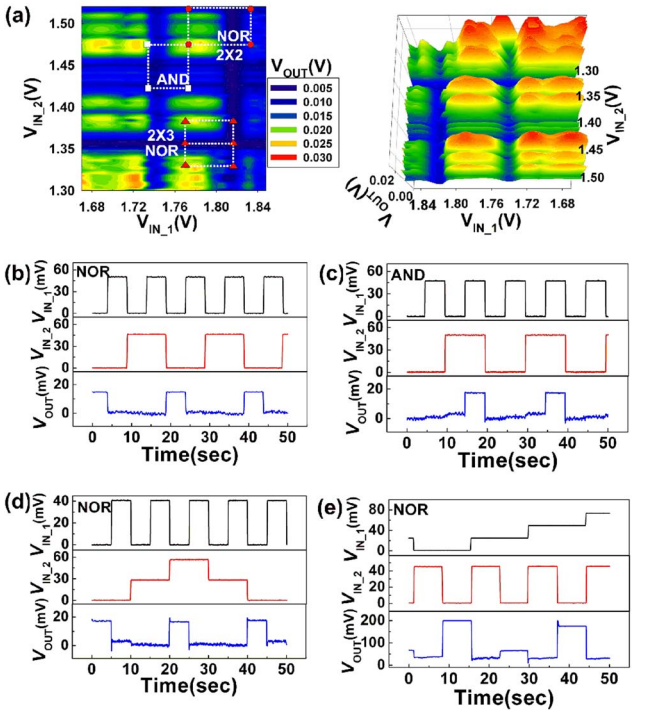

FIG. 3. (Color online) (a) Gray scale contour and three-dimensional plot of the V_{out} vs two SET input voltages of $V_{\text{in\_1}}$ and $V_{\text{in\_2}}$. [(b) and (c)] The voltage transfer characteristics of NOR and AND functions for a 2×2 binary input modes. (d) The voltage transfer characteristics of NOR function for a 2×3 binary-MV mixed mode. (e) Reducing the current leakage in the FET by using a postannealing instead of rapid thermal annealing resulted in increasing the output of the NOR gate up to ~200 mV for a 2×4 binary-MV mixed mode.

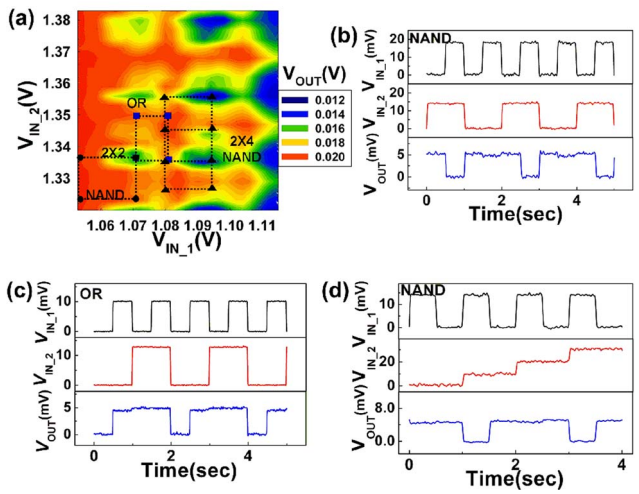

FIG. 4. (Color online) (a) Gray scale contour plot of the V_{out} vs two SET input voltages of V_{in_1} and V_{in_2}. [(b) and (c)] The voltage transfer characteristics of NAND and OR functions for a 2×2 binary input modes. (d) The voltage transfer characteristics of NAND function for a 2×4 binary-MV mixed mode.

a CC load of 100 pA, we could exploit 4 Coulomb oscillations, resulting in eight multilevel functionality. The CC load could be increased up to 5 nA, for which 2 Coulomb oscillations could be used to yield four MV levels.

Figure 4(a) is gray scale contour plot of the voltage output for NAND gates. The CC load is set to 100 pA with a voltage limit of 20 mV and the V_{gg} of FET is set to 841 mV. Similar to the NOR gate, the V_{out} displays a periodic high/low pattern versus two SET input voltages. The voltage transfer characteristics are seen in Fig. 4(b) for 2×2 binary inputs and in Fig. 4(d) for 2×4 binary-MV mixed mode. They were taken from operating points with circles and triangles, respectively, as shown in Fig. 4(a). Similar to NOR-to-AND conversion, the NAND function can be converted into OR by shifting two SET input voltages up to one-step higher levels, as seen by points with squares in Fig. 4(a). Its voltage swing waveform is seen in Fig. 4(c). Tuning ranges of the input voltages for the mode conversions (~40 mV for NOR/AND and ~20 mV for NAND/OR for our devices) can be further increased for the stability of operation. Since the input level spacing corresponds to the Coulomb oscillation period, it can be increased by reducing the topgate-Coulomb channel capacitance. We have actually made an enhancement in the tuning range of the input up to ~360 mV by increasing the Coulomb oscillation period of the SET with a reduced gate capacitance C_g=0.44 aF. It is also noted that the output voltages (~30 mV for NOR and ~10 mV for NAND) are very low. Such a low value of output is mainly due to a leakage in the FET part. By using the postannealing, we have reduced the current leakage in the FET and obtained a threshold with better sharpness, resulting in the output of the NOR gate increased up to ~200 mV, as seen in Fig. 3(e), for a 2×4 binary-MV mixed mode.

As seen in the above data of NAND and NOR gates, the MV logics implemented by SETs are thus very flexible and effective since they fully utilize the periodic mosaic patterns of the output resulting from the multiple switching on/off, which is a unique inherent feature of the SET and is quite different from the single threshold or single negative differential resistance peak in the traditional complimentary metal-oxide semiconductor and resonant tunneling transistor.

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