Single Event Effects in Static and Dynamic Registers in a 0.25μm CMOS Technology

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Abstract

We have studied Single Event Effects in static and dynamic registers designed in a quarter micron CMOS process. In our design, we systematically used guardrings and enclosed (edgeless) transistor geometry to improve the total dose tolerance. This design technique improved both the SEL and SEU sensitivity of the circuits. Using SPICE simulations, the measured smooth transition of the cross-section curve between LET threshold and saturation has been traced to the presence of four different upset modes, each corresponding to a different critical charge and sensitive area. A new architecture to protect the content of storage cells has been developed, and a threshold LET around 89 MeVcm^{2}mg^{-1} has been measured for this cell at a power supply voltage of 2 V.

I. INTRODUCTION

The High Energy Physics (HEP) community is working on the construction of a new p-p collider to extend to higher energy the exploration of the ultimate structure of matter. The LHC (Large Hadron Collider), will be built in an already existing underground tunnel at CERN, Geneva, Switzerland. Four experiments, situated along the tunnel at the location of the beam crossings, will observe the collisions and study the fundamental physics. Due to the high energy and luminosity of the colliding beams, different parts of each experiment (detectors, electronics, mechanics and infra-structures) will be exposed to a radiation environment whose particle energy and composition widely varies with the position and surrounding materials [1]. Therefore, the HEP community needs a relatively large amount of radiation tolerant/hard electronics, a considerable part of which will be custom developed ASICs.

In an attempt to reduce the costs and improve the circuit performance, the possibility of using a deep submicron commercial technology for ASIC design is under investigation. Such an approach is based on the increased radiation tolerance of the gate oxide which accompanies the shrinking of CMOS processes. As the gate oxide becomes thinner, both the charge trapping in the oxide and the interface state creation decrease, eventually becoming negligible below about $t_{ox} = 6$ nm [2]. The systematic use of enclosed NMOS transistor topology (edgeless devices) and guardrings prevents any radiation-induced leakage current under the still thick isolation oxide [3]. Total dose tolerance complying with the LHC requirements has been achieved using this technique [4, 5].

On the other hand, deep submicron technologies are generally more sensitive to Single Event Upset (SEU) than older technologies [6]. In LHC the presence of heavy ions will be limited to the beam pipe, and the radiation environment for the electronics will be dominated by charged hadrons and neutrons. Nevertheless, enough energy to trigger Single Event Effects (SEE) can be deposited by recoils from the nuclear interaction of incoming charged hadrons and neutrons with target nuclei in the integrated circuit itself, or in its close surroundings. The sensitivity to SEEs of circuits designed using edgeless devices and guardrings needs therefore to be measured, and the results should be translated into expected upset and latchup rates in the LHC environment.

The objectives of the work described hereafter are twofold: to evaluate the SEE sensitivity of ASICs developed in deep submicron processes using enclosed transistor topologies and guardrings, and to develop countermeasures to lower or eliminate the risk associated with SEEs.

II. EXPERIMENTAL DETAILS

For this study, we have designed dedicated test structures in a 0.25 μm CMOS technology using enclosed NMOS transistors and guardrings systematically. The choice of a quarter micron process was driven by the present wide availability of commercial processes of such generation.

A. Test Structures

The simple circuit we have chosen for our test is the shift register. This choice was driven both by the simplicity and the universality of the shift register. This circuit is easy to design and requires a minimum of input signals for its operation. This translates into a small number of pads, hence the opportunity to integrate several circuits close to each other in a small area and mount them in the same package. These circuits can then be tested simultaneously, saving beam time. The basic element of the shift register, the Flip-Flop, is widely used in digital and mixed-mode ASICs for LHC, both in synchronous clocked operation and in control registers.

We have designed three shift registers, each composed of a number of identical Flip-Flop cells (DFF), differing from each other in the architecture of the basic DFF cell. For the first DFF, we used a standard static architecture, whilst for the second a dynamic architecture was chosen. The schematic of these two cells is shown in Figure 1. There is a substantial difference in the SEU sensitivity for the two architectures. In the static cell, data is stored in loops composed of

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cross-coupled inverters. Therefore, each storage node has a low resistance path to either Vdd or ground, through which charges deposited by an ionizing particle can be evacuated. On the other hand, in the dynamic cell several nodes store data in a high impedance state during different phases of the clock cycle. The charge deposited by an ionizing particle can therefore easily accumulate and induce a SEU. Besides these two traditional schemes, we have developed a new DFF architecture hardened against SEU, to which we will refer hereafter as "hardened" cell. This cell will be described in section III.

The layout of the three cells is shown in Figure 2, where the enclosed topology used for all NMOS transistors is observable. Some of the PMOS transistors have been also integrated as enclosed devices to match the size of the NMOS in the x-direction, saving some space in the y-direction. Compared to the static architecture, the dynamic one is almost a factor of 2 smaller, leading therefore to a higher integration density. The three cells have been designed with a height of 16 μm, and their length is 18, 33 and 50 μm respectively for the dynamic, static and "hardened" cell.

The static and "hardened" registers are composed of 2048 DFF cells, whilst for the dynamic we integrated 1024 cells. In total, some 150000 transistors were used for a total active area of about 2.7 mm^2.

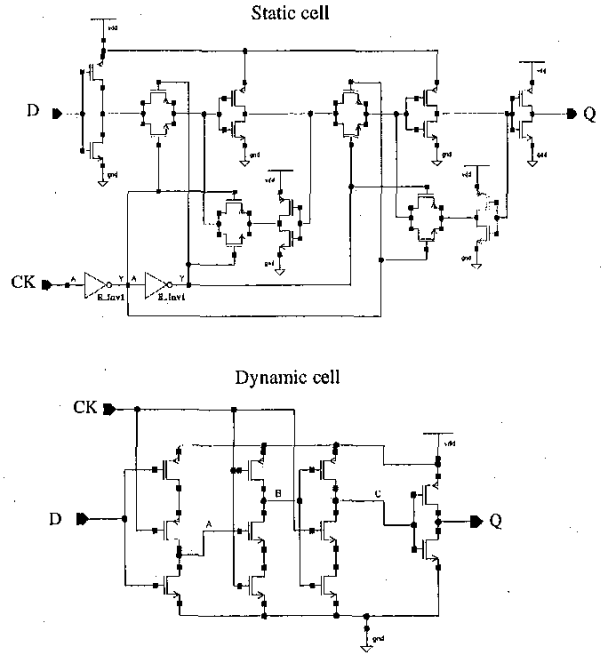

Figure 1: Schematic of the static and dynamic DFF cells.

B. Irradiation procedure

The SEE experiment took place at the Lawrence Berkeley National Laboratories (LBNL) 88-Inch Cyclotron, adjusting the Linear Energy Transfer (LET) of the incoming ions between 3.2 and 89 $MeVcm^2mg^{-1}$. The irradiation was performed at room temperature, and two test modes were used: un-clocked and clocked. In the un-clocked mode, the data pattern is streamed into the shift register by applying a train of clock pulses, stored without clock for an adjustable time span, then streamed out for comparison. The dynamic register could not be tested this way as it needs a continuous clock. In the clocked mode, the clock is constantly applied: data streams in and out all the time and are constantly compared for error detection. This also corresponds to the storage mode for the dynamic register. All the following results refer, unless otherwise specified, to a data pattern composed of an alternate 1-0 sequence.

During the irradiation, the current consumption of the circuits was constantly monitored to detect the occurrence of latchup. The supply voltage was generally kept at 2 V during the SEU measurements, but raised to the technology nominal voltage of 2.5 V to look for increased SEL sensitivity at higher voltage.

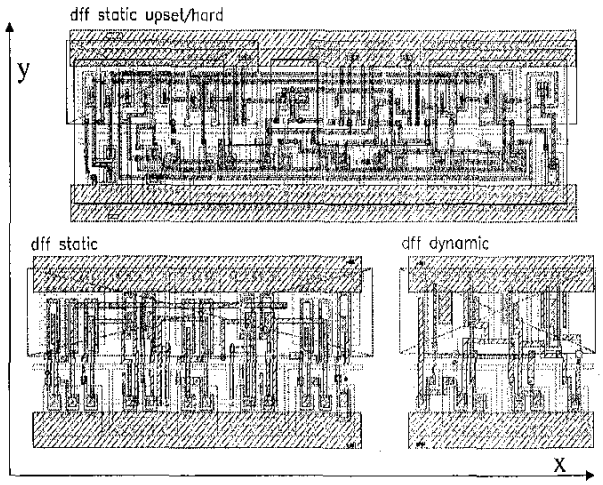

Figure 2: Layout view of the three DFF cells.

III. The Hardened DFF Cell

The proposed "hardened" DFF cell is derived from previously developed solutions to protect the content of storage cells against SEU [7], [8]. As its predecessors, it follows the approach of logic redundancy, and it is aimed at further reducing implementation costs in terms of area, speed and power consumption.

In the edge-triggered master-slave flip-flops typical of synchronous sequential circuits, SEU immunity must be ensured for both the master and the slave latch. This is necessary even though their time-related sensitivity ratio may be highly asymmetric, since actually the master latch only stores the data during the active clock phase. This observation led us to the idea of implementing upset-immune flip-flops with dynamic-static operation, where a dynamic configuration is used for the master latch section. This section

can be implemented either as a distinct element or, as in the case of our cell, using one of the existing nodes in a dual feedback four-node storage loop latch.

The architecture of the "hardened" DFF is shown in Figure 3. The dual feedback in the slave section is integrated through split clocked inverter gates (SCI1 and SCI2). During the storage phase (clock inactive) this feedback ensures that the perturbation induced on a single node by a particle hit does not propagate further into the latch, and the initial condition is quickly restored. As a consequence of such SEU-hardened architecture, data have to be written simultaneously in two nodes to be latched into the slave. This has been implemented using a sequential access to nodes X1 and X2, controlled by two clocks: a master precharge clock (CK1) and a slave transfer clock (CK2). The slave clock can be easily generated from the master by introducing a delay sufficient to allow the data writing in X2 (about 200 ps in our case).

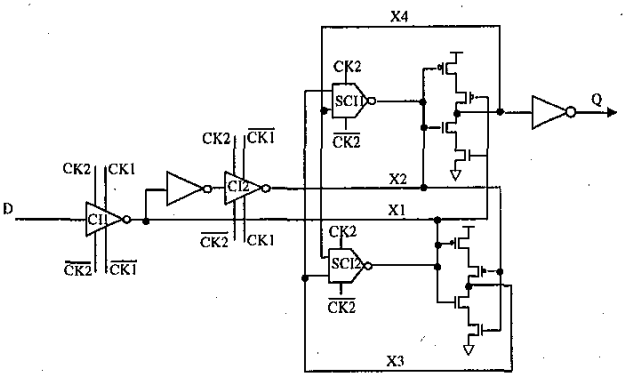

Figure 3: Schematic of the "hardened" dynamic-static DFF. CI = Clocked Inverter, SCI = Split Clocked Inverter.

The dynamic master section precharges the input data at node X1, through the clocked inverter CI1, when both CK1 and CK2 are active. Data precharged at X1 is subsequently transferred and latched into the slave through CI2 only when CK1 is low and CK2 is high, as shown in Figure 4.

The fast access timing of this flip-flop allows reliable operation with narrow clock pulses that satisfy the minimum data input setup and hold time requirements. This in turn reduces the SEU vulnerability time interval of the master latch section. The need for two clocks for the write cycle also protects the contents of the DFF against hits on one of the clock buffers.

Finally, to avoid the possibility that charges deposited by a single highly ionizing particle could simultaneously corrupt the state of two nodes in the slave section, the layout of the DFF has been carefully studied. The chosen layout provides adequate spacing and isolation of transistor drains connected to pairs of sensitive nodes (as X1 and X2). This is simple to implement using transistors with edgeless topologies when the drain is the central diffusion, hence being completely surrounded by the gate and source. The resulting DFF cell has an area overhead of only 50% with respect to its standard static counterpart.

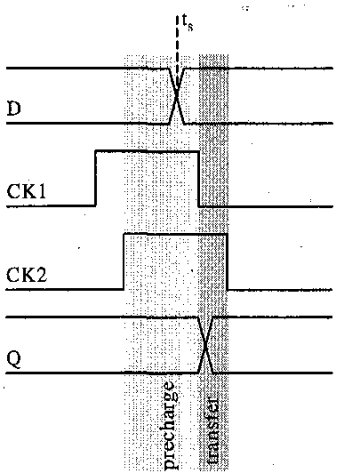

Figure 4: Time diagram of the write cycle in the "hardened" DFF. The active edge of the clock is the falling edge of CK1. t_s is the setup time of the DFF.

IV. Results and Discussion

A. *Single Event Latchup*

No SEL has been observed during the whole irradiation test, up to the maximum LET of 89 MeVcm^{2}mg^{-1}. This result was expected, as SEL sensitivity has been shown to decrease in modern deep submicron CMOS processes [9] due to the reduced thickness of the epitaxial layer, the presence of retrograde wells and the use of Shallow Trench Isolation (STI). Moreover, device simulation has pointed out the effectiveness of guardrings in substantially decreasing the SEL susceptibility [10]. As the design practice we follow requires the systematic use of guardrings to obtain total dose tolerance, at the same time it increases the circuit robustness against latchup. This layout practice assures a low resistance path to V_{ss} in any point of the circuit.

B. *SEU in un-clocked operation mode*

1) Static shift register

The measured cross-section curve is shown in Figure 5 for the static shift register, normalized to one cell (cm^2/bit). The measured points for the static register are fitted by a Weibull curve, and the parameters of the fit are indicated in Figure 5. The threshold LET (LET$_{th}$) is just below 15 MeVcm^{2}mg^{-1}, a high value for a 0.25 µm technology. This can be explained by the use of enclosed transistor geometry in the DFF cell. The minimum gate width of an enclosed transistor is imposed by the minimum size of the central diffusion (drain), which has to be completely surrounded by the gate. In our design, we have chosen the minimum gate length and the minimum drain diffusion size for all NMOS transistors, obtaining a

channel width of about 3.3 μm. Also the PMOS transistors are considerably bigger than the minimum achievable size to match the drive capability of the NMOS. As a result, both the node capacitance (proportional to the gate area) and the current drive of the transistors (proportional to the aspect ratio W/L) are higher than for the use of minimum size transistors. This translates into higher critical charge for upset, which explains the result of our measurement.

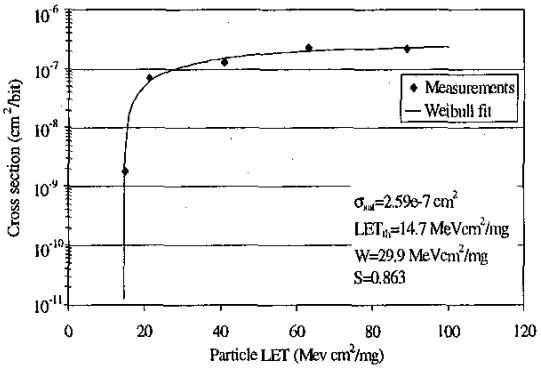

Figure 5: Measured cross-section curve for the static DFF cell. A Weibull curve fits the measured points.

To gain some insight into the measured upset curve, we have used a SPICE simulator to estimate the critical charge of the static DFF cell. The simulation has been performed using the typical set of parameters given by the CMOS manufacturer. DC measurements of single transistors from the same wafer are consistent with the used parameters. The charge injection from an ionizing particle was simulated with a pulsed current generator with linear rise and fall times of 50 and 100 ps respectively. The injection took place at the two sensitive nodes of the slave part of the DFF, named A and B in Figure 6. In the absence of the clock, data are stored into these nodes.

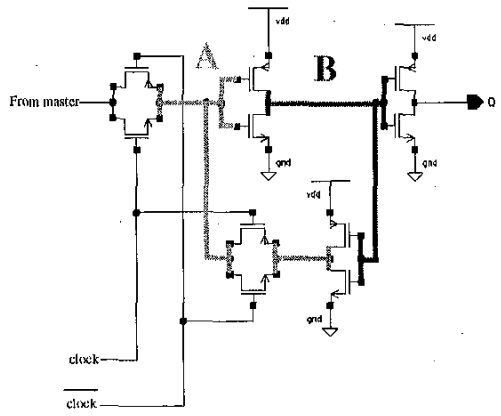

Figure 6: The simulation of the charge injection from an ionizing particle took place on nodes A and B of the slave part of the static DFF.

Table1: Critical charge from SPICE simulations for hits on nodes A and B. The transition refers to the output of the cell, and SA stands for Sensitive Area as measured from the cell layout.

	Transition 0->1		Transition 1->0		Total SA
	Q_{crit} (fC)	SA(μm²)	Q_{crit} (fC)	SA(μm²)	(μm²)
Hit on B	225	0.7	255	2.1	2.8
Hit on A	170	5.6	180	11.7	17.3

The critical charge computed from the SPICE simulation is reported in Table1, which also indicates the sensitive area SA (or cross-section) of the cell estimated from the layout for hits in both A and B and for 0->1 and 1->0 transitions. In the estimate from the layout, the sensitive area has been taken as the drain diffusion area of the inverter transistors and the source and drain diffusion areas of the switches.

The cell has actually four different critical charges, two for each sensitive node, each corresponding to a different particle hit. The simulation results can be used to reconstruct a curve for the evolution of the sensitive area (or cross-section) as a function of the charge collected from the particle hit. This curve is shown in Figure 7. To be able to plot the results of our measurements in the same chart, we need to translate the LET of the heavy ions used in the experiment into collected charge at the sensitive node. This requires an estimate for the sensitive depth, that is the limit beyond which the charge deposited by the ion does not contribute to the upset mechanism (either is not collected at the node or is collected too late to contribute). Though there is no consensus on this number, we have chosen a sensitive depth of 1 μm, as recently proposed for a 0.6 μm process [11]. In that case, the sensitive depth was estimated with 3-D simulations and confirmed by the experiments. Our assumption for the sensitive depth does not in anyway affect the shape of the cross-section curve.

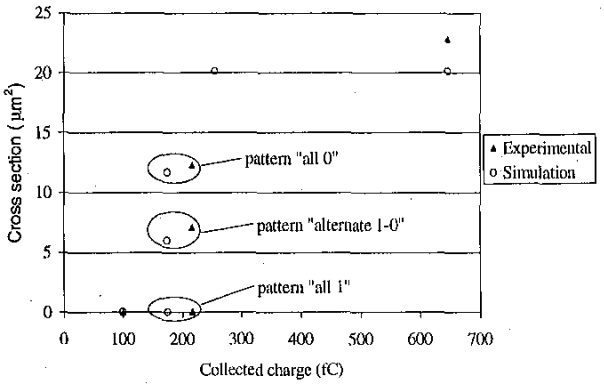

Figure 7: Cross-section as a function of the charge collected at the sensitive node. Measurements are compared with the estimate from the SPICE simulation and the knowledge of the cell layout.

The simulation and measured points are slightly shifted, which might indicate that the estimate for the sensitive depth is not precise, but the overall behaviour is well in agreement. This result indicates that the smooth transition of the cross-section curve between threshold LET and saturation is determined by the consecutive opening of different upset modes. With the gradual increase of the particle LET, hence of the deposited charge, more and more upset modes become accessible: hit on A for a transition 0→1, then also for a transition 1→0, then also strike on B for a transition 0→1 until eventually the whole area of nodes A and B becomes sensitive. Moreover, in our case the measured values depend on the data pattern stored into the register.

2) "Hardened" shift register

The measured cross-section curve for the "hardened" shift register is shown in Figure 8, normalized to one cell (cm^2/bit).

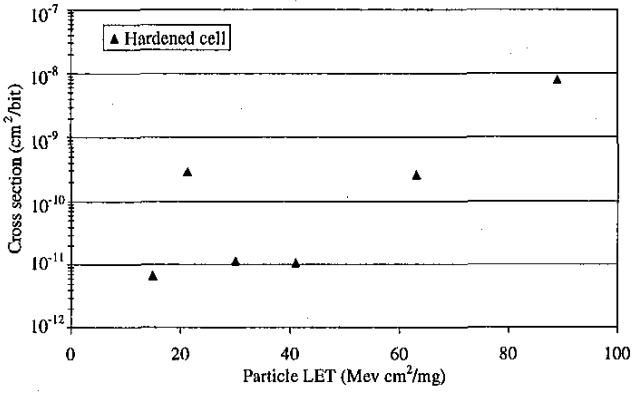

Figure 8: Measured cross-section for the "Hardened" cell.

The cross-section for all the points except the one at higher LET is actually determined by the maximum fluence reached in the experiment, and should therefore generally be considered as an upper limit. In most cases, the number of errors was zero, but sometimes one error was found. We found that the error occurrence was not proportional to the fluence, rather on the number of read and write cycles during the test. We have therefore concluded that these rare errors did not correspond to SEU during storage, but during the read/write cycles, when the clock was applied. This conclusion is strongly supported by the measurements in clocked mode discussed in subsection C.

At the maximum available LET of 89 MeVcm^{2}mg^{-1}, the "hardened" shift register began to experience SEU during data storage. The measured cross-section was still below 10^{-8} cm^2/bit, proving that the threshold LET is close to 89 MeVcm^{2}mg^{-1}. This very high value is a significant result for a design in a quarter micron process biased at only 2 V, and confirms the effectiveness of the proposed design to prevent SEU in storage cells.

C. SEU in clocked operation mode

Due to the limited beam time available, only the dynamic and "hardened" shift registers could be tested in the clocked operation mode, and it was not possible in any case to draw the complete cross-section curve.

The clocked operation test was performed at the frequency of 2.5 MHz, which is far from the maximum working frequency of the registers. This choice was imposed by the limited speed capability of the test board, which could not reliably transmit the clock and data to the shift registers chip at higher frequency.

1) Dynamic shift register

During the test of the dynamic shift register, SEUs were detected already for a LET of 3.2 MeVcm^{2}mg^{-1}, the minimum used during our irradiation run. From this value, and again assuming a sensitive depth of about 1 μm, one can deduce a critical charge lower than 35 fC. Increasing the LET to 5.6 and then to 15 MeVcm^{2}mg^{-1} does not significantly affect the measured cross-section, which stays around 10^{-7} cm^2 (for one DFF cell).

The analysis of the SEU event using SPICE is much less straightforward for the dynamic cell, as this cell has three different sensitive nodes, and their sensitivity changes when the clock and data are high or low. To get an idea of the critical charge, we have simulated a particle hit in node C (Figure 1), with the clock low, so that node C is either floating or connected to V_{dd} according to the state of node B. In the most sensitive case (B low), the critical charge was about 34 fC.

Both the SPICE simulation and the experiment point out the high sensitivity to SEU of this dynamic architecture, which makes it unattractive for ASICs design to be used in a radiation environment. Even in the LHC environment, this cell would experience a high rate of upsets. In that case, enough energy to induce SEU can be deposited by the recoils from nuclear interaction of the charged hadrons and neutrons in the silicon of the IC or in the surrounding materials.

2) "Hardened" shift register

In the case of the "hardened" shift register tested in the clocked operation mode, upsets were detected starting from a LET of 5.6 MeVcm^{2}mg^{-1}. In that case the cross-section was very low (about 8 10^{-10} cm^2), but increased by 2 orders of magnitude when a LET of 15 MeVcm^{2}mg^{-1} was used.

The upset mechanism has been identified clearly with SPICE simulations, and is related to the use of the DFF cell as an element of a shift register. During the write cycle, when the slave clock (CK2) is high, node X2 (see Figure 3) is in a high impedance state. If hit by an ionizing particle during this period, this node can easily change its logic state. This change of state is only temporary, as the correct output value is recovered at the end of the write cycle, but happens during the write cycle of the next DFF cell. Therefore, in the specific

case of the shift register, the wrong data is latched into the next DFF and generates an upset.

To eliminate this upset mode, and render the "hardened" cell adapted also to synchronous clocked operation, it is possible to replace the clocked inverters with the combination of pass gates and clocked multiplexers. The resulting modified DFF cell is currently being integrated in the same submicron technology, and the characterization of its performance will be the object of a future work.

V. Conclusion

We have studied SEE in static and dynamic cells designed in a quarter micron CMOS process using edgeless transistors and guardrings systematically. This design technique, aimed at increasing the total dose tolerance of the design, has some beneficial effects on both SEL and SEU sensitivity.

The presence of guardrings increases the robustness to SEL, and no latchup has been observed during the irradiation tests performed up to a maximum LET of 89 $MeVcm^2mg^{-1}$. Moreover, the particular shape of edgeless transistors poses a limit on the minimum achievable gate width, which translates into higher node capacitance and current drive. The combined effect of these two characteristics increases the critical charge for upset. For a static DFF cell designed this way, we have measured a threshold LET of about 15 $MeVcm^2mg^{-1}$, which is quite high for a 0.25 μm technology.

The study of the SEU mechanism on the static DFF cell, performed with the help of a SPICE simulator, has revealed the origin of the measured smooth transition of the cross-section curve between threshold and saturation. This transition is determined by the presence of four different upset modes, each having a different critical charge and corresponding to a different sensitive area. As the particle LET is increased, more and more upset modes becomes active, and the measured cross-section increases.

To effectively protect the contents of storage cells from data corruption, we have developed a new architecture for data storage, based on a dynamic-static flip-flop. A DFF integrated using this architecture had an area penalty of about 50% with respect to a static standard architecture. We measured a threshold LET close to 89 $MeVcm^2mg^{-1}$ for this cell at a power supply of 2 V, which is a very high value for a design in a quarter micron technology.

Acknowledgments

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References

[1] CMS, The Tracker Project Technical Design Report, CERN/LHCC 98-6, CMS TDR 5, 18 March 1998.

[2] N.S. Saks, M.G. Ancona, J.A. Modolo, "Generation of Interface States by Ionizing Radiation in Very Thin MOS Oxides", IEEE Trans. Nucl. Science, Vol.33, p.1185, December 1986.

[3] D.R. Alexander, "Design Issues for Radiation Tolerant Microcircuits for Space", Short Course presented at the 1996 NSREC conference, Indian Wells, Ca, July 15-19, 1996.

[4] P. Jarron et al., "Deep Submicron CMOS Technologies for the LHC Experiment, presented at the 6th International Conference on Advanced Technology and Particles Physics, October 5-9, 1998, Villa Olmo, Como, Italy, to be published in NIM.

[5] M. Campbell *et al.*, "A Pixel Readout Chip for 10-30 Mrad in Standard 0.25 m CMOS", presented at the IEEE NSS Conference, Toronto, Canada, November 1998, to be published on IEEE Trans. Nucl. Science.

[6] P.E. Dodd, F.W. Sexton, G.L. Hash, M.R. Shaneyfelt, B.L. Draper, A.J. Farino, R.S. Flores, "Impact of Technology Trends on SEU in CMOS SRAMs", IEEE Trans. Nucl. Science, Vol.43, No.6, p.2797, December 1996.

[7] R. Velazco, D. Bessot, S. Duzellier, R. Ecoffet, R. Koga, "2 CMOS Memory Cells Suitable for the Design of SEU-Tolerant VLSI Circuits", IEEE Trans. Nucl. Science, Vol.41, No.6, p.2229, December 1994.

[8] T. Calin, M. Nicolaidis, R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology", IEEE Trans. Nucl. Science, Vol.43, No.6, p.2874, December 1996.

[9] A.H. Johnston, "The Influence of VLSI Technology Evolution on Radiation-Induced Latchup in Space Systems", IEEE Trans. Nucl. Science, Vol.43, No.2, p.505, April 1996.

[10] T. Aoki, "Dynamics of heavy-ion-induced latchup in CMOS structures", IEEE Trans. El. Dev., Vol.35, No.11, p.1885, November 1988.

[11] C. Detcheverry, R. Ecoffet, S. Duzellier, E. Lorfevre, G. Bruguier, J. Barak, Y. Lifshitz, J.M. Palau, J. Gasiot, "SEU Sensitive Depth in a Submicron SRAM Technology", Proceedings of the 1997 RADECS Conference, Palm Beach, Cannes, France, September 15-19, 1997, p.537.