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Single Event Gate Rupture in Thin Gate Oxides

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Abstract

The dependence of single event gate rupture (SEGR) critical field on oxide thickness is examined for thin gate oxides. Critical field for SEGR increases with decreasing oxide thickness, consistent with an increasing "intrinsic" breakdown field.

Introduction

As integrated circuit densities increase with each new technology generation, both the lateral and vertical dimensions shrink. Operating voltages, however, have not scaled as aggressively as feature size, with a resultant increase in the electric fields within advanced geometry devices. Oxide electric fields are in fact increasing to greater than 5 MV/cm as feature size approaches 0.1 μm [1]. This trend raises the concern that single event gate rupture (SEGR) may limit the scaling of advanced integrated circuits (ICs) for space applications. There is evidence that SEGR is already a concern for devices that rely on thin dielectrics for electrical programming, such as field programmable gate arrays (FPGAs) [2]. Johnston [3] has predicted that at 2.5-V, technologies will near the threshold for SEGR by iron nuclei, a significant component of the galactic cosmic ray spectrum.

An early study of metal-gate and silicon-gate capacitors by Wrobel [4] indicated that SEGR failure was caused by the combination of an initiating event and a destructive runaway condition. In Wrobel's model, the initiating event was postulated to be the generation within the dielectric of a plasma column. If this plasma wire was sufficiently dense, e.g. the ion linear energy transfer (LET) was sufficiently high, a low conductivity path would be formed through which the capacitor discharged. The destructive event was the discharge of capacitively stored energy through the plasma wire. While this model matched high LET data well, it predicted an infinite critical field for low LET ions, which is obviously unphysical. Significantly, Wrobel's data indicated SEGR failure at critical fields below 5 MV/cm for ions with LET greater than 60 MeV-cm^2/mg.

More recently, Allenspach et al. [5] have developed an SEGR model based on DMOS power transistor data of Wheatley et al. [6], where the initiating event is the buildup of excess holes in the silicon substrate beneath the gate oxide. In this model the resultant transient electric field across the gate oxide increases to a point where catastrophic gate rupture is initiated. This model correctly accounts for the observed drain bias dependence of SEGR in DMOS power transistors, and also predicts a finite critical field at low LET, consistent with observation. An empirical fit to the data relied on a single valued intrinsic critical field, E_0, that is independent of oxide thickness in the range of 50 to 150 nm.

Titus et al. [7,8] further explored the dependence of SEGR in DMOS power transistors for oxide thicknesses ranging from 30 to 150 nm. Their data could be fit by a single empirical expression with an intrinsic critical field value of 10 MV/cm that was also independent of oxide thickness.

In this work, we explore the dependence of SEGR on oxide thickness for conventional thermal gate oxides from 6.5 to 18 nm — values representative of submicron geometries. We also compare our results to those of Wrobel and Allenspach. Finally, we relate our observations to present models for breakdown in dielectric layers and discuss the implications of these results on SEGR vulnerabilities in deep submicron technologies.

Test Devices and Approach

Thin oxide layers were thermally grown on n-type silicon substrates to thicknesses of 6.5, 12, and 18 nm. Following oxide growth, aluminum-gate capacitors were formed by e-beam

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evaporation of an aluminum film through a contact dot mask positioned over each wafer. The dot capacitors used in this work were 400 μm in diameter.

Devices were biased at an initial voltage well below rupture threshold, and bias was increased in steps until rupture was observed while the device under test was continuously exposed to a flux of energetic heavy ions. The SEU Test Facility at Brookhaven National Laboratories was used to provide a flux of heavy ions. Bias voltage and gate current were continuously monitored during exposure. A sudden increase in gate current or decrease in gate voltage was considered a rupture. Post-rupture IV curves confirmed that a destructive event had occurred. All exposures were at normal incidence and room temperature.

Results

Measured rupture voltage for test capacitors is shown as a function of oxide thickness and ion LET in Figure 1. Each data point is the average of three parts. The data show the expected trend of decreasing rupture voltage with increasing LET. Also shown in the figure are dashed lines indicating normal operating voltages (nominal + 10%) for 5 V and 3.3 V operation. Gate oxides of 12-nm thickness approach a critical voltage of 5.5 V (upper dashed line) at high LET, but appear to have some margin. Gate oxides of 6.5 nm approach a critical rupture voltage of 3.6 V (lower dashed line) with little to no margin at high LET.

We also show IC failure data in Figure 1 for a 16Kbit SRAM with two values of oxide thickness. The 12-nm oxide (open inverted triangle) failed at 5.5 V and an LET of 80 MeV-cm^2/mg, while a slightly thicker 14-nm oxide (open diamond) failed at 7.0 V and the same LET. The maximum voltage we could apply to the ICs was limited by drain junction breakdown and prevented us from obtaining further data at lower LET. *Failure analysis confirmed that IC failure was due to gate ruptures.* These results are slightly worse than the capacitor data at comparable oxide thicknesses at 80 MeV-cm^2/mg. This may be due to increased work functions in the n+ polysilicon gate n-channel transistors in the ICs, as compared to the n-substrate metal-gate capacitors [9]. The ICs also experienced more post gate processing which may give rise to an increase in oxide defects.

When we plot critical electric field, E_{CR}, vs. LET (Figure 2), the data show increasing critical field with decreasing oxide thickness at any given LET. The thinnest oxides in this work have critical fields well above 5 MV/cm, indicating the potential for improved SEGR tolerance for advanced technologies.

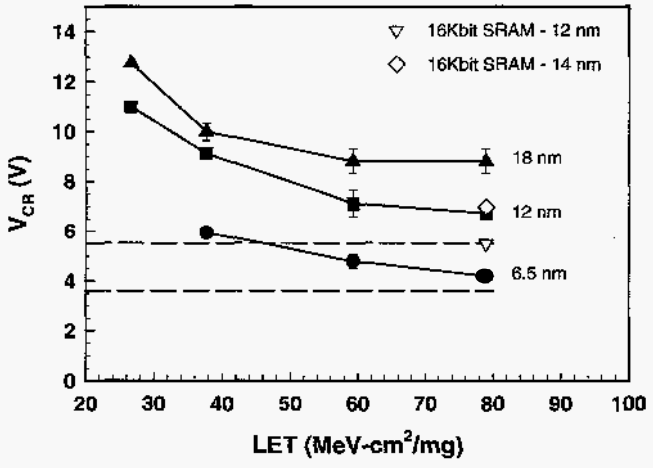

Figure 1: Critical voltages for SEGR in thin gate oxides as a function of oxide thickness and ion LET. The dashed lines correspond to maximum operating voltage (nominal plus 10%) for 5 V and 3.3 V operation, respectively. Also shown are measured failure voltages for 16Kbit SRAMs for 12-nm (inverted triangle) and 14-nm (diamond) gate oxides at 80 MeV-cm^2/mg.

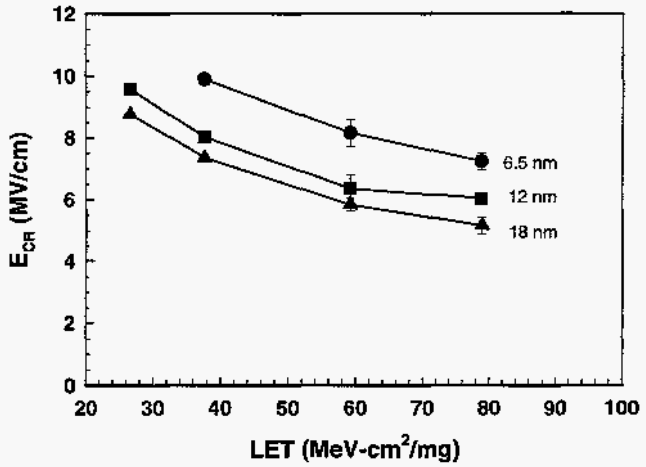

Figure 2: Critical electric field for SEGR as a function of gate oxide thickness and ion LET. Note that E_{CR} increases with decreasing oxide thickness at a given LET

Discussion

Wheatley et al. [6] described the dependence of rupture field on LET at V_{DS}=0 V with the empirical equation:

$$E_{CR} = \frac{E_o}{1 + L/B} \qquad (1)$$

where E_0 is the intrinsic breakdown field of the oxide in MV/cm, L is the ion LET in MeV-cm^2/mg, and B is a fitting parameter. For their data, B=53 MeV-cm^2/mg and E_0=10 MV/cm, from the generally assumed intrinsic breakdown strength of silicon dioxide [10]. A response of the same form has been observed by Titus et al. [7]. Allenspach et al. [5] also noted that E_0 depends to some extent on processing differences between oxides which results in a variation in intrinsic breakdown strength.

The data of this work and those of previous workers [4,6,7] are plotted as $1/E_{CR}$ vs. LET in Figure 3. Here, the y-axis intercept is equal to $1/E_0$, and the slope is equal to $1/E_0B$. Note that a lower value of $1/E_{CR}$ implies an increased SEGR tolerance. A clear pattern emerges of increasing breakdown strength with decreasing oxide thickness, even at high LET. The dependence of E_{CR} on LET also weakens as thickness decreases as seen by the decreasing slope with thinner gate oxides (Figure 3). Fitting parameters to the data are presented in Table 1.

Recent models of breakdown in oxides depend on trap creation and defect generation as hot electrons are injected into the oxide at high electric fields [11]. Thick oxides (> 15nm) exhibit both bulk hole and electron trapping at high fields,

Table 1: Summary of empirical fit parameters.

Oxide	Eo (MV/cm)	B (MeV-cm^2/mg)
This work (6.5 nm)	14.8	75
This work (12 nm)	12.0	76
This work (18 nm)	12.5	55
Wrobel 87 (45 nm)	10.9	62
Wheatley '94 (50 nm)	11.1	50
Titus '95 (30-150 nm)	10	53

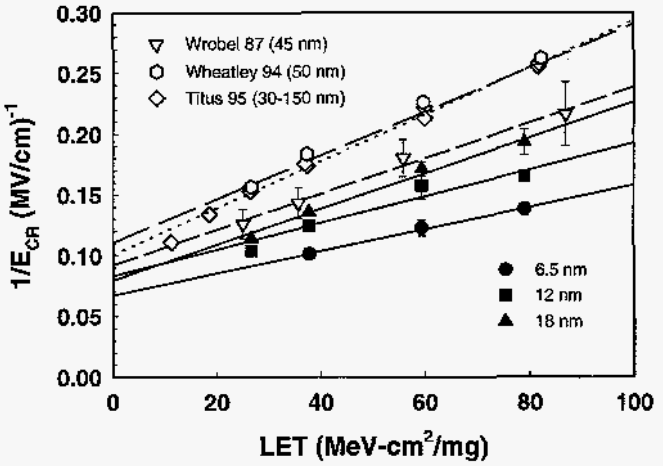

Figure 3: Comparison of the data from this work to that of previous researchers [4,6,7].

while only electron trapping is typically observed in the bulk of thin oxides (<10 nm). In Figure 3, there appears to be different regimes of behavior for the thin oxides (6.5 and 12 nm) and the thicker oxides of the Wheatley '94 and Titus '95 data sets. The 18 nm data and the Wrobel (45 nm) data fall between the thin and thick oxide response. Note that the Titus et al. data have a mixture of oxide thicknesses ranging from 30 to 150 nm. The departure from linearity at low LET (< 20) may be due to the thinner gate oxides (30 nm). A more detailed analysis of these data as a function of oxide thickness will be presented in the full paper.

Finally, we consider the implications of SEGR in thin gate oxides based on the observed increase in E_0. In Figure 4, we plot the critical voltage for SEGR as a function of oxide thickness and ion LET using a fit to the parametric data of Table 1 and equation (1). At 5.5 V operation, a minimum oxide thickness of 11 nm is required to survive a maximum LET of 80 *with no margin*. Similarly, at 3.6 V operation a minimum oxide thickness of 7 nm is required. As the IC data of Figure 1 indicate, at least a 10% margin in oxide thickness would be advised. At thin oxide thicknesses, the curves converge as a result of the weakening dependence on LET.

In the full paper we will consider the effects of oxide processing and gate electrode material on SEGR tolerance.

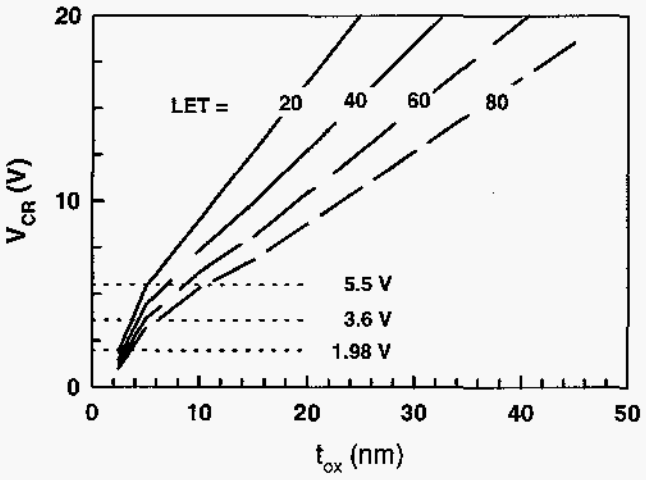

Figure 4: Maximum operating voltage as a function of oxide thickness and ion LET.

Conclusions

The industry trend toward thinner gate dielectrics raises the concern that single event gate rupture (SEGR) may be a limiting factor for integrated circuits (ICs) in space applications. Fortunately, as silicon dioxide thins, the intrinsic dielectric strength increases, and our results suggest that advanced technologies will be correspondingly more SEGR resistant at a given electric field.

Acknowledgments

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