Single Event Transient Response of SiGe Voltage References and Its Impact on the Performance of Analog and Mixed-Signal Circuits

Laleh Najafizadeh, *Student Member, IEEE*, Stanley D. Phillips, *Student Member, IEEE*, Kurt A. Moen, *Student Member, IEEE*, Ryan M. Diestelhorst, *Student Member, IEEE*, Marco Bellini, *Member, IEEE*, Prabir K. Saha, *Student Member, IEEE*, John D. Cressler, *Fellow, IEEE*, Gyorgy Vizkelethy, *Member, IEEE*, Marek Turowski, *Senior Member, IEEE*, Ashok Raman, and Paul W. Marshall, *Member, IEEE*

***Abstract*—We investigate the single-event transient (SET) response of bandgap voltage references (BGRs) implemented in SiGe BiCMOS technology through heavy ion microbeam experiments. The SiGe BGR circuit is used to provide the input reference voltage to a voltage regulator. SiGe HBTs in the BGR circuit are struck with 36-MeV oxygen ions, and the subsequent transient responses are captured at the output of the regulator. Sensitive devices responsible for generating transients with large peak magnitudes (more than 5% of the dc output voltage) are identified. To determine the effectiveness of a transistor-layout-based radiation hardened by design (RHBD) technique with respect to immunity to SETs at the circuit level, the BGR circuit implemented with HBTs surrounded by an alternate reverse-biased pn junction (n-ring RHBD) is also bombarded with oxygen ions, and subsequent SETs are captured. Experimental results indicate that the number of events causing transients with peak magnitude more than 5% above the dc level have been reduced in the RHBD version; however, with the inclusion of the n-ring RHBD, new locations for the occurrence of transients (albeit with smaller peak magnitude) are created. Transients at the transistor-level are also independently captured and are presented. It is demonstrated that while the transients are short at the transistor level (ns duration), relatively long transients are obtained at the circuit level (hundreds of nanoseconds). In addition, the impact of the SET response of the BGR on the performance of an ultra-high-speed 3-bit SiGe analog-to-digital converter (ADC) is investigated through simulation. It is shown that ion-induced transients in the reference voltage could eventually lead to data corruption at the output of the ADC.**

***Index Terms*—Radiation hardening by design (RHBD), silicon-germanium (SiGe), silicon-germanium heterojunction bipolar transistor (SiGe HBT), single-event transient (SET), time-resolved ion-beam induced charge collection (TRIBICC), voltage references.**

Manuscript received July 17, 2009; revised September 28, 2009. Current version published December 09, 2009. This work was supported by the NASA-GSFC under the NASA Electronic Parts and Packaging (NEPP) program, the NASA Exploration Technology Development Program (ETDP), the Defense Threat Reduction Agency (DTRA) under the Radiation Hardened Microelectronics Program, and an AFOSR Multidisciplinary University Research Initiative (MURI) program. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DEAC04-94AL85000.

L. Najafizadeh, S. D. Phillips, K. A. Moen, R. M. Diestelhorst, M. Bellini, P. K. Saha, and J. D. Cressler are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: laleh@ece.gatech.edu; stan.phillips@gatech.edu; kmoen@ece.gatech.edu; ryan@ece.gatech.edu; bellini@ece.gatech.edu; prabirs@ece.gatech.edu; cressler@ece.gatech.edu).

G. Vizkelethy is with Sandia National Laboratory, Albuquerque, NM 97185 USA (e-mail: gvizkel@sandia.gov).

M. Turowski and A. Raman are with CFD Research Corporation, Huntsville, AL 35805 USA (e-mail: mt@cfdrc.com; ar2@cfdrc.com).

P. W. Marshall is a consultant with NASA-GSFC, Brookneal, VA 24528 USA (e-mail: pwmarshall@aol.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2009.2034159

I. Introduction

SINGLE-EVENT transients (SETs) can originate when high-energy particles interact with sensitive structures in a circuit and deposit sufficient energy to generate electron-hole pairs near critical electrical nodes of the device. During SETs, the corresponding injected charge carriers can appear in the form of either voltage or current spikes (or both), which are then able to propagate from the device through the circuit to the system, resulting in transient excursions, data corruption, and possibly system failure. Since first reported in 1993 in operational amplifiers (opamps) and voltage comparators [1], the SET response of different types of circuits (mostly commercial, off-the-shelf products) have been investigated through a variety of beam experiments and device/circuit simulations [2]–[21]. When the SET response of a particular circuit is determined, usually under specific operating conditions, one may not be able to use this response to predict the SET response of a system where the circuit is used as a subsystem. Therefore, SET effects continue to be a growing concern for space electronics. This is due to the fact that the amplitude and the duration of SETs depend on several factors, including output load, dynamic nodal impedances, operating conditions, and the nature of the radiation environment [22].

Silicon-germanium heterojunction bipolar transistors (SiGe HBTs,) with their known inherent multi-$\mathrm{Mrad(SiO_2)}$ total ionizing dose (TID) tolerance, enhanced performance at cryogenic temperatures, low cost, and performance comparable with that of III-V materials, have become prime contenders for a variety of space-borne circuit applications [23]. With regard to single-event effects (SEEs), SiGe HBTs do, however, lack immunity due to charge collection through the reversed-biased lightly-doped substrate (p) to subcollector (n) junction [24], [25]. Therefore, mitigation techniques, which can be accom-

0018-9499/$26.00 © 2009 IEEE

plished at the circuit level [26], at the device level [27], [28], or both, need to be further incorporated in SiGe-based circuits to reduce their vulnerability to SEEs. To date, most of the research on SEE in SiGe has centered on single-event upset (SEU) in high-speed digital circuits. Here, we focus on SET in analog/mixed-signal circuits.

Bandgap voltage references (BGRs) are extensively used in a variety of circuits required for space applications, including regulators, and data converters. The TID tolerance of SiGe reference circuits due to proton irradiation was previously investigated [29], where it was shown that proton-induced changes in the SiGe bandgap references are minor. However, no results exist on their SET response, and importantly, how SETs in such precision references can affect the performance of other circuits that are critically dependent on BGRs for their operation. In this paper, the SET response of a SiGe BGR circuit is investigated experimentally for the first time. This BGR circuit is used to provide the input reference voltage to a voltage regulator. SiGe HBTs in the BGR were then struck via ion microbeam experiments, and the subsequent transient responses at the output of the regulator are reported. In addition, the effectiveness of employing transistor-layout RHBD techniques for mitigating SETs in the BGR circuit are also investigated. Studies of this RHBD approach have, to date, centered only on digital circuits [26]. The applied transistor-layout RHBD approach for mitigating single-event effects provides a low-impedance secondary path for the excess charge carriers (generated as a result of ion strike) by including an additional reverse-biased pn junction [27]. This is accomplished by surrounding the deep trench (DT) area of the device by an n-type implant [n-ring (NR)] and by biasing it with a positive dc voltage to shunt charge away from the collector. This technique has been applied to HBTs in the BGR circuit, and its heavy ion microbeam transient response has been evaluated and compared with the transient response from the standard version. It is shown that the applied RHBD technique provides some degree of immunity to SETs at the circuit level.

II. Circuit Description and Experiment

The technology used to implement the voltage reference and regulator circuits is the commercially available, first-generation IBM SiGe 5AM technology. This six-level metal process technology features npn SiGe HBTs with an emitter width of 0.5 μm and a unity gain cutoff frequency and maximum frequency of oscillation of 45 and 60 GHz at room temperature, respectively. The DT surrounding the active area is estimated to be 8 μm deep. All SiGe HBTs under investigation have single emitter stripe (CEB configuration) with emitter area of $0.5 \times 2.5\ \mu\text{m}^2$. Proton tolerance, laser-induced current transients, and single-event upset mechanisms of these transistors have been reported in [19], [30], and [31]. The RHBD structure employs an n-type implant (N^+ Subcollector) layer that surrounds the HBT's DT area. Top-down and cross-section views of both devices are shown in Fig. 1. Neither dc or ac performance of the RHBD device is expected to be affected by the inclusion of the n-ring [27]. In addition, since the location of emitter-base spacer and shallow trench isolation remains intact, it is expected that the RHBD transistor will maintain its TID hard capability.

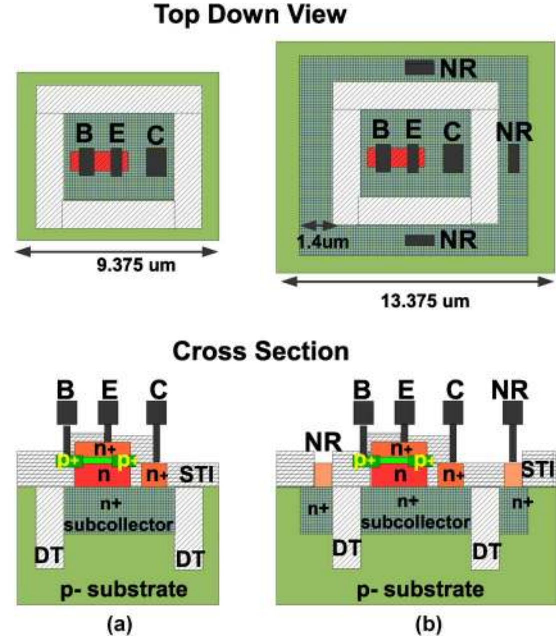

Fig. 1. Top-down and cross-section views of the (a) standard HBT and (b) RHBD HBT.

Fig. 2 shows the schematic of the voltage regulator designed for this study. An exponential, curvature-compensated BGR [32] was used to provide the reference voltage (V_{ref}) to the positive input of an operational amplifier (opamp). The opamp is a two-stage amplifier followed by an emitter-follower buffer, and it is biased with an on-chip current source. The die photo is shown in Fig. 3, indicating the location of each circuit on the chip. The output voltage of the regulator is given by

$$V_{\text{out}} = V_{\text{ref}}\left(1 + \frac{R_7}{R_8}\right). \quad (1)$$

The SiGe BGR circuit is designed to generate an output voltage of 1.17 V at room temperature, and an output voltage of 1.65 V is expected from the regulator. During normal circuit operation, the substrate is grounded, and a power supply of 3.3 V is used to bias the circuit.

The SiGe regulator circuit, along with HBT test structures (consisting of four parallel $0.5 \times 2.5\ \mu\text{m}^2$ HBTs), were mounted onto a high-speed board specifically designed for this experiment. The board consist of Rogers material that provides the electrical properties essential for high frequency applications. Using 1-mil gold bond wires, each terminal of the device under the test was wirebonded to an on-board transmission line with impedance characteristic of approximately 50 Ω. At the back of the board, 18-GHz subminiature version A (SMA) connectors were provided for each terminal to establish electrical connectivity. These SMA launchers were connected to the terminals of a Tektronix DPO72004 20-GHz (50 GS/s) real-time digital oscilloscope via 40-GHz cables and through 40-GHz bias tees. Fig. 4 illustrates the experimental setup used for testing the SiGe regulator.

Time-resolved ion-beam induced charge collection (TRIBICC) testing [33] was performed at Sandia National Laboratory using 36-MeV ^{16}O ions, with a peak LET of

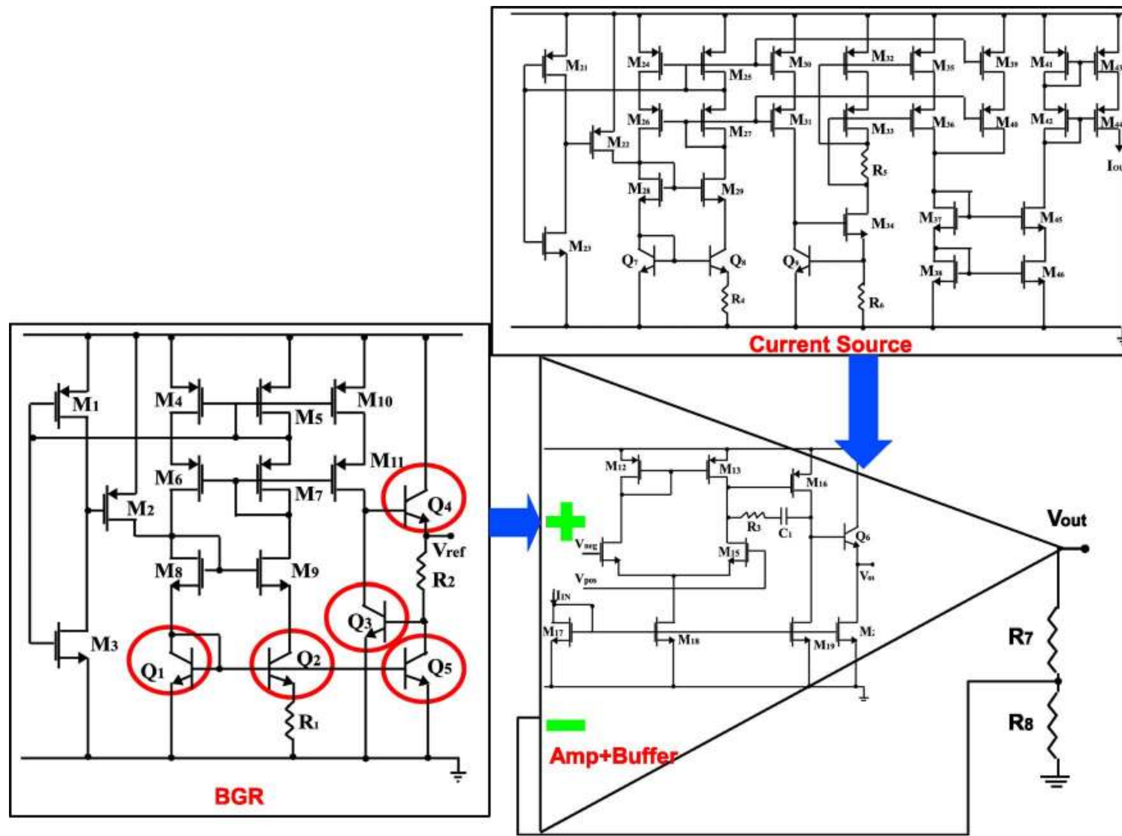

Fig. 2. Schematic of SiGe voltage regulator.

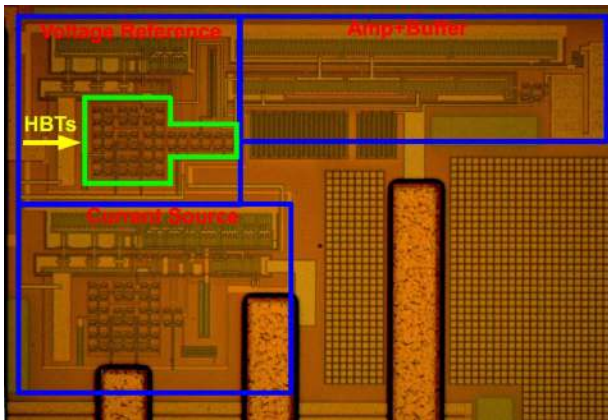

Fig. 3. Die photograph of SiGe voltage regulator.

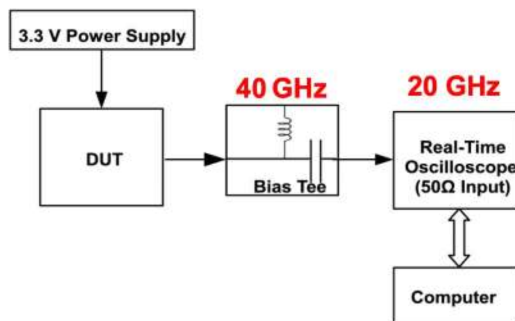

Fig. 4. Diagram of the experimental test setup.

5.4 MeV.cm^2/mg. During ion strikes, the regulator circuits were maintained under normal operating conditions. In the RHBD version of the regulator, the n-ring was shorted to the supply rail (3.3 V). For standard HBT structures that were irradiated, all terminals of the transistors were grounded ($V_C = V_B = V_E = 0$ V) except for the substrate, which was biased at -4 V ($V_{\rm SUB} = -4$ V). Same biasing conditions were applied to the collector, emitter, base and the substrate terminals of RHBD HBT structures, with the N-ring terminal biased at 2 V ($V_{\rm NR} = 2$ V).

III. Experimental Results

The SiGe HBT bank in the BGR circuit, (transistors Q1–Q5 shown in Fig. 2) was targeted for heavy ion strikes. Note that transistors Q1 and Q3–Q5 each consist of four parallel $0.5 \times 2.5\ \mu\text{m}^2$ HBTs, and transistor Q2 consists of 32 parallel $0.5 \times 2.5\ \mu\text{m}^2$ SiGe HBTs. To achieve better matching between Q1 and Q2, a common centroid layout technique was employed. In this section, we will present the microbeam experimental results for both standard and RHBD regulators. Measured transients at the transistor level for both standard and RHBD cases are also presented.

A. Regulator With Standard SiGe HBTs

The heavy ion beam was scanned over the HBT block shown in Fig. 5 and the corresponding transients at the output of the regulator with peak magnitude larger than 12 mV were captured (limited by scope resolution). Fig. 6 illustrates the relative

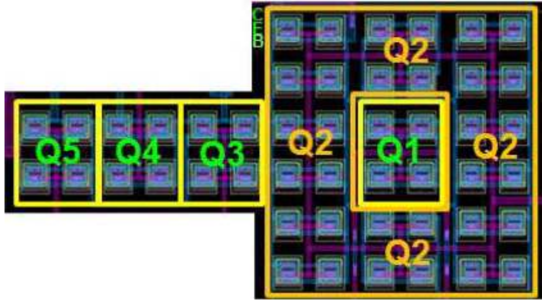

Fig. 5. Layout of the SiGe HBT bank in the BGR circuit.

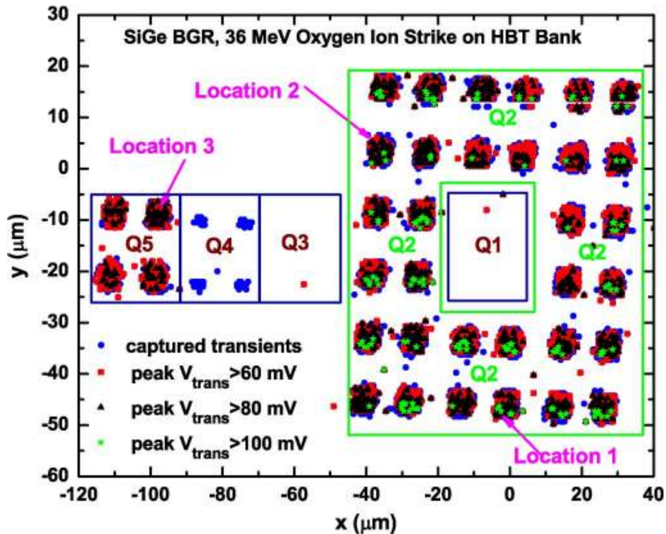

Fig. 6. Locations of the strikes generating transients at the output of the regulator.

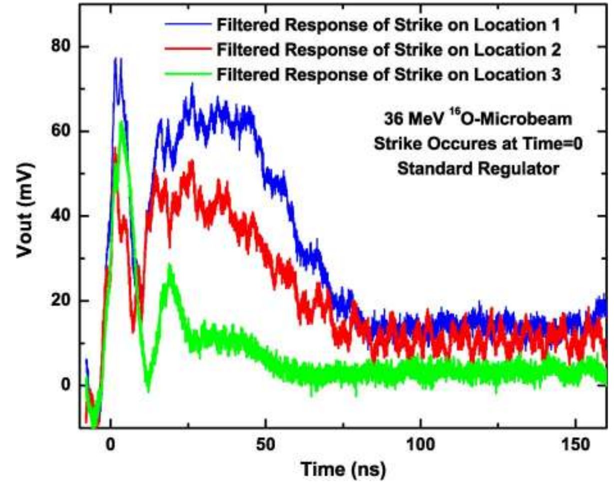

Fig. 7. Single-event transient response of the regulator for three different strike locations.

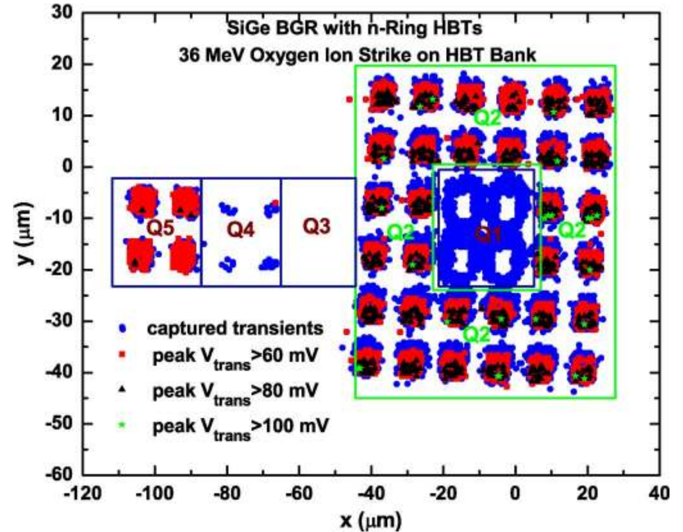

Fig. 8. Location of strikes generating transients at the output of the RHBD regulator.

positions of the strikes on the HBT bank that have generated such transients. Locations of the strikes causing transients with peak magnitudes larger than 60, 80, and 100 mV have been also marked. We observe that transient response strongly depends on the location of the ion strike, as expected. Interestingly, transistors Q1 and Q3 are shown to be insensitive with respect to SET for this circuit. Emitter strikes on transistor Q4 create transients with small peak magnitude, and the mirroring transistors, Q2 and Q5, are responsible for generating the transients with peak magnitude larger than 5% of dc level. All the transients with peak magnitude larger than 100 mV occur as a result of emitter strike on the 32 HBTs shaping transistor Q2.

A typical transient response waveform at the output of the regulator for three strike locations (two over Q2 and one over Q5) is plotted in Fig. 7 (corresponding locations over the HBT bank are marked in Fig. 6). It is observed that the transient responses exhibit double peak waveforms. The first peak has a large magnitude and decays rapidly, while the second peak has a smaller magnitude but larger decay duration. This figure also indicates that strikes over the HBTs forming Q2 cause transients that not only have large magnitudes, but also long durations (up to 100 s of ns versus only a few ns for a transistor-only transient). This demonstrates that strong circuit-level effects are operative.

B. Regulator With RHBD SiGe HBTs

To examine the effectiveness of transistor layout-based RHBD with respect to providing SET immunity at the circuit level, the HBT bank in the regulator implemented with RHBD transistors was also bombarded with heavy oxygen ions. The location of the strikes on the RHBD HBT bank in the BGR circuits causing transients is shown in Fig. 8. Comparing Figs. 6 and 8, one can conclude that the number of transient events with large peak magnitude have been significantly reduced in the RHBD version of the circuit, which is clearly good news. The peak magnitude of transients as a result of striking Q5, except for three cases, remains below 80 mV, while in the standard version, the probability of getting transients larger than 80 mV from strikes on Q5 is much higher. An interesting (and unexpected) observation that can be made by inspecting Fig. 8 is the fact that striking outside the active area of the four HBTs shaping Q1 results in transients (with small peak magnitude)

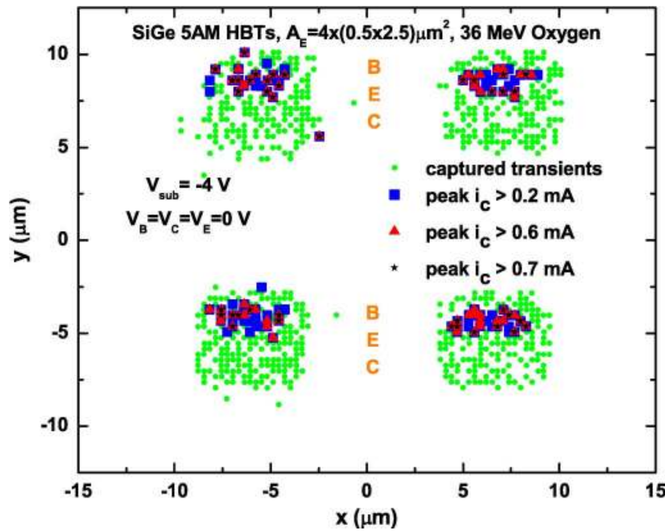

Fig. 9. Location of strikes generating transients in the HBT structure.

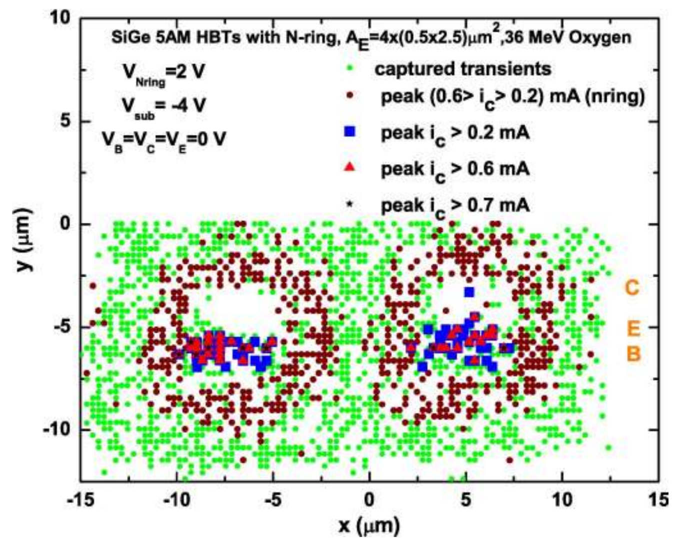

Fig. 11. Location of strikes generating transients in the RHBD HBT structure.

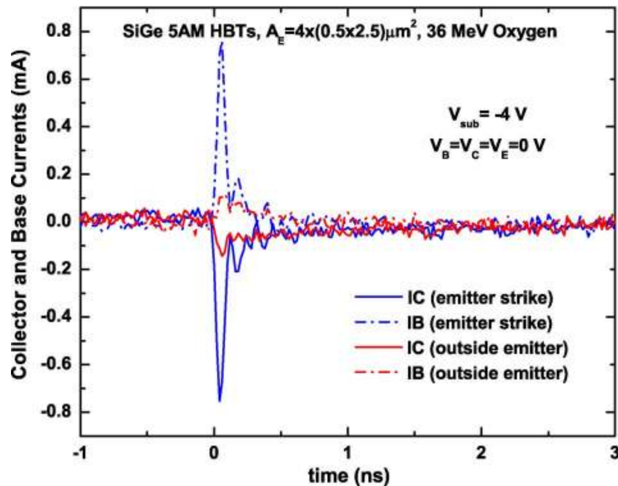

Fig. 10. Collector and base transient currents for strikes over and outside the emitter area for standard HBTs.

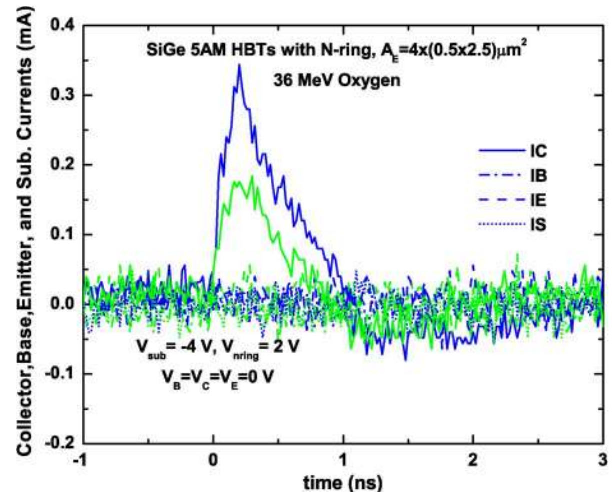

Fig. 12. Collector, base, emitter, and substrate transient currents for two strikes outside the active area in RHBD HBTs.

at the output of the regulator, which was not observed in the standard implementation.

C. Transistor-Level Response

To shed light on understanding the observed anomalies with respect to striking Q1 in the RHBD version of the regulator, test structures consisting of four parallel standard/RHBD HBTs were implemented and bombarded with oxygen ions. Transient currents were captured at the collector, base, emitter, and substrate terminals. Fig. 9 shows the location of the strikes causing transients at the collector terminal. This figure indicates that transients with large peak magnitude occur when striking the emitter area, which is expected. The transient collector and base currents for strikes over and outside the emitter area are shown in Fig. 10. Note that the duration of transient current is much less than 1 ns. The positions of strikes for the RHBD case are shown in Fig. 11. Similar to the standard case, emitter strikes generate the largest peak magnitude transients, and the shape of the current transient waveforms is similar to what is observed for the standard case. However, by moving away from the active transistor area, new transient events are observed. Plotted in Fig. 12, are the captured transient currents at the substrate, base, emitter and collector terminals of the RHBD device for two strikes that are located outside the DT and over the n-ring area. Note that the polarity of the collector current has been changed, indicating that the type of carriers have been changed from electrons (for strikes inside the active area) to holes at the collector node.

IV. Discussion

Experimental measurements presented in the previous section reveal four important results. First, transistors within the circuit generate different SET responses at the output of the circuit. For the BGR circuit under study, while strikes to transistor Q3 and the diode connected transistor Q1 did not generate transients at the output of the circuit, striking the mirroring transistors, Q2 and Q5, generated transients with large peak magnitudes (more

than 5% of the dc level) in the regulator output. Further understanding of this observation could possibly lead to solutions for developing circuit-level hardening techniques.

Second, significant differences between the transient duration of an ion strike at the device level and at the circuit level were observed. While the duration of current transients in SiGe HBTs stays below 1 ns, it was observed that the corresponding transients at the circuit level could last hundreds of nanoseconds. These results indicate that the circuit topology (e.g., feedback) can play a very strong role in defining the analog transient duration as it has also been observed in other circuit topologies [17], [34]. Therefore, special attention must be paid in designing mixed-signal circuits so that SET does not become a significant threat to the overall system. The results also strongly suggests that true mixed-mode TCAD simulations will be required for accurate modeling of SET in mixed-signal SiGe circuits.

Third, it was demonstrated that employing layout-based RHBD technique is to some degree effective with respect to providing SET immunity in analog circuits. The magnitude of the peak transients were significantly reduced in the RHBD version compared to the standard version. However, new locations (around the n-ring area of certain transistors in the circuit) for the occurrence of transients with smaller peak magnitudes were observed. This problem may be resolvable by changing the electric field across the isolation junction by varying the n-ring bias voltage but requires further investigation.

Finally, new transient effects from strikes to the n-ring area in RHBD transistors were captured. While the collector terminal has been identified as the sink for electrons, the observed collector transient currents for ion strikes over the n-ring area and over the active area have opposite polarities. For transients over the n-ring area, transient currents with negative polarity were captured. While it was shown through ion-beam-induced charge collection (IBICC) experiments that use of an external n-ring provides up to 90% reduction in collector collected charge [27], our results indicate that transient currents still exist. More investigation is required to understand the physics of such complex transients in the presence of device-level RHBD.

V. Impact on ADC

Precision voltage references are widely used in data converters. To examine the impact of the SiGe BGR SET response on the performance of SiGe ADCs, a measured SET waveform of the regulator with a peak magnitude of 83.2 mV was incorporated into the voltage reference used to set reference values for the 3-bit 20-GS/s SiGe ADC-DAC circuit. The block diagram of the 3-bit ADC-DAC is shown in Fig. 13. The 3-bit flash ADC consists of a resistor ladder subdividing the $V_{\rm ref}$ voltage into $2^3 - 1$ equal segments, and $2^3 - 1$ comparators. The block diagram of the comparator is shown in Fig. 14. The comparator consists of a preamplifier and two master/slave stages. The second master/slave stage was added to reduce the effective regeneration time constant [36]. The function of the comparator is to compare the input signal with a reference level and consequently generate a logic output of "one" or "zero". Each comparator compares the input signal with the fraction of $V_{\rm ref}$ at its input and generates the corresponding logic level. The ADC converts the input analog signal into a seven-level

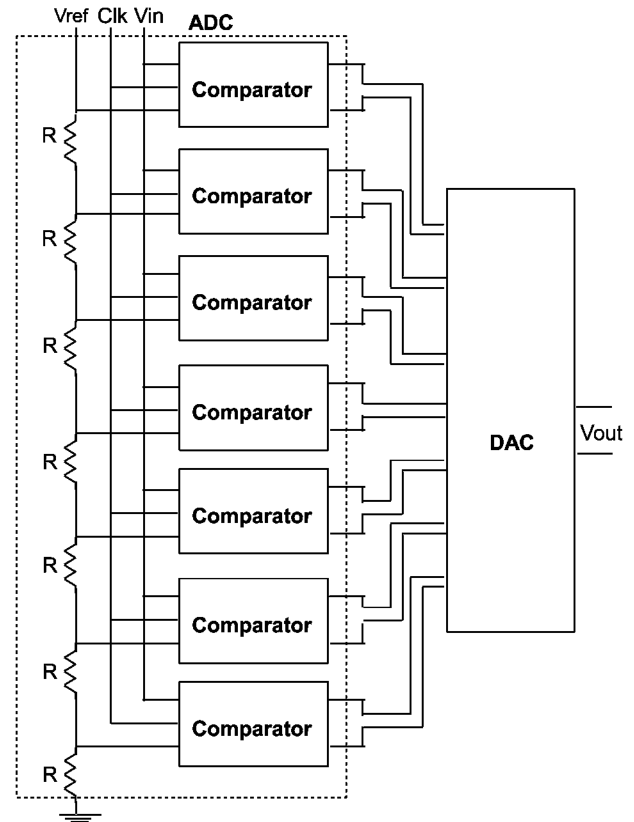

Fig. 13. Block diagram of the 3-bit high-speed ADC-DAC.

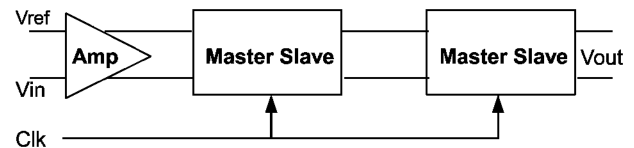

Fig. 14. Block diagram of the high-speed comparator.

thermometer digital code. A seven-level thermometer code DAC has been implemented on chip, both as a standalone circuit, and also directly connected to the output of the ADC to facilitate testing. The DAC follows the current-steering topology [37], [38] and consists of seven HBT-differential pairs designed in current-mode logic configuration and driven by the thermometer codes that are generated at the output of the ADC. The output currents of these current mode logic inverters are summed at the on-chip 50 Ω resistors to reconstruct the input signal sent to the ADC. In an ideal case, eight levels of quantization should appear at the output of DAC.

In our simulation deck, a 500-MHz sinusoidal signal was applied to the input. The ADC's clock frequency was set to 12.5 GHz. A measured transient response was included in the voltage source setting the reference levels for the comparators and transient simulations were run. Shown in Fig. 15 are the simulated output waveforms from the DAC prior to and during the occurrence of SET in the SiGe voltage reference. Note that one quantization step has been missed due to inclusion of SET in the voltage reference, clearly a potential concern. This observation is better explained in Fig. 16 for a 2-bit ADC. The input signal

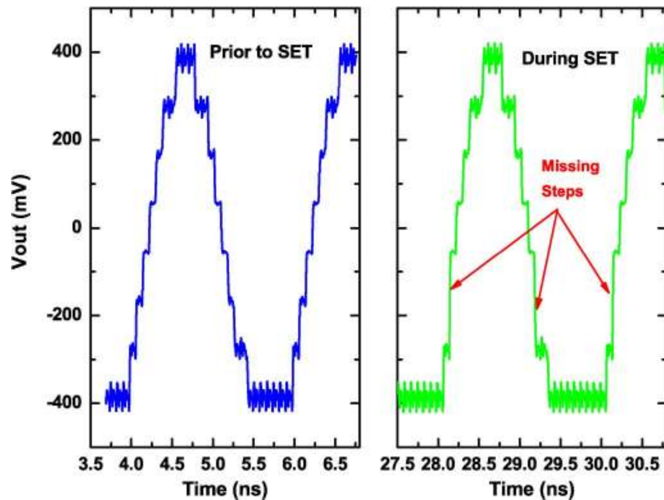

Fig. 15. Simulated output waveform of the 3-bit SiGe ADC-DAC, prior to and during an SET event in the $V_{\rm ref}$.

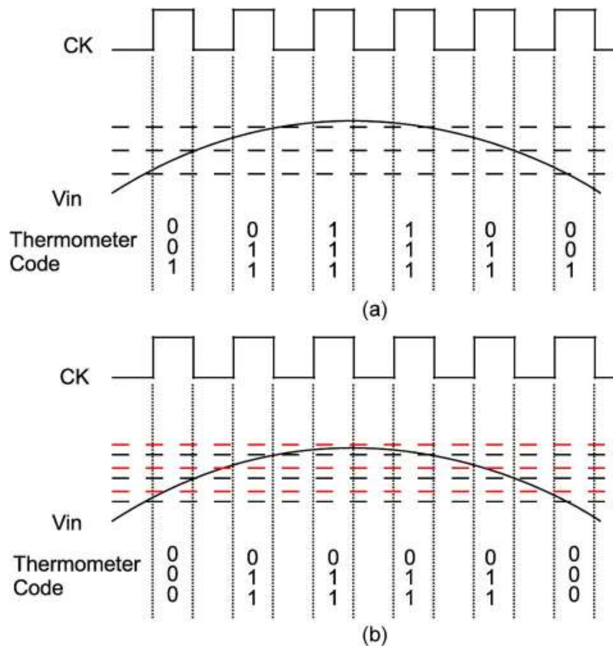

Fig. 16. Generation of thermometer codes at the output of a 2-bit ADC a) prior to the ion strike and b) during an SET event in the $V_{\rm ref}$.

is compared to three reference levels at the positive edge of the clock and the corresponding thermometer codes are generated. The SET occurrence in the BGR will result in a time-dependent reference voltage at the input of each comparator. The duration of the SET is assumed to be long enough to last six clock cycles. The transient in the voltage reference shifts the reference points to new voltage levels (lighter dashed-lines in Fig. 16(b)), and as a result, the digital output codes are corrupted in the first, third, fourth, and the sixth clock cycles. This issue becomes of greater concern for high resolution ADCs, since the output code will become extremely sensitive to changes in the reference levels. SETs in the BGR reference could eventually lead to digital data corruption in such circuits.

VI. Summary

Analog single-event transient response of SiGe bandgap voltage references used in a regulator circuit were examined through heavy ion microbeam experiments. The HBT banks in the BGR circuit were struck with 36-MeV oxygen ions and the transient responses were captured at the output of the regulator. It was demonstrated that the shape of the transient waveform depends on the location of the strike. Sensitive HBTs in the BGR circuit were identified. Some transistors were shown to be insensitive with respect to generating transients at the output of the regulator, while others were responsible for creating worst-case transients (long duration and large peak magnitude). Further understanding of this observation could possibly lead to solutions for developing circuit-level hardening techniques. HBT structures were also bombarded with 36-MeV oxygen ions, and their current transient waveforms at transistor's terminals were captured. Comparing the transient waveforms at the device level to the waveforms at the circuit level, it was observed that the duration of current transients at the device level is less than 1 ns, while at the circuit level, transients as along as 150 ns were captured (at least 150× larger). This comparison demonstrates that unlike in the digital world, in analog and mixed-signal domain, circuit topology plays a very strong role in defining the transient shapes and duration. To examine the effectiveness of transistor-layout-based RHBD techniques with respect to immunity to SETs at the circuit level, an RHBD version of the BGR circuit was also bombarded with heavy ions. Experimental results indicated that the number of events with large peak magnitudes have been reduced in the RHBD version compared to the standard version; however, with the inclusion of the RHBD n-ring, new locations for the occurrence of transients (albeit with smaller peak magnitude) were created. A measured transient voltage at the output of the regulator was used to evaluate the impact of BGR's SET on the performance of a SiGe ADC. It was shown, through simulation, that SET in reference voltage circuits can result in output code corruption at the output of an ADC. This issue could become a great concern for high resolution and high-speed ADCs.

Acknowledgment

The authors would like to thank K. LaBel, L. Cohn, A. Keys, M. Beatty, M. Watson, A. Joseph, the NASA SiGe ETDP team, and the SiGe team at IBM for their contributions and support of this work.

References

[1] R. Koga, S. D. Pinkerton, S. C. Moss, D. C. Mayer, S. LaLumondiere, S. J. Hansel, K. B. Crawford, and W. R. Crain, "Observation of single event upsets in analog microcircuits," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1838–1844, Dec. 1993.

[2] R. Harboe-Sorensen, F. X. Guerre, H. Constans, J. V. Dooren, G. Berger, and W. Hajdas, "Single event transient characterisation of analog IC's for ESA's satellites," in *Proc. Radiat. Effects Compon. Syst. Conf.*, 1999, pp. 573–581.

[3] P. Adell, R. D. Schrimpf, H. J. Barnaby, R. Marec, C. Chatry, P. Calvel, C. Barillot, and O. Mion, "Analysis of single-event transients in analog circuits," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pt. 3, pp. 2616–2623, Dec. 2000.

[4] A. H. Johnston, G. M. Swift, T. F. Miyahira, and L. D. Edmo, "A model for single-event transients in comparators," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pt. 3, pp. 2624–2633, Dec. 2000.

[5] A. L. Sternberg, L. W. Massengill, R. D. Schrimpf, and P. Calvel, "Application determination of single-event transient characteristics in the LM 111 comparator," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pt. 1, pp. 1855–1858, Dec. 2001.

[6] S. Buchner, D. McMorrow, A. Sternberg, L. Massengill, R. L. Pease, and M. Maher, "Single-event transient (SET) characterization of an LM119 voltage comparator: An approach to SET model validation using a pulsed laser," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 3, pt. 3, pp. 1502–1508, Jun. 2002.

[7] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, R. L. Pease, S. Buchner, J. W. Howard, D. McMorrow, M. W. Savage, and C. Poivey, "Circuit modeling of the LM124 operational amplifier for analog single-event transient analysis," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pt. 1, pp. 3090–3096, Dec. 2002.

[8] A. H. Johnston, T. F. Miyahira, L. D. Edmonds, and F. Irom, "Single-event transients in high-speed comparators," *IEEE Trans. Nucl. Sci,*, vol. 49, no. 6, pt. 1, pp. 3082–3089, Dec. 2002.

[9] W. Chen, V. Pouget, G. K. Gentry, H. J. Barnaby, J. D. Cressler, G. Niu, P. Fouillat, Y. Deval, and D. Lewis, "Investigation of single-event transients in voltage-controlled oscillators," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pt. 1, pp. 2081–2087, Dec. 2003.

[10] M. W. Savage, J. L. Titus, T. L. Turflinger, R. L. Pease, and C. Poivey, "A comprehensive analog single-event transient analysis methodology," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pt. 2, pp. 3546–3552, Dec. 2004.

[11] P. C. Adell, R. D. Schrimpf, C. R. Cirba, W. T. Holman, X. Zhu, H. J. Barnaby, and O. Mion, "Single event transient effects in a voltage reference," *Microelectron. Rel.*, vol. 45, pp. 355–359, Feb. 2005.

[12] B. D. Olson, D. R. Ball, K. M. Warren, L. W. Massengill, N. F. Haddad, S. E. Doyle, and D. McMorrow, "Simultaneous single event charge sharing and parasitic bipolar conduction in a highly-scaled SRAM design," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pt. 1, pp. 2132–2136, Dec. 2005.

[13] "Single event testing of the IS-1009RH voltage reference," Intersil, Oct. 2000 [Online]. Available: http://www.intersil.com/space/IS-1009RH_SEE_Test_Report.pdf

[14] P. C. Adell, A. F. Witulski, R. D. Schrimpf, R. M. V. Pouget, P. Calvel, and F. Bezerra, "Single event-induced instability in linear voltage regulators," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pt. 1, pp. 3506–3511, Dec. 2006.

[15] A. T. Kelly, P. Adell, A. F. Witulski, W. T. Holman, R. D. Schrimpf, and V. Pouget, "Total dose and single event transients in linear voltage regulators," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 4, pt. 3, pp. 1327–1334, Aug. 2007.

[16] T. D. Loveless, L. W. Massengill, W. T. Holman, and B. L. Bhuva, "Modeling and mitigating single-event transients in voltage-controlled oscillators," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pt 1, pp. 2561–2567, Dec. 2007.

[17] T. D. Loveless, L. W. Massengill, B. K. Bhuva, W. T. Holman, R. A. Reed, D. McMorrow, J. S. Melinger, and P. Jenkins, "A single-event-hardened phase-locked loop fabricated in 130 nm CMOS," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pt. 1, pp. 2012–2020, Dec. 2007.

[18] B. D. Olson, W. T. Holman, L. W. Massengill, B. L. Bhuva, and P. R. Fleming, "Single-event effect mitigation in switched-capacitor comparator designs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pt. 1, pp. 3440–3446, Dec. 2008.

[19] E. J. Montes, R. A. Reed, J. A. Pellish, M. L. Alles, R. D. Schrimpf, R. A. Weller, M. Varadharajaperumal, G. Niu, A. K. Sutton, R. M. Diestelhorst, G. Espinel, R. Krithivasan, J. P. Comeau, J. D. Cressler, P. W. Marshall, and G. Vizkelethy, "Single event upset mechanisms for low-energy-deposition events in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 3, pt. 3, pp. 1581–1586, Jun. 2008.

[20] P. Jaulent, V. Pouget, D. Lewis, and P. Fouillat, "Study of single-event transients in high-speed operational amplifiers," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pt. 1, pp. 1974–1981, Aug. 2008.

[21] F. Irom, T. F. Miyahira, P. C. Adell, J. S. Laird, B. Conder, V. Pouget, and F. Essely, "Investigation of single-event transients in linear voltage regulators," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pt. 1, pp. 3352–3359, Dec. 2008.

[22] R. L. Pease, "Modeling single event transients in bipolar linear circuits," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pt. 1, pp. 1879–1890, Aug. 2008.

[23] J. D. Cressler, "On the potential of SiGe HBTs for extreme environment electronics," *Proc. IEEE*, vol. 93, pp. 1559–1582, Sep. 2005.

[24] G. Niu, J. D. Cressler, M. Shoga, K. Jobe, P. Chu, and D. L. Harame, "Simulation of SEE-induced charge collection in UHV/CVD SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pt. 3, pp. 2682–2689, Dec. 2000.

[25] M. Varadharajaperumal, G. Niu, R. Krithivasan, J. D. Cressler, R. A. Reed, P. W. Marshall, G. Vizkelethy, P. E. Dodd, and A. J. Joseph, "3-D simulation of heavy-ion induced charge collection in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pt. 1, pp. 2191–2198, Dec. 2003.

[26] R. Krithivasan, M. Bellini, A. P. G. Prakash, G. A. Espinel, J. D. Cressler, P. W. Marshall, and C. J. Marshall, "Proton tolerance of SiGe precision voltage references for extreme temperature range electronics," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pt. 1, pp. 3400–3407, Dec. 2006.

[27] A. K. Sutton, M. Bellini, J. D. Cressler, J. A. Pellish, R. A. Reed, P. W. Marshall, G. Niu, G. Vizkelethy, M. Turowski, and A. Raman, "An evaluation of transistor-layout RHBD techniques for SEE mitigation in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pt. 1, pp. 2044–2052, Dec. 2007.

[28] M. Varadharajaperumal, G. Niu, X. Wei, T. Zhang, J. D. Cressler, R. A. Reed, and P. W. Marshall, "3-D simulation of SEU hardening of SiGe HBTs using shared dummy collector," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pt. 1, pp. 2330–2337, Dec. 2007.

[29] L. Najafizadeh, M. Bellini, A. P. G. Prakash, G. A. Espinel, J. D. Cressler, P. W. Marshall, and C. J. Marshall, "Proton tolerance of SiGe precision voltage references for extreme temperature range electronics," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pt. 1, pp. 3210–3216, Dec. 2006.

[30] A. P. G. Prakash, A. Sutton, R. Diestelhorst, G. Espinel, J. Andrews, B. Jun, J. D. Cressler, and C. J. Marshall, "The effect of irradiation temperature on the proton response of SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pt. 1, pp. 3175–3181, Dec. 2006.

[31] J. A. Pellish, R. A. Reed, D. McMorrow, J. S. Melinger, P. Jenkins, A. K. Sutton, R. M. Diestelhorst, S. D. Phillips, J. D. Cressler, V. Pouget, N. D. Pate, J. A. Kozub, M. H. Mendenhall, R. A. Weller, R. D. Schrimpf, P. W. Marshall, A. D. Tipton, and G. Niu, "Laser-induced current transients in silicon-germanium HBTs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pt. 1, pp. 2936–2942, Dec. 2008.

[32] L. Najafizadeh, A. K. Sutton, R. M. Diestelhorst, M. Bellini, B. Jun, J. D. Cressler, P. W. Marshall, and C. J. Marshall, "A comparison of the effects of X-ray and proton irradiation on the performance of SiGe precision voltage references," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pt. 1, pp. 2238–2244, Dec. 2007.

[33] H. Schone, D. S. Walsh, F. W. Sexton, B. L. Doyle, P. E. Dodd, J. F. Aurand, R. S. Flores, and N. Wing, "Time-resolved ion beam induced charge collection (TRIBICC) in micro-electronics," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pt. 1, pp. 2544–2549, Dec. 1998.

[34] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, B. L. Bhuva, and W. T. Holman, "Towards SET mitigation in RF digital PLLs: From error characterization to radiation hardening considerations," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 4, pt. 1, pp. 2047–2053, Aug. 2006.

[35] W. Chen, N. Varanasi, V. Pouget, H. J. Barnaby, B. Vermeire, P. C. Adell, T. Copani, and P. Fouillat, "Impact of VCO topology on SET induced frequency response," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pt. 1, pp. 2500–2505, Dec. 2007.

[36] W. Cheng, W. Ali, M. Choi, K. Liu, T. Tat, D. Devendorf, L. Linder, and R. Stevens, "A 3b 40 GS/s ADC-DAC in 0.12 μm SiGe," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2004, pp. 262–263.

[37] B. Razavi*, Principles of Data Conversion Sysytem Design*. New York: IEEE Press, 1995.

[38] S. Halder and H. Gustat, "A 30 GS/s 4-bit binary weighted DAC in SiGe BiCMOS Technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Oct. 2007, pp. 46–49.