Single-Event Transients in Bipolar Linear Integrated Circuits

Stephen Buchner, *Member, IEEE*, and Dale McMorrow, *Member, IEEE*

***Abstract*—Single-event transients (SETs) in linear integrated circuits have caused anomalies in a number of spacecraft. The consequences of these anomalies have spurred efforts to better understand SETs, including the mechanisms responsible for their generation, the best approaches for testing, how data should be analyzed and presented, and approaches for mitigation.**

***Index Terms*—Heavy ions, linear circuits, pulsed laser, single-event transients (SETs).**

I. Introduction

SINGLE-EVENT TRANSIENTs (SETs) are voltage glitches that occur in integrated circuits (ICs) operating in a radiation environment. They are caused by ionizing particles passing through sensitive p-n junctions in the ICs. By their very nature, SETs are temporary, but they can lead to long-term effects if, for example, they corrupt instruction code in memory or trigger unwanted actions, such as power resets.

Generally, any device that uses charge to represent information is susceptible to SETs. That would include all silicon-based technologies (CMOS, bipolar, and BiCMOS) as well as all compound semiconductor technologies (MESFET and heterojunction). Both digital and analog circuits are susceptible to SETs, but there are sufficient differences to warrant treating them separately. SETs in digital circuits (DSETs) make their presence known when they are converted to single-event upsets (SEUs), such as when a SET changes the information stored in a register or memory. On the other hand, SETs in linear analog circuits (ASETs) originate at a sensitive p-n junction within the circuit, but they must first propagate to an output in order to be detected. ASETs generally have no long-term effects on the linear circuits in which they are generated. However, they can trigger long-term effects in follow-on circuits connected to the output of the struck circuit, with the type of effect depending on the function of the follow-on circuit.

Experience has taught us that ASETs pose a potentially serious threat to spacecraft operating in the radiation environment of space. It is well established that a number of system malfunctions on board spacecraft have been attributed to ASETs. The first occurred shortly after the launch of NASA's TOPEX/Poseidon satellite in 1992, when an anomaly occurred in an operational amplifier (OP15) that was part of the electronics for a scientific instrument [1]. Malfunctions on other spacecraft, including TDRS, CASSINI, [2] SOHO [3], [4], TERRA, and MAP [5], were also attributed to SETs. In most cases, the SETs caused the satellites to switch into "safe mode," in which all nonessential systems were temporarily powered down until the cause was identified.

This paper is devoted exclusively to the study of ASETs in linear bipolar devices. It addresses all aspects of ASET generation and propagation, with special emphasis on the application of a variety of different experimental methods and computer simulations to reveal ASETs properties.

II. Background

Spacecraft contain many different types of linear ICs including operational amplifiers (op-amps), voltage comparators, voltage references, pulsewidth modulators, voltage-controlled oscillators, dc/dc converters, etc., all of which may be ASET sensitive. Only operational amplifiers and voltage comparators will be discussed in detail here because most of the ASET studies to date have been devoted to these two types of linear circuits.

Many factors determine whether ASETs pose a threat to a spacecraft. They include the function of the linear IC, the type of ion, the location within the IC of the ion strike, device and circuit parameters, device configuration (input and supply biases), and output impedance. Factors such as the incident ion type and energy, the ion strike location and the parameters of the struck transistor determine the initial ASET size. Circuit parameters then determine whether the ASET is able to propagate from the strike location to the IC output.

After propagating through an IC and appearing at an output, an ASET must still propagate through the subsystem until it reaches a critical IC where it can trigger a change. The propagation is determined by the bandpass of the subsystem, and only sufficiently large ASETs will be able to switch the state. As a result, of the many ASETs produced with a variety of shapes and sizes, the number that will pose an actual threat to a system is quite small.

Op-amps are used in a wide variety of applications, including power-supply circuits where their outputs are routinely filtered to remove noise. Those same filters are also effective at removing ASETs, so that additional mitigation is not always necessary for power-supply circuits. However, in applications where the outputs of op-amps cannot be filtered, such as for high-speed measurements, ASETs present a very real problem for the circuit designer.

ASETs in op-amps have a variety of shapes and sizes. Fig. 1 shows examples of ASETs from a single device, the LM124

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S. Buchner is with QSS Group Inc., Lanham, MD 20772 USA (e-mail: sbuchner@pop500.gsfc.nasa.gov).

D. McMorrow is with the Naval Research Laboratory, Washington, DC 20375 USA (e-mail: mcmorrow@ccs.nrl.navy.mil).

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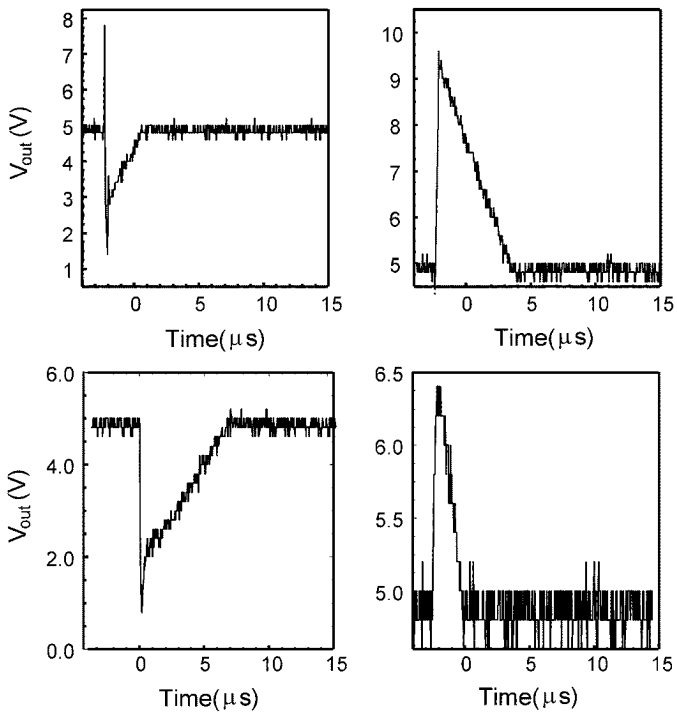

Fig. 1. Variety of ASETs produced in the LM124 operational amplifier by high-energy heavy-ion irradiation [6].

operational amplifier, configured as an inverting amplifier with gain [6]. Some ASETs are positive, some are negative, and some are bipolar. Some are of very short duration, while others are much longer. It is important to note that the operating configuration may determine ASET shape and sensitivity, so that ASETs captured for a specific set of operating conditions are not representative of those in other configurations.

Comparators are used in applications where their outputs have digital character (either high or low voltage). ASETs at the outputs of voltage comparators are less complex as they are unipolar and all have approximately the same shape, i.e., their widths are proportional to their amplitudes. The sizes and sensitivities of the ASETs also depend on the operating conditions, particularly the differential input voltage, which, if sufficiently large, can greatly reduce the overall ASET sensitivity of a comparator.

Other types of linear circuits such as pulse width modulators (PWMs) and voltage-controlled oscillators (VCOs) have very different ASET signatures. Fig. 2 shows the two output signals of a PWM [7]. An ASET takes the form of a shortened pulse in one of the PWM's outputs, but by the next clock period, the PWM operates normally again. ASETs in PWMs may consist of dropped pulses, shortened pulses, or phase shifts.

Fig. 3 shows an ASET in a VCO. The ASET causes a temporary distortion in the output signal for a time that spans more than one clock period [8]. The temporary operational malfunctions in both the PWM and the VCO qualify as ASETs because they are caused by voltage transients induced by ions passing through sensitive transistor nodes in circuits. In each case, the device returned to its normal mode of operation at the end of the voltage disturbance.

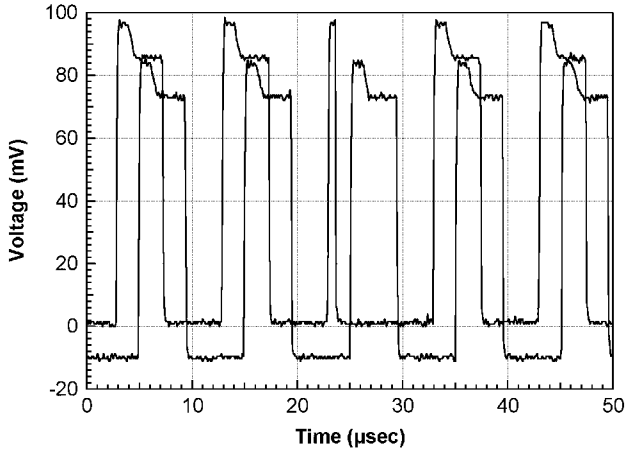

Fig. 2. Two pulse trains from a SG1525A pulsewidth-modulator showing a shortened positive pulse in one of the trains [7].

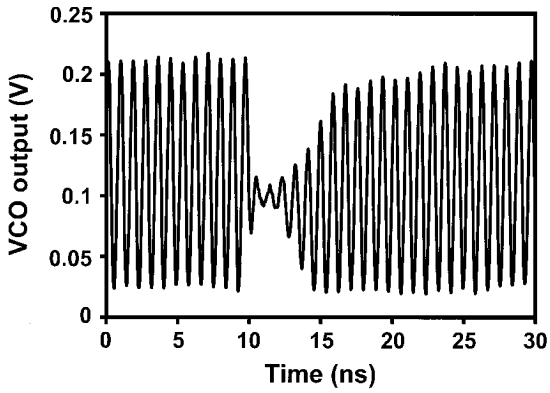

Fig. 3. Output voltage as a function of time for a voltage controlled oscillator. The ASET appears as a reduction in the amplitude that lasts for about 10 cycles [8].

There are several reasons why ASETs pose a serious threat to linear ICs operating in space. One is the low linear energy transfer (LET) threshold ($\sim$1 MeV·cm^2/mg) that prevails for some configurations, resulting in large numbers of heavy ions in space being capable of producing ASETs. Another is the combination of large amplitudes (rail-to-rail) and long durations (typically tens of microseconds, but some as long as milliseconds) that enhance the likelihood of an ASET propagating through a series of follow-on circuits before eventually becoming "latched." Finally, the low-energy threshold ($<$30 MeV) measured for proton-induced ASETs in some devices means that a large number of protons in space will be able to generate ASETs [9]. Since protons are by far the most abundant positive ion species, circuits sensitive to proton-induced ASETs will exhibit high rates in space.

III. ASET Propagation

Integrated circuits on board spacecraft are exposed to energetic positive ions with masses that span the periodic table from hydrogen to uranium. Most of those ions are capable of producing ASETs in ICs, a process consisting of a number of steps. The first step involves energy deposition by an ionizing particle that produces a track of charge (electrons and holes) through or near a p-n junction transistor node. The second step involves

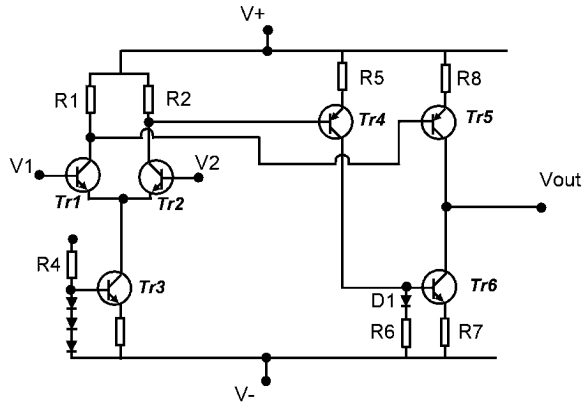

Fig. 4. Circuit elements for a simple operational amplifier consisting of six transistors [10].

separation of the charge by the electric field of the p-n junction. The charge separation alters the voltage at the transistor node by reducing the voltage in the n-type region and increasing it in the p-type region. The magnitude of the voltage disturbance depends on many factors, including ion (type and energy) transistor (doping levels, voltages, transistor size) and circuit (location of transistor in circuit). The third step involves the propagation of the ASET from its origin through the IC to the output.

Because the literature on single event effects contains numerous discussions on charge generation, charge collection, and transistor response, the mechanisms involved will not be discussed here. Instead, this review will concentrate on transient propagation through a simple op-amp. Fig. 4 shows a basic op-amp circuit with no feedback [10]. The input stage contains a differential amplifier consisting of a pair of identical n-p-n bipolar transistors whose emitters are connected to a constant current supply Tr3. In addition, $\mathrm{R}_5 = \mathrm{R}_6 = \mathrm{R}_7 = \mathrm{R}_8$ and all the transistors are assumed to have infinite gain, which means their base currents are zero.

For equal input voltages $(\mathrm{V}_1) = \mathrm{V}_2)$, the currents through R1 and R2 are equal, as are the voltage drops across R1 and R2. This leads to equal currents flowing through Tr4 and Tr5. With equal currents flowing through R_5 and R_6, the potential drops across R_5 and R_8 must be equal. The diode D1 ensures that the potential drop across R_7 is the same as across R_5, so that $\mathrm{V}_{\mathrm{out}}$ is midway between V+ and V−, i.e., $\mathrm{V}_{\mathrm{out}} = 0$ V.

An increase in V_1 causes an increase in I_1 and a reduction in I_2. The result is a reduction in the voltage at the base of Tr4 and an increase in the voltage at the base of Tr5. More current will flow through Tr5 and less through Tr6, which increases $\mathrm{V}_{\mathrm{out}}$. In fact, $\Delta\ \mathrm{V}_{\mathrm{out}}$ is proportional to $(\mathrm{V}_1 - \mathrm{V}_2)$. The same analysis shows that if V_2 increases relative to $\mathrm{V}_1, \Delta\mathrm{V}_{\mathrm{out}}$ will drop by an amount proportional to $(\mathrm{V}_2 - \mathrm{V}_1)$.

Based on the above analysis, it is relatively straightforward to explain how ASETs propagate to $\mathrm{V}_{\mathrm{out}}$ when charge is injected into either one of the input transistors. Charge injected into the C/B junction of Tr1 will cause the E/B junction to be slightly more forward biased. As a result, I_1 will increase and I_2 will decrease. An increase in I_1 increases the voltage drop across R_1 and a decrease in I_2 decreases the voltage drop across R_2. Both voltage transients will propagate through the op-amp, the positive transient to the base of transistor Tr4 and the negative transient to the base of Tr5. Tr5 becomes more conducting and Tr6 becomes less conducting. Together they cause the output voltage to drop. When the excess charge deposited in transistor Tr1 disappears, the voltage drops across R_1 and R_2 return to their original values and so do the voltages on the bases of Tr5 and Tr6. $\mathrm{V}_{\mathrm{out}}$ gradually recovers and the ASET disappears.

The analysis above is for ASETs originating in the differential input transistors of a very simple op-amp circuit. Some op-amps contain more than fifty transistors, many of which may be sensitive to ASETs. To determine which ones are in fact ASET sensitive may require the use of computer simulations or experimental investigations using pulsed laser light.

To prevent op-amps from going into spontaneous oscillation, compensating capacitors are added that reduce the op-amp's bandwidth. The inclusion of the capacitor, which functions as a low-pass filter, eliminates some fast ASETs and dampens others. For instance, although charge collection in the input transistor of the LM124 op-amp occurs over a time interval lasting hundreds of nanoseconds, the presence of the compensating capacitor dampens the ASET, which may last on the order of tens of microseconds.

The ASET response of a circuit cannot be calculated by simple linear analysis (output as a function of input) because the charge deposited by an ion at a sensitive transistor may be sufficient to drive the transistor out of its normal operating regime. To calculate the response, one is forced, instead, to use device and circuit simulator programs—an approach that will be discussed in more detail in Section V.

IV. Critical Charge

When applied to digital circuits, critical charge $(\mathrm{Q}_{\mathrm{crit}})$ is defined as the minimum amount of charge required for producing a SEU [11]. $\mathrm{Q}_{\mathrm{crit}}$ may be obtained experimentally by measuring the threshold LET $(\mathrm{LET}_{\mathrm{th}})$, provided the collection depth (d) is known. At threshold, $\mathrm{Q}_{\mathrm{crit}}$ equals the collected charge $(\mathrm{Q}_{\mathrm{col}})$, which, to a first approximation, is given by the product of $\mathrm{LET}_{\mathrm{th}}$ and d. Conversely, d may be obtained from the calculated Q_{crit} and the measured $\mathrm{LET}_{\mathrm{th}}$ through $\mathrm{Q}_{\mathrm{crit}}/\mathrm{LET}_{\mathrm{th}}$. This is important information for the experimentalist wishing to measure SEU cross section as a function of ion LET, because ions with sufficiently large energies must be selected so that the ion ranges exceed the charge collection depth, which may be quite large for devices where charge collection by diffusion is significant.

The concept of critical charge may also be applied to linear circuits. The value of $\mathrm{Q}_{\mathrm{crit}}$ is somewhat arbitrary for linear devices, since it must be related to a measurable quantity, such as ASET amplitude. Therefore, any definition of $\mathrm{Q}_{\mathrm{crit}}$ should include the criterion used for measuring it. $\mathrm{Q}_{\mathrm{crit}}$ may be defined as the minimum amount of charge required to produce an ASET of a given amplitude in a particular operating configuration. $\mathrm{Q}_{\mathrm{crit}}$ may also be defined with respect to a system application for which some minimum amount of charge must be collected to change a system.

Experiments have shown that the LET thresholds for some linear bipolar devices are very small—on the order of 1 MeV·cm^2/mg, which is equivalent to depositing 0.01 pC per micron [1]. Such a low LET begs the question as to whether the

cause is a small Q_{crit} and a small collection depth or a large Q_{crit} and a large collection depth. To answer this question, Q_{crit} was determined for two linear circuits—the LM111 voltage comparator and the LM124 op-amp—using a variety of experimental techniques [12]. Q_{crit} for the most sensitive transistor in each IC was also calculated from computer simulation. Results indicate that the critical charge is approximately 1 pC for both devices, which suggests that the collection depth is about 100 μm. Evidently, for these devices, charge is collected from well beyond the deepest junction, which is about 10 μm below the silicon surface. To measure ASET cross sections accurately requires that the ions have ranges on the order of 100 μm, a requirement that limits the choice of accelerators to those with high-energy ions.

V. ASET Simulation via Computer Modeling

Simulation is an important tool for studying ASETs. It requires the development of models to represent the devices (transistors, diodes, etc) in an IC. Once the model has been generated and validated, simulation may be used to obtain a great deal of information about ASETs difficult to obtain by other means. In particular, modifications to ASET shapes and sensitivities resulting from changes in design and manufacturing can be studied. Another potent application of simulation is to the explanation and evaluation of possible mitigation approaches for anomalous ASETs. It may also be used to determine whether ASETs generated in an IC, such as an operational amplifier or voltage comparator, will propagate through a variety of potential follow-on circuits that have not yet been assembled.

There are two approaches to computer simulation of ASETs. One combines a device simulator program with a circuit simulator program, and the other uses only a circuit simulator program. The latter approach, which may be used when the response time of the circuit is much slower than the charge collection time, is the approach of choice because it is much less computer intensive.

A. Device Simulation

Several commercial device simulator programs are available for investigating ASETs in linear ICs. A device simulator program solves the set of equations that governs the movement of charge in the device, i.e., Maxwell's equations, Poisson's equation, the continuity equations and the carrier transport equations. Because these equations cannot be solved analytically, the device simulator program is used to solve them numerically.

Once a transistor has been selected for modeling, a fine grid is overlaid on the transistor's structure. The equations governing the movement of charge are solved self consistently at each grid node, a time-consuming procedure. Information needed for the device simulator includes doping levels, geometrical layout, and thickness of the various layers, all of which must be obtained from the IC manufacturer or from reverse engineering. In addition, the injected charge profile is required. The movement of the charge (via drift and diffusion) and the responses of the terminal voltages are calculated as a function of time.

The device simulator may be combined with a circuit simulator to calculate how the circuit as a whole responds to the changes in voltages at the transistor terminals. This procedure must be repeated for charge tracks at various locations throughout the transistor, because the sizes and shapes of ASETs depend on ion strike location. Each transistor in the linear IC must be simulated in turn, a mammoth task when one considers that some ICs contain on the order of fifty transistors. It is, therefore, not surprising that, to date, there have been no published reports using this approach.

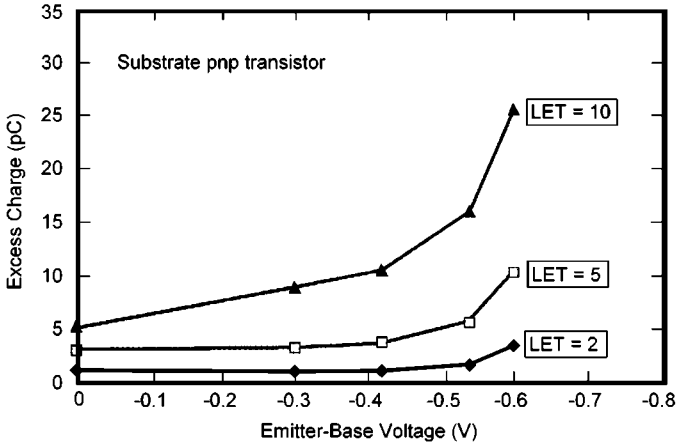

Fig. 5. Excess charge collected in the substrate p-n-p transistor as a function of emitter-base voltage for three different ion LETs [13].

Device simulators by themselves have been used to study charge collection processes in isolated transistors representative of those in voltage comparators and op-amps [13], [14]. Fig. 5 shows the excess charge (obtained by subtracting the dc current from the ion-induced current) at the collector of a vertical p-n-p transistor as a function of E/B voltage. The calculations are carried out for three different ions, each with a different LET [13]. With the E/B voltage near 0 V, the transistor is turned off. Deposited charge is not sufficient to turn the device on, so the amount of charge collected is proportional to the amount deposited.

As the E/B junction is more forward biased, the transistor begins to conduct current weakly. Any additional injected charge will further increase the forward bias leading to more charge being collected than deposited. The amplification effect increases as the bias becomes more negative, so that at a bias of -0.6 V the amplification is a maximum. Although not shown, the amplification decreases for more negative voltages, because the device begins to conduct a large amount of current.

B. Circuit Simulation

Circuit simulations require transistor libraries and a netlist for the IC. Transistor libraries contain all the needed parameters extracted from electrical measurements of individual transistors and a netlist describes how the transistors are interconnected. For proprietary reasons, IC vendors are reluctant to provide that type of information. One way to obtain the information is through reverse engineering, which involves isolating a transistor from the rest of the circuit by using ion-beam etching to sever all the connections [15]. Once a transistor has been isolated, contact to the terminals is made with mechanical probes

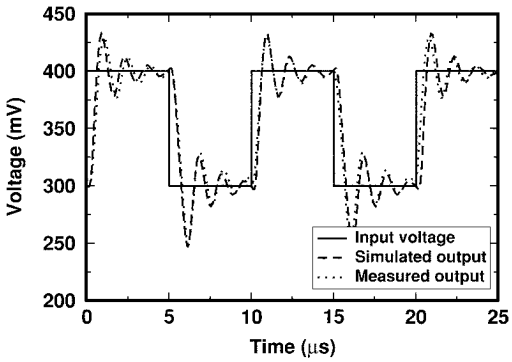

Fig. 6. Simulated and measured small-signal output waveforms for the LM124 when a square wave is applied to the input [15].

and the current-voltage characteristics are measured. The parameters needed for the Gummel-Poon model, as implemented in the circuit simulator program, SPICE, are obtained from the *I–V* transistor curves.

The first step to validate the model is to apply various input signals to an actual device and compare the output signals with those obtained by simulation. Both large and small signal inputs are necessary because ion strikes give rise to output disturbances with large nonlinear voltage swings (requiring large-signal inputs) and high-frequency components (requiring small-signal inputs) [15]. This approach was used for validating a model for the LM124 operational amplifier [15]. Fig. 6 shows the response for a small square-wave input signal. The excellent agreement confirms that the transistor parameters used in the model are accurate. Excellent agreement was also obtained for the large-signal response.

The next step is to check that the model generates valid ASETs. Just because the model accurately calculates the output response of an IC to a particular input does not mean that it will accurately reproduce ASET shapes, because some devices are forced out of their normal operating range by the deposited charge. Direct comparison between calculated ASETs and those generated by heavy ions is one way to establish the validity of the model. A broad beam of heavy ions is of little use because there is no way to identify the origin of a specific ASET. Instead, one may use a focused ion microbeam or a pulsed laser. The tool of choice is a pulsed laser because of the limitations of the ion microprobe (to be discussed in Section VI.C. Comparisons between simulated and laser-induced ASET pulse shapes may be used to assess the accuracy of the model. Additional tweaking of the model might be necessary to ensure that the calculated transients match the experimental ones. For example, many linear ICs contain parasitic elements that affect ASET shapes, but are not identified from reverse engineering. The pulsed laser may be used to identify parasitic elements for inclusion in the model.

Clearly, the development and validation of device and circuit models for an IC is a formidable task so that it is really only worth the effort if the IC is expected to find wide application in space. An example of a popular device used on spacecraft is the LM139 voltage comparator, which has been the subject of extensive modeling and experimental measurements.

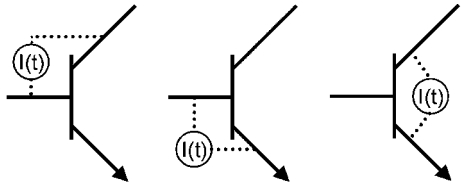

Fig. 7. Illustration showing the connections for a current generator across the collector/base, emitter/base, and emitter/collector junctions [16].

To mimic the charge deposited by an ion, ideal current sources are connected across the bipolar transistor junctions. Fig. 7 shows how the ideal current sources are connected. As long as the response time of the circuit is much greater than the time during which the charge is collected, the shape of the current pulse has no effect on the shape of the ASET. The only relevant variable is the total amount of injected charge obtained by integrating the current pulse over time [20]. The amount of charge injected at each junction is varied by adjusting the current pulse's amplitude or duration until it matches that of an experimentally obtained ASET. If they do not match, the circuit model might have to be changed by adjusting some of the Gummel-Poon parameters or by including parasitic elements that might have been missed during the initial attempt at building a model.

Modeling results have proved conclusively that the ASET shape is insensitive to the injected current profile, provided the total integrated charge remains constant and provided the circuit response is slower than the charge collection time [16]. Further confirmation that the time evolution of the current pulse has no effect on the shape of the ASET comes from the lack of any discernable differences between the shapes of ASETs calculated with SPICE and those generated by focusing a pulse of laser light on the same junction of the same device.

VI. Experimental Techniques for Measuring ASETs

Three different experimental approaches have been used for studying ASETs in analog ICs. They are unfocused and focused beams of ions from an accelerator and a focused beam of light from a pulsed laser. The application of all three techniques to the study of ASETs has proven enormously useful, providing comprehensive information that is not available from a single technique alone. This section will be devoted to describing each technique.

A. Accelerator Testing—Broad Beam of Heavy Ions

Accelerator testing is essential for predicting the event rate in space. The standard approach involves exposing an IC to a broad beam of heavy ions and counting the number of events and recording the particle fluence (ions/cm^2). The cross section is calculated by dividing the number of events by the fluence. This procedure is repeated for several different ions, each having a different LET.

An issue that must be considered when measuring ASET cross sections, particularly when the incident accelerator ions have low energies or are incident at large angles, is the ion

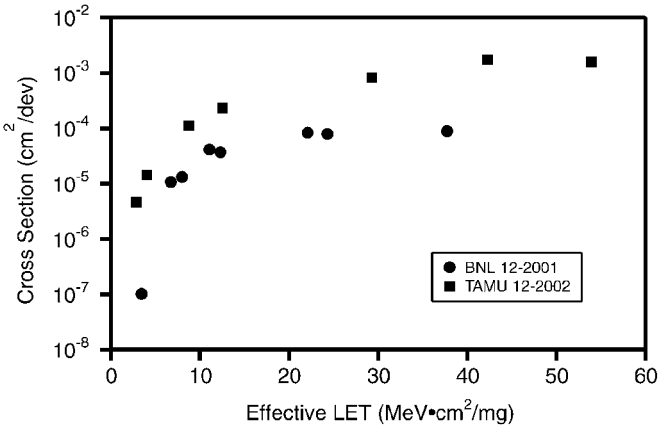

Fig. 8. Cross section as a function of ion LET for the LM124 op-amp. The part was configured as a voltage follower with $V_{in} = 5$ V. The measured cross section is larger for ions at TAMU than at BNL [17].

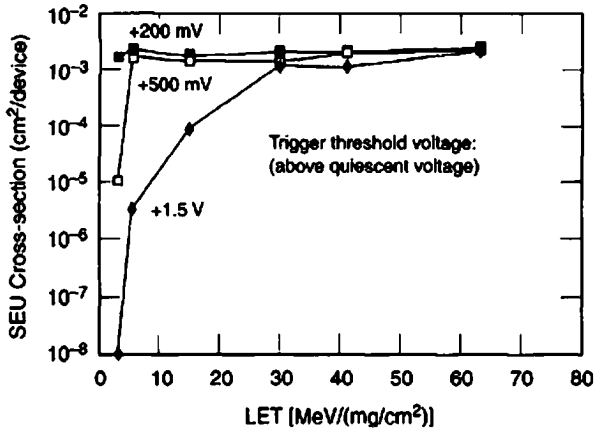

Fig. 9. ASET cross section as a function of ion LET for the OP-42 [1]. The figure clearly shows that as the trigger level is increased from 200 mV to 1.5 V, the LET threshold also increases.

range. Sensitive junctions in some bipolar transistors are quite deep ($\sim$10 μm below the surface) and additional charge collection by diffusion may take place from tens of microns beyond the junctions. In those cases, range cannot be ignored. For example, some SET data have been collected using I-127 with energy of 321 MeV. The LET at the surface of the device is 60 MeV·cm^2/mg, but the range is only 31 μm, which is not sufficient for those devices where a large amount of charge is collected by diffusion from depths approaching 100 μm. The result will be errors in the calculated ASET cross section.

Fig. 8 is a plot of σ (LET) for ASETs in the LM124 that reveals the role played by particle range [17]. The ASET cross sections measured at Brookhaven National Laboratory (BNL) are smaller than those measured at Texas A&M University Cyclotron Institute (TAMU) due to the lower energies and smaller ranges of the ions at BNL.

The unique nature of ASETs becomes evident when comparing the experimental approach used for measuring their cross section with that used for measuring the SEU cross- section of a memory. To test a memory for SEUs, a pattern of "1s" and "0s" is written to the memory. The memory is then exposed to a predetermined fluence of heavy ions or protons. After the exposure, the memory is read, the number of errors recorded, and the cross section calculated. Since ASETs appear as temporary disturbances at the output of a bipolar IC, the device itself does not record the number of disturbances. A counter must be connected to the device output to count and record the total number of ASETs. A counter with a fixed trigger level is of limited value because experiments have shown that σ (LET) depends on trigger level and it is unlikely that the chosen trigger level will match that for a particular application. Another approach uses a digital pulse-height analyzer with variable trigger level, which can be adjusted to match that of the intended application.

Fig. 9 shows how the ASET cross section for the OP-42 depends on trigger level. The experiments were repeated for different pulse height settings for the discriminator, a procedure that made it possible to replicate the different "decision" levels for circuits connected to the output of the OP-42. The figure shows the obvious result that an increase in the trigger level caused an increase in the LET threshold [1].

The best approach is to connect the output of the device under test (DUT) to a storage oscilloscope, which not only counts the number of ASETs but also stores the waveform for later analysis. The trigger level of the storage oscilloscope should be set to a relatively small voltage ($<$100 mV) in order to capture all the relevant transients. For a particular application, only those ASETs with amplitudes greater than the switching level need by considered. This type of analysis may be done after the conclusion of the experiment.

Merely counting the number of ASETs that exceed a specific decision level is not sufficient for calculating the ASET cross section because the bandwidth of the intended application limits the number of ASETs that are relevant. For example, none of the ASETs may cause a problem if the bandwidth of the application is sufficiently small. To calculate the cross section, it is necessary to count only those ASETs that exceed minimum values of amplitude and width as determined by the application's bandwidth.

Knowing the configuration of the device in the intended application is essential for calculating ASET cross sections. Configuration for an op-amp includes power-supply voltage, input voltage and output impedance. It also includes the external circuitry necessary for configuring a voltage follower or an amplifier with gain. Since ASET sensitivity has been shown to depend on all these factors, the device must be tested in a configuration identical to that of the application. The results are generally applicable only to that configuration.

The large variety of pulse shapes for ASETs generated in the LM124 operational amplifier was shown earlier in Fig. 1. In order to capture both positive and negative ASETs with a digital storage oscilloscope, two probes should be attached to the output of the device. Each probe is connected to a different channel on the oscilloscope. One channel is set to trigger on positive pulses and the other on negative pulses. Care must be taken when connecting the output of the device to the oscilloscope's input. Long cables will have sufficient capacitance to distort the ASET's shape, particularly very fast ASETs. To avoid this problem, active probes with very low capacitances ($<$10 pF) should be used.

Testing at some accelerators is only possible with the device located inside a vacuum chamber. BNC feed-throughs should be avoided because of their limited bandwidth. Instead, the active probes should be placed inside the vacuum chamber so that they can be connected directly to the output of the device. Special feed-throughs are necessary for the active probes. Most of these problems may be avoided by testing in air, which is possible at accelerators with high-energy ions.

When the test engineer cannot be close to the device under test due to radiation hazard, the oscilloscope and power supply should be located adjacent to the device and controlled remotely with a computer. Another option is to locate all the equipment outside the radiation chamber and use long cables to connect the DUT to the oscilloscope. Because the DUT generally does not have sufficient drive for the load imposed by the 50-ohm terminated BNC cable, the signal from the DUT should be connected to a high-speed buffer located adjacent to the output of the device. The high-speed buffer has sufficient drive to transmit an undistorted ASET to the oscilloscope.

An ASET test report should include all the test conditions so that others may determine whether the data are relevant to their application. For example, a test report for an operational amplifier should include information on the supply voltage, input voltage, configuration, gain, output loading, and oscilloscope trigger level, in addition to ion species, LET, flux, and fluence.

B. Accelerator Testing—Broad Beam of Protons

A device with a heavy-ion LET threshold below 15 MeV·cm^2/mg is considered so sensitive to SEEs that it may also be sensitive to proton-induced SEEs [18]. Therefore, linear devices, which have LET thresholds of approximately 1 MeV·cm^2/mg would, according to the above rule, be expected to be proton sensitive. However, as already pointed out, the LET threshold is small because the long charge collection depth partially compensates for the relatively large critical charge. Given the short range of the secondary particles generated in a nuclear interaction, it is certainly not a given that protons will produce transients in all linear devices.

The first linear device tested for ASET sensitivity to protons was the LM139 voltage comparator, which had a LET threshold of 2 MeV·cm^2/mg when the differential input voltage was 25 mV and the trigger level was 2 V [9]. To improve the chances of seeing ASETs with protons, the differential input voltage was reduced to 12.5 mV. Fig. 10 shows the measured cross sections as a function of proton energy for a trigger level of 2 V. Although there is some scatter in the data, the trend is unmistakable—as the proton energy increases, so does the cross section. The data also reveal a greater ASET cross section for negative values of differential input voltage than for positive values. Low-energy (30 MeV) protons produced smaller transients than high-energy (200 MeV) protons, and when the differential input voltage was increased to 25 mV, only 200-MeV protons produced ASETs greater than 2 V.

To calculate the ASET rate in space requires data from both heavy ion and proton experiments. In fact, in some cases the rate from protons will most likely dominate that from heavy-ions, so it is essential to do proton testing when, for example, the differential input voltage of a comparator is small.

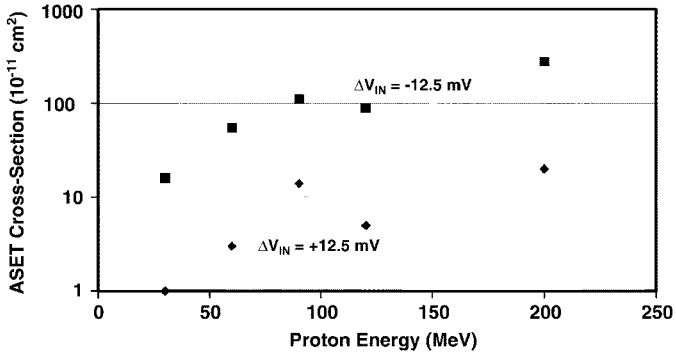

Fig. 10. ASET cross section for the LM139 as a function of proton energy for two different values of differential input voltage [9].

C. Accelerator Testing—Focused Ion Beam

The major drawback of broad-beam ion testing is the inability to obtain spatial information concerning the physical origins of the induced transients. That type of information can be enormously helpful in understanding anomalous behavior and in validating models used for computer simulation studies. A focused ion beam is an experimental method that provides information on the spatial origins of ASETs [19].

There are numerous microbeam facilities throughout the world, including Sandia National Laboratories (SNL) in the U.S. and Gesellschaft für Schwerionenforschung (GSI) in Germany. Unfortunately, this experimental technique has only rarely been used for investigating ASETs due to a number of reasons: limited accessibility to almost all facilities, the use of low-energy ions at some facilities that have small ranges in silicon, and the difficulty of changing ion species. Nevertheless, some useful results have been obtained with the microbeam.

The focused ion microbeam at SNL was used to study the origins of ASETs in the LM111 voltage comparator [20]. Both the utility and the limitations of the technique were evident from the results of this study. The usefulness of the ion microbeam technique was confirmed when it identified the base of a transistor in the differential input section of the LM111 as ASET sensitive, in contradiction to the results from SPICE modeling, which determined that the base was not sensitive. This lack of agreement was rectified when it was realized that the SPICE model failed to include the spreading resistance between the input and the base. The fact that the focused ion beam failed to identify other ASET-sensitive areas in the LM111 points to its major deficiency—the low energies and, therefore, short ranges of the ions in silicon.

D. Pulsed Laser Testing

Over the years, the pulsed picosecond laser has been successfully applied to the evaluation of single event effects in a number of different circuits and devices, including SRAMs, DRAMs, logic circuits, analog-to-digital converters, etc. [21]–[26]. It is in the area of ASETs, however, that the pulsed laser truly has come into its own. It has been unequivocally demonstrated for the devices investigated to date that the ASET shapes generated by pulsed laser light are *identical* to those generated by heavy

ions. The similarity of the pulse shapes suggests that the differences in the mechanisms responsible for free-carrier generation—Coulomb excitation for charged particles and light absorption for photons—are not important for the devices tested thus far.

One key factor that distinguishes the pulsed laser from a broad ion beam, apart from the physics of carrier generation, is the control over the location of the charge injection. By focusing the laser light to a spot with a diameter of approximately one micron and scanning the spot across the surface of the IC, information regarding the locations of ASETs as well as their pulse amplitudes and shapes can be obtained.

Several features of the pulsed laser technique have been used during the ASET studies reported herein. They include the ability to obtain spatial information without any concomitant radiation damage (total ionizing dose or displacement damage) to the device being tested, provided the light intensity is not excessive. Additional practical features of the technique are that testing may be performed in air, and it is a simple matter to adjust the "equivalent LET" merely by increasing or decreasing the laser pulse energy.

The laser approach has been used to extract a great deal of useful information regarding ASETs. For example, the information provided by the pulsed laser has proved vital for fine-tuning the models used to calculate ASET pulse shapes with computer programs such as SPICE [20]. Parasitic capacitances and resistances, not available from manufacturers' data sheets, have had to be included in the circuit models to ensure that calculated ASET pulse shapes matched those obtained experimentally [16]. The pulsed laser has also provided essential information regarding the location of anomalous ASETs, such as unusually long pulses observed in some circuits [27]. It has been used to study the effect of changing supply and input voltages as well as device configuration on the shapes and amplitudes of ASETs [28]. Finally, the pulsed laser has been used to determine whether a linear device is suitable, from an ASET point of view, for a specific application. This was done by measuring maximum amplitudes and widths of ASETs produced by scanning a laser beam across the surface of the linear IC. If none of the transients exceeded the minimum values required for being latched into a follow-on circuit, the device could be used [29].

The physical mechanism responsible for ASET generation in ICs with pulsed laser light is the excitation of electrons from the valence to the conduction band of the semiconductor by the absorption of photons. (This may be compared to the mechanisms responsible for ASET generation by particles where the excitation is the result of a Coulomb interaction between the nucleus of the incident particle and the bound electrons of the semiconductor material). The free carrier generation rate (dN/dt) is given by

$$\frac{dN(r,z)}{dt} = \frac{\alpha I(r,z)}{\hbar\omega} + \frac{\beta_2 I^2(r,z)}{2\hbar\omega} \tag{2}$$

where $I(r,z)$ is the pulse irradiance in W/cm^2 at a distance z from the surface and a radial distance r from the center of the track. N is the density of free carriers generated by the light, α is the linear absorption coefficient, β_2 is the two-photon absorption coefficient, which is the real part of χ^2, the second-order nonlinear-optical susceptibility, and $h\omega$ is the photon energy. Equation (2) includes both linear and nonlinear processes. The linear term governs one-photon absorption, and the quadratic term governs two-photon absorption.

To date, two different methods of charge injection using laser light have been developed for studying ASETs. The first, well-established approach involves single-photon absorption, which is governed by the first term in (2). The second, recently developed, relies on the nonlinear-optical process in which two subbandgap photons are absorbed simultaneously to generate a single electron-hole pair. Nonlinear absorption is governed by the second term in (2). The two processes may be prevented from interfering with each other by selecting the appropriate values of laser wavelength, pulse energy, and pulse width [30]. The photon energy, which is inversely proportional to wavelength, should be chosen to be greater than the bandgap of Si (1.1 eV) for linear absorption, and less than the bandgap for nonlinear (two-photon) absorption to be the dominant process. To obtain sufficient intensity for efficient carrier generation in the latter, an optical pulse of around 100 fs (or less) duration is focused to a spot of about one micrometer in diameter. This pulse length is a factor of 10 to 100 shorter than that typically used for single-photon absorption experiments.

The application of each method is described in detail later.

1) Linear Absorption: For photon energies larger than the bandgap of the semiconductor, α in (2) is greater than zero. At low light intensities, the first term on the right hand side of (2) dominates, and the light intensity $I(r,z)$ decays exponentially with distance z from the surface according to

$$I(r,z) = I_o e^{-\alpha z}. \tag{3}$$

The penetration depth (δ) is defined as the depth at which the intensity drops to $1/\mathrm{e}$ (37%) of its intensity at the surface and is given by the inverse of the absorption coefficient, which depends on the wavelength of the light. For example, the pulsed laser at the Naval Research Laboratory typically operates at a wavelength between 590 nm and 610 nm, and δ is approximately 1.8 μm in silicon [31]. The charge density along the track varies in the same way as the intensity given in (3). Fig. 11(a) shows the charge track produced in silicon by focusing a 590 nm optical pulse with a microscope objective lens [30]. The radial charge density ideally has a Gaussian shape whose profile is determined by the characteristics of the incident laser beam and the focusing power of the microscope objective lens. Fig. 11(b) illustrates the corresponding carrier density profile produced by 800 nm light under analogous conditions.

There are some issues regarding the pulsed laser technique that bear consideration. The first, and most obvious, is the presence of metallization that prevents the light from reaching some of the junctions. Fortunately, however, transistors in many linear devices have large surface areas devoid of metal, making it possible to probe almost all potentially sensitive areas with laser light. In those cases where metal does completely cover a sensitive area, two options remain. One is to focus the light onto a spot adjacent to the metal and increase the light intensity so

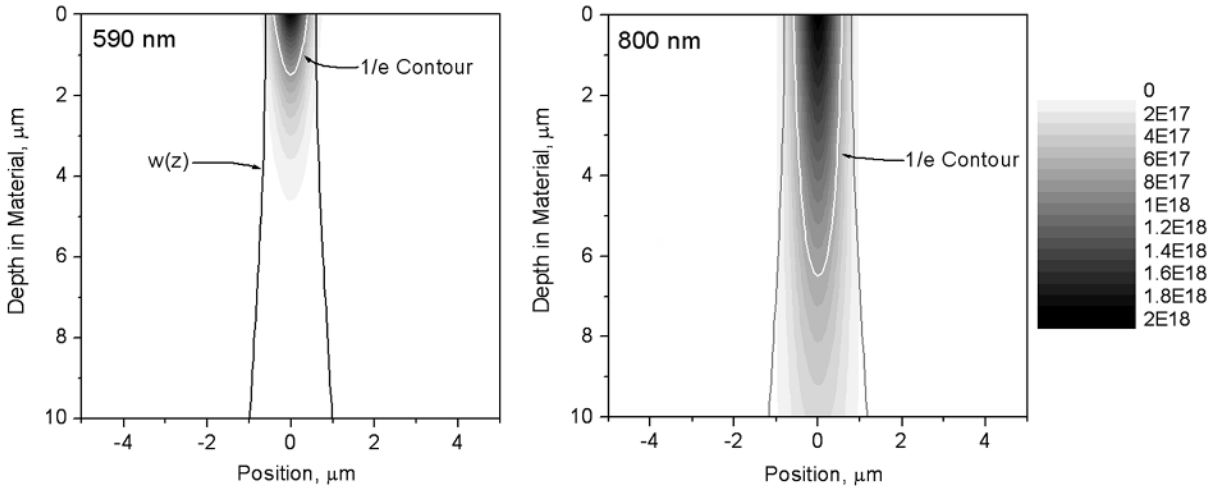

Fig. 11. Electron-hole density plot for (a) 590 nm and (b) 800 nm single-photon excitation processes in silicon as a function of depth in the material for a 1–ps pulse focused to a diameter having a full-width at half-maximum of 1.2 and 1.6 μm, respectively. The carrier density is plotted in electron-hole pairs/cm^3 [30].

that charge can diffuse under the metal to the sensitive region [21]. The impact of metal coverage of the sensitive nodes on the results was minimal in that case, and quantitative agreement with heavy ion measurements was achieved. Another approach, which is described in detail in the next section, is the use of subbandgap optical pulses that propagate through the wafer from the backside of the chip. The subbandgap laser pulse propagates unimpeded through the substrate until it reaches the focal point of the microscope objective lens, at which point it has sufficient intensity to generate carriers via the two-photon processes.

The second issue is the difference in the charge profile generated by heavy ions and laser light. Calculations have clearly demonstrated that, within a matter of a few picoseconds after the charge has been deposited, there are essentially no differences in the profiles produced by focused laser light and by heavy ions [32]. Therefore, this issue is of no concern.

Previous experiments have demonstrated that it is possible, in many cases, to relate the pulsed laser light energy needed to produce a SEU with the threshold LET measured with heavy ions [25], [33]. The method is purely empirical and found valid for a variety of devices, all of which have their junctions near the surface of the semiconductor. In contrast, analog devices frequently make use of different types of bipolar transistors (vertical n-p-n, substrate p-n-p, and lateral p-n-p) with junctions at different depths. The fact that the amount of light reaching two junctions at different depths will be different makes the direct comparison of their ASET sensitivities challenging.

The decisive test showing unequivocally that the pulsed laser faithfully reproduces ASETs was obtained by comparing ASET pulse shapes generated by laser light and heavy ions. Fig. 12 shows that the pulse shapes of the ASETs generated in the LM124 by these two methods are effectively identical [6]. Evidently, the charge deposition processes and details of the spatial profiles of the deposited charges play no role in determining the resultant ASET output pulse shape, provided the charge is deposited in a time shorter than the response time of the circuit. For the example of Fig. 12, after collection of the heavy-ion SET measurements, the unique signatures of the different nodes were identified using a 590–nm pulsed laser. To obtain the correspondence illustrated in Fig. 13, the laser pulse

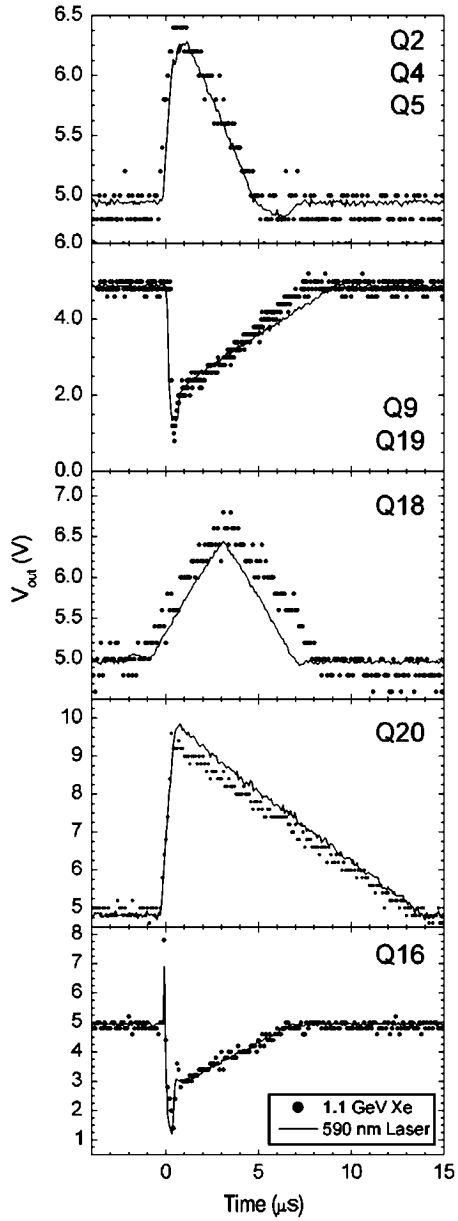

Fig. 12. Comparison of ASETs induced by a broad beam of heavy ions and 590 nm pulsed laser light [6].

energy was adjusted so that the ASET amplitude matched that of the heavy-ion transient for each node of interest.

The technique may be used to automatically scan the surface of ICs to map areas sensitive to ASETs. IXL Microelectronics Laboratory in Bordeaux, France, has developed such a laser scanning system [34]. The IC of interest is mounted on an x-y stage and a focused beam of light is directed at the IC surface. A computer controls the movement of the x-y stage. A complete scan of the IC is performed for a series of laser energies. During the scan, all ASETs are captured and stored on an oscilloscope and their locations noted. The data are used to construct contour plots of ASET amplitude or width. The contour plots are then superimposed on a photomicrograph of the chip to assist in identifying the origins of all ASETs. The software is sufficiently powerful that it can produce contour plots of any ASET characteristic of interest, such as pulse width, pulse amplitude, positive pulses, negative pulses, pulses larger than an arbitrary threshold, location of bipolar pulses, etc. Scans of localized areas are achieved by reducing the step size to 0.1 μm, whereas scans of the whole chip are more efficiently done with larger step sizes. Scanning the entire surface of an IC is the best way to begin a study of ASETs in the IC.

2) Nonlinear Absorption: The second method for injecting charge involves the nonlinear-optical process of two-photon absorption (TPA). The wavelength of the optical pulses is selected so that the individual photons have energies smaller than the bandgap of the semiconductor. In this case, α in (2) is effectively zero, and the light passes through the semiconductor unattenuated by linear absorption processes. However, as the pulse irradiance is increased, the second term in (2) becomes nonnegligible and electrons can be excited to the conduction band via the simultaneous absorption of two photons.

In practice, the laser pulse irradiance is increased by using a very short optical pulse ($\sim$100 fs) with high energy and focusing it to a small ($\sim$1 μm) spot. The free-carrier generation rate for TPA is proportional to the square of the laser pulse irradiance, as can be seen in (2). As already noted, TPA requires a laser system that has different characteristics from the one used for single-photon absorption; the photons must have energies less than 1.1 eV, the bandgap of silicon, and the pulses must be on the order of 100 fs or less.

Fig. 13 shows a first-order calculation illustrating carrier deposition profile for propagation of a sub-bandgap femtosecond optical pulse through intrinsic silicon under conditions optimized for efficient TPA [30]. As is evident, absorption only occurs near the focal region where the pulse irradiance is a maximum. The carrier profile produced by TPA has the shape of a "cigar" whose dimensions are determined by the confocal parameter of the incident laser beam, the focusing power of the lens, and the index of refraction of the material.

Using this approach, for which linear absorption processes are absent, the focal point, and hence, the location of the carrier generation, can be positioned at any depth below the surface of the IC by translating the device relative to the lens. Two advantages accrue from this approach. One is the ability to inject carriers in a localized volume at any depth below the surface to separate the contributions to ASETs from different junctions, so they may be studied independently.

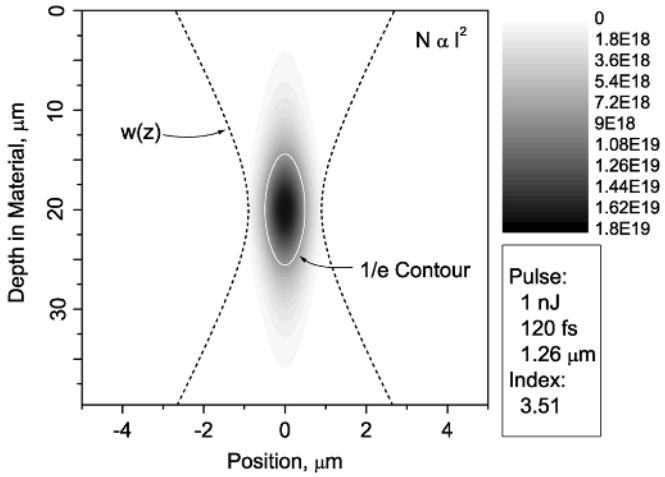

Fig. 13. Electron-hole density plot for the 2-photon excitation process in silicon as a function of depth (z). The laser light had a wavelength of 1.27 μm, an energy of 1 nJ, a pulse duration of 120 fs, and was focused to a diameter of 1.6 μm. The carrier density is plotted in electron-hole pairs/cm^3 [30].

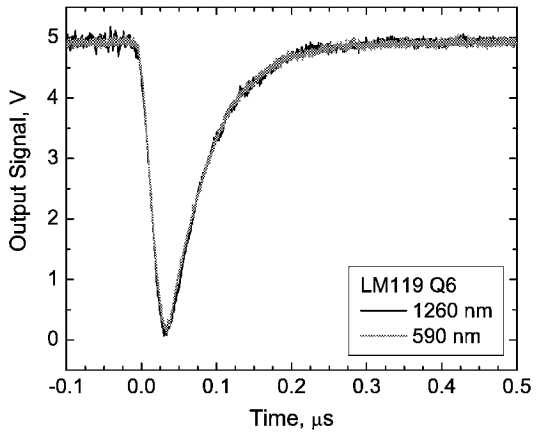

Fig. 14. Comparison of ASETs generated by one-photon and two-photon processes in the LM119. In both cases, the light was focused on the same spot on transistor Q6 [30].

The second is potentially more important in that it provides another option for ASET testing of devices that may be covered with metal or are packaged "face down." Access to the sensitive regions may be gained by directing the incident light through the wafer from the backside of the IC. Reservations about the utility of the pulsed laser technique arising from the presence of metal layers on the surface of the IC that would prevent the laser light from reaching sensitive junctions are allayed by backside probing.

The one situation in which the two-photon technique requires additional processing is for the case of highly doped ($>10^{18}$ cm^{-3}) silicon substrates. When the free-carrier density in the semiconductor is sufficiently high, the incident optical pulse is attenuated by free-carrier absorption [35]. This impacts both the optical pulse propagation through the wafer, and the imaging capability of the experiment. In this case, it is necessary to thin the device by removing most of the substrate material, an approach that has been demonstrated recently [36].

The two-photon method for producing ASETs was first validated by comparing the ASETs generated in the LM124 for one- and two-photon absorption processes. Fig. 14 shows that

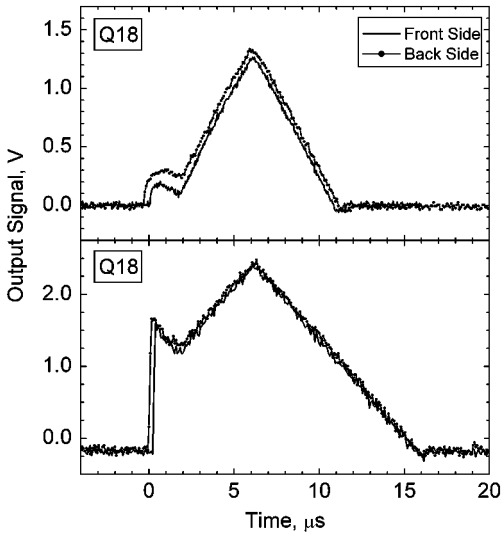

Fig. 15. Transients obtained from two-photon absorption at two different locations on transistor Q18 of the LM124 op-amp. The dark lines are for light incident from the front side and the grey lines are for light incident from the backside. No adjustment of the light intensity was made [30].

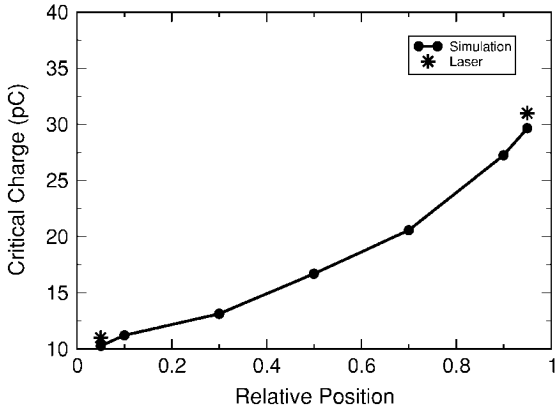

Fig. 16. Critical charge calculated for ASETs produced in the LM119 voltage comparator (solid line). The two data points were obtained with a pulsed laser [16].

the transients generated via two-photon absorption are identical to those generated via one-photon absorption. Fig. 15 illustrates that, for topside illumination, there is no difference in the ASET pulse shapes generated by the two approaches [30]. Validation of the through-wafer approach was performed by comparing ASET pulse shapes generated by front-side and backside illumination at identical locations in a number of transistors in the LM124 operational amplifier. Fig. 15 shows that there is no difference in the ASET shapes, or in the amount of energy needed to produce equivalent ASET pulses for light incident from the top-side of the chip, or for optical pulses that propagate through the unthinned wafer from the back of the IC [30]. The minor differences between the two data sets are not significant, and are associated with uncertainties in the laser spot location.

VII. Case Studies

Earlier, the pulsed laser was presented as a convenient laboratory tool for studying ASETs because analog ICs may be evaluated for ASET sensitivity with a minimum of delay and a maximum of convenience. The ability to focus the light on a specific transistor junction is essential for identifying the sources of anomalous ASET responses. Since linear devices can be used in a large number of different operating configurations (gain, output load) and voltages (supply and input), it is impractical to perform accelerator testing for all possible conditions. By supplementing conventional accelerator testing with pulsed laser testing and circuit simulation, the full spectrum of ASET responses and sensitivities can be investigated and characterized. What follows is a brief overview of some examples for which the pulsed laser and/or circuit simulations have proven invaluable in unraveling the complex ASET response of some linear ICs.

A. Dependence of ASETs on Circuit Parasitic Elements

This section will describe briefly how focused laser light was used to identify specific areas in linear ICs that were not originally known to be ASET sensitive. In fact, in the cases outlined here, sensitive areas were first identified by scanning the focused laser light across the entire surface of the IC and noting where ASETs were generated. Knowing which transistors are sensitive is enormously important for interpreting the results of broad-beam heavy-ion tests and for improving the accuracy and completeness of the device models used for simulation.

The first example is that of the LM119 high-speed voltage comparator [16]. A laser scanned across the surface of the die revealed an unexpected result: SETs were produced when the laser spot was focused on some internal resistors. Closer examination revealed that the resistors were long narrow p-type structures formed in n-wells. It was first assumed that the light absorbed in the p-type resistor led to an increase in the number of free carriers, which caused an increase in conductivity. Such an increase in conductivity could, in theory, cause an ASET, but the fact that the ASET amplitude depended on the position of the charge injection along the resistor's length, ruled out conductivity modulation as the sole mechanism responsible for ASET production.

An alternate mechanism was proposed to explain this effect: injected charge was separated by the resistor/substrate p-n junction. The charge-separation effect was modeled by replacing a single resistor with two resistors in series, and adjusting their resistances in proportion to their relative lengths. A diode connected to V_{dd} was added to the circuit to simulate the junction, with a current generator across the diode to simulate the charge injection. Fig. 16 shows excellent agreement between the charge required to produce an ASET using computer simulation and that measured by charge injection using a pulsed laser. This analysis would not have been possible without the detailed spatial information provided by the pulsed laser interrogation. Another study affirmed the accuracy of the SPICE model used for simulating the ASETs is the LM119.

In a second example, pulsed laser SET measurements proved essential in the development of an accurate SPICE model for the current source used for the LM111 voltage comparator [20]. The pulsed laser identified the C/B junction of an input transistor (Q2) as the area most sensitive to ASETs for the bias configuration under consideration. To simulate an ASET in SPICE, a current source was connected across the C/B junction of Q2. However, the base of Q2 in the test configuration is connected

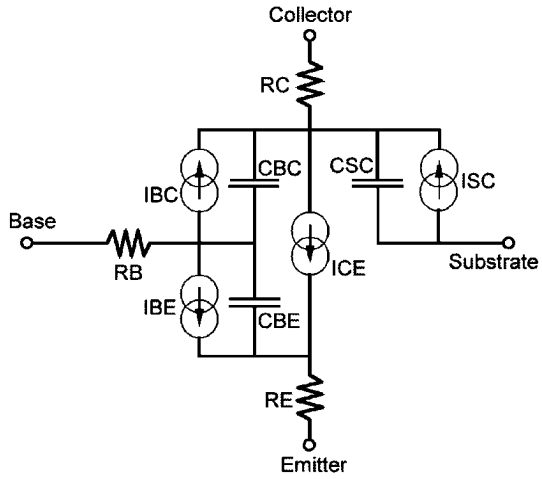

Fig. 17. Parasitic elements included in the SPICE model of a simple p-n-p transistor that formed the input transistor in the LM111 voltage comparator [20].

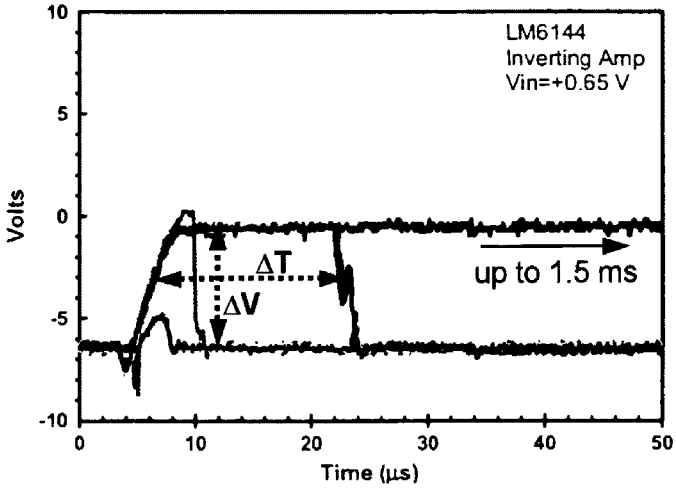

Fig. 18. LDPs observed for the LM6144 exposed to a beam of heavy ions [27].

to ground such that any injected current would flow directly to ground and not disturb any voltages across the transistor. To accurately reproduce the experimental results it was necessary to include a spreading resistance (RB) between the base and the input contact.

Fig. 17 shows how RB was included in the model. The Gummel-Poon compact SPICE model includes resistances for the emitter, base, and collector internal to the model, but the ASETs are produced by charge injected across the junctions and the current sources must be connected between the resistances and the internal nodes. With these modifications, the calculated ASET shapes and sensitive junctions agree with those measured with the pulsed laser.

The third example is that of the LM124 operational amplifier in which a device designated as a resistor in the manufacturer's schematic diagram was found to be one of the most sensitive locations for ASET production [20]. The ASETs originating in this "resistor" had large positive amplitudes with very narrow, almost square wave, characteristics and were unlike any other ASETs observed for the circuit. Identical ASETs were observed in heavy-ion experiments, but the pulsed laser was used to identify the resistor structure as the origin of the unique transients. This "resistor" is used as a biasing element in the gain stage of the amplifier. Following considerable physical analysis, it was determined that the resistor was fabricated as a floating-base transistor. Once the structure of the resistor was established, it was straightforward to understand its sensitivity to ASETs: any charge deposited in the "floating" base would cause a large change in the potential that could produce a transient that would propagate to the output of the device. Furthermore, once this information was understood, the floating base transistor was included in a circuit model that was more complete than that supplied by the manufacturer.

The examples cited demonstrate how the pulsed laser can play a key role in the development of accurate circuit models.

B. Long-Duration ASETs

It has long been recognized that the pulsed laser is a powerful tool for investigating the origins and mechanisms of anomalous SEEs. One particularly interesting and totally unexpected case was the occurrence of long-duration pulses (LDPs) in the LM6144 operational amplifier [27]. The LDPs were observed during heavy-ion testing at Texas A&M University Cyclotron, and it was the pulsed laser that helped identify the mechanisms responsible.

The LM6144 was configured as an inverter with gain (10 V/V) and $V_{cc} = -V_{ss} = 10$ V. With the input set at 625 mV, the dc output was -6.25 V. Fig. 18 shows the LDPs that occurred when the part was irradiated with heavy ions having LETs greater than 50 MeV·cm^2/mg. The longest ASET measured in the heavy-ion tests had a width of 1.5 ms, which is approximately two orders of magnitude longer than ASETs typically observed for similar op-amps. Of particular interest was the fact that the LDP amplitude saturated at 6 V, which is well short of the maximum possible amplitude (16.25 V) determined by the difference between the rail ($+10$ V) and the dc output (-6.25 V).

The pulsed laser was used to determine the origins of the LDPs by scanning the focused laser light across the IC surface and monitoring the output. A layout of the circuit, provided by the manufacturer, helped identify two n-p-n transistors as the sensitive nodes in question. The two transistors are part of a startup circuit whose function is to force the bias circuit into a particular state so that the op-amp will assume a stable operating state when power is first applied.

Fig. 19 shows the response of the circuit to a laser pulse focused on one of the two transistors. For this test the configuration of the part was the same as used during the heavy-ion testing except that the input was set at -60 mV instead of $+650$ mV. Therefore, the dc output was at $+0.6$ V. The ASET amplitude was -0.6 V and the duration 25 ms.

A detailed study was undertaken to unravel the processes associated with the occurrence of LDPs in this device. It was noticed that background light had a major effect on the duration of the pulse—the LDP persisted as long as any background light was present. Numerous sources of background light bedevil the experiment. They include: the light bulb used to illuminate the surface of the chip when positioning the laser pulse on the area

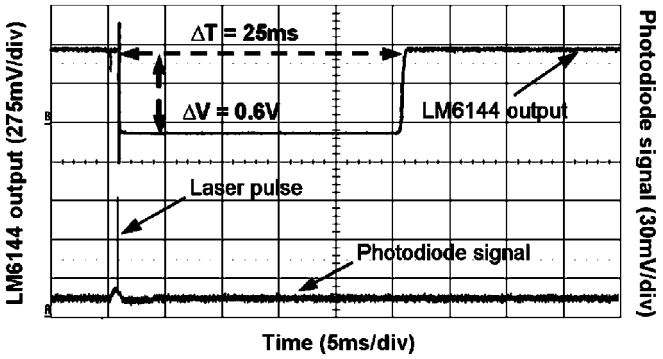

Fig. 19. Two oscilloscope traces, one displaying the signal from the photodiode monitoring the light emission by the pulsed laser (lower trace) and the other displaying the ASET that appeared at the output of the LM6144 [27].

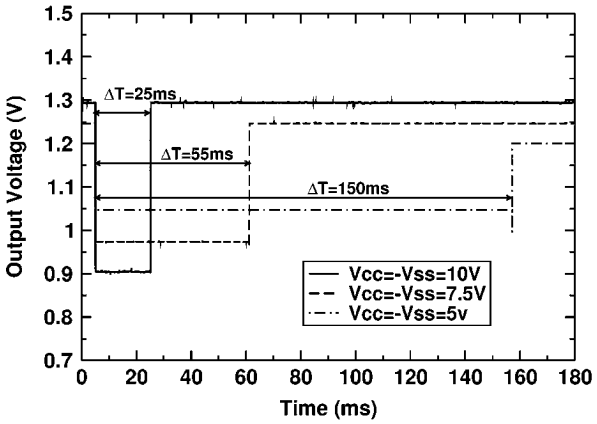

Fig. 20. Simulation results for the effect of power supply voltage on the width and amplitude of the LDPs. As the power supply voltage is increased, the recovery of the LM6144 is speeded up and the transients become shorter while their amplitudes increase [27].

of interest; the room lights; and the noncoherent or scattered light emitted by the laser (the scattered light provides a constant, low-level background collinear with the coherent laser beam).

Another phenomenon discovered with the laser was that once a LDP was generated in the presence of background light, it could be removed with a laser pulse directed at a transistor outside the initially sensitive area. This important finding helped explain some of the heavy-ion data. During heavy-ion testing, the delidded part was exposed to light from an ionization gauge used to measure the vacuum level of the beam line. It is believed, though not conclusively demonstrated, that the intensity of the light from the ionization gauge was sufficient to cause LDPs to persist indefinitely. However, once generated by an ion strike in the sensitive region, the LDP could be switched off by another strike in the surrounding circuit. It is believed that the varying lengths of the LDPs measured in the heavy-ion tests are a consequence of the random arrival times of the individual ions exiting the accelerator.

Pulsed-laser testing in the absence of background light revealed that, as the power supply voltage was reduced, the recovery time increased. Fig. 20 shows that, when the supply voltages were set at ± 10 V, the LDP width was 25 ms, at ± 7.5 V, it was 55 ms, and at ± 5 V, it was 150 ms.

The presence of LDPs may be explained by noting that there are two different stable operating states for the bias circuit, and that injection of charge onto either one of the two n-p-n transistors in the startup circuit causes the bias circuit to switch into a stable state different from the one it entered when power was first applied. A change in the bias circuit affects many transistors throughout the op-amp, and the result is a change in the op-amp's output. As long as even a small amount of charge is continuously being injected into either one of the two n-p-n transistors by background light, the bias circuit remains in the wrong state. Removal of all external sources of light allows the circuit to return to its preferred operating state.

The role of the bias/startup circuit was revealed by computer simulation. All the observed effects mentioned above were simulated. For example, Fig. 20 shows the results of calculations of LDP-width for different supply voltages, and shows general agreement with the experimental results. Once the mechanism responsible for the LDPs was understood, a simple mitigation was devised—the addition of small capacitors across the base/collector junctions of the two NPN transistors eliminated the LDPs.

The realization that even relatively little background illumination can affect SEE generation means that special attention must be given to reducing all background light when performing either laser or heavy-ion testing.

C. ASETs in a Fast Voltage Comparator (LM119)

Mention has already been made of the fact that voltage comparators are used in many different configurations and that the ASET sensitivity depends on the actual configuration implemented. A detailed investigation of ASETs in the LM119 voltage comparator was undertaken with the pulsed laser to study how ASETs are affected by changes in operating conditions [28].

The ASET-sensitive transistors were identified by scanning the pulsed laser across the surface of the IC. Two different values of ΔV_{in} were used, i.e., ± 60 mV. Of the 22 transistors in the LM119, seven are ASET sensitive for $\Delta V_{in} = +60$ mV and eleven are sensitive for $\Delta V_{in} = -60$ mV. Three of them are sensitive in both configurations. For $\Delta V_{in} = +60$ mV, the most sensitive transistor is the output transistor (Q16), whereas for $\Delta V_{in} = -60$ mV, the most sensitive is the input transistor (Q1).

Simulation results for comparators have indicated that, for small values of ΔV_{in}, the transistor most sensitive to ASETs is the "off" transistor in the differential input pair. For the input transistor to dominate the ASET response of the LM119, ΔV_{in} must be less than $+60$ mV. For negative values of ΔV_{in}, the amplitude of the ASET generated at an input transistor shows little dependence on the differential input voltage.

The first accelerator tests of the LM119 indicate no dependence on ΔV_{in}, in agreement with the pulsed laser results [37]. However, subsequent pulsed laser testing at reduced values of ΔV_{in} revealed that the LM119 is, in fact, sensitive to ASETs, with the most sensitive transistor being the input transistor (Q2) [28]. Heavy-ion measurements later confirmed that the ASET sensitivity of the LM119 depends on ΔV_{in} when the trigger level was set at 50 mV or lower [18].

TABLE I
DEPENDENCE OF ASET CHARACTERISTICS ON SUPPLY VOLTAGES ($V_{dd} = -V_{ss}$) FOR THE LM119

Supply Voltages	5V	10V	15V
Leading Edge Fall Time (ns)	48	20	15
Trailing Edge Rise Time (ns)	220	220	220
Amplitude (V)	-5	-5.6	-6
Threshold (a.u.)	8	5	4

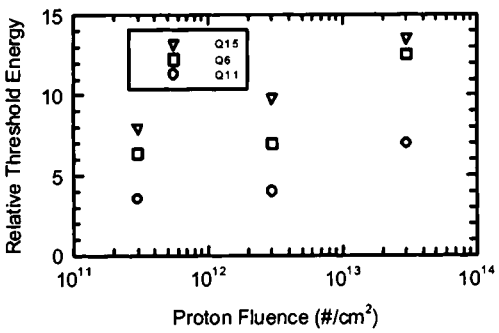

Fig. 21. Relative laser energies to produce the ASETs with the same amplitude for three different transistors (Q15, Q6, and Q11) as a function of proton fluence [28]. The highest fluence is equivalent to approximately 40 Mrad(Si).

Other ASET characteristics (rise time, fall time, amplitude and threshold) may be investigated with the pulsed laser. Table I lists the results obtained when transistor Q15, located close to the output, was irradiated. Since the differential input-voltage was positive, the dc output was at 5 V and transients appeared with negative amplitudes. Increasing the supply voltage caused the fall time of the leading edge to decrease, but it had no effect on the rise time of the trailing edge. The absence of an effect on the trailing edge is related to the open collector of the output transistor that is connected to V_{DD} through a "pull-up" resistor. The combination of the resistor and the capacitance of the large output resistor together determine the recovery time. Since neither of those two values changes as the supply voltage increases, the recovery time is constant. Notice that the amplitude of the negative-going pulse increased as the supply voltage increased, while the energy to produce the ASET decreased.

One LM119 was irradiated with 3-MeV protons to produce both ionizing and displacement damage. The effect of the damage on the energy threshold needed to produce an ASET was measured. With increasing damage, the amount of energy needed to produce an ASET also increased. Fig. 21 shows the dependence of the laser threshold energy for three different transistors of the LM119 as a function of proton fluence [28]. It is clear that the energy threshold increased with increasing proton fluence.

Finally, the effects of changing the value of the "pull-up" resistor on ASET shapes and thresholds were measured. A reduction in the value of the resistor by an order of magnitude (from 1.7 to 0.157 kOhm) had no effect on the leading edge fall time or the threshold, but the recovery time was reduced from 145 to 50 ns.

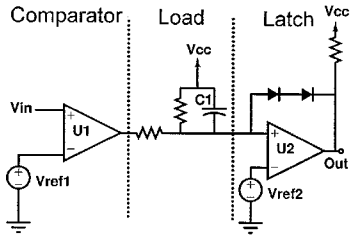

Fig. 22. Components used in an undervoltage detector. U1 and U2 are both LM111 voltage comparators [38].

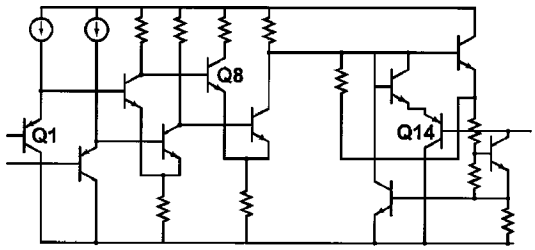

Fig. 23. Simplified circuit diagram of the LM111 op-amp. Q1, Q8, and Q14 were identified as the transistors most sensitive to ASETs. Macromodels were used to describe the rest of the circuit [38].

D. Application Dependence of ASETs

As was mentioned in the previous section, if a valid model for an IC is available, computer simulation may be used to study ASETs in ways that are sometimes difficult or impossible to do experimentally. For example, it is straightforward to use computer simulation to study the dependence of ASET shape and sensitivity on the values of internal resistors and capacitors. Another application would be the effect of the load on the ASET sensitivity. In fact, dramatic effects have been found when the load was only slightly altered.

The application chosen for analysis was an undervoltage detector incorporating the LM111 voltage comparator [38]. Fig. 22 shows the application, which includes a comparator, a load, and a latch. Under normal circumstances, the output of the circuit is high, but if the input voltage drops below a reference voltage (V_{ref1}), the output latches into a low state. Fig. 23 shows a simplified diagram of the LM111 using macromodels for parts of the circuit not sensitive to ASETs. Calculation revealed that the transistors most sensitive to ASETs were Q1, Q8, and Q14.

ASETs generated in U2 did not cause latching. Therefore, the study concentrated on ASETs generated in U1. The most significant result was that the identity of the transistor most sensitive to ASETs depended on the external application circuitry, in particular on the value of the capacitor (C1). For values of C1 up to 0.3 nF, Q1 was the most sensitive transistor. For values greater than 0.4 nF and less than 1.3 nF, Q8 was the most sensitive transistor, whereas for values greater than 1.2 nF, Q14 was the most sensitive. The study also found unexpected behavior of the critical charge with increasing capacitance, i.e., the critical charge for a single transistor increased slightly as the capacitance increased, but when the identity of the most sensitive transistor changed, the critical charge increased by orders of magnitude.

The implications of these calculations for laser testing are obvious: Since the identity of the transistor most sensitive to

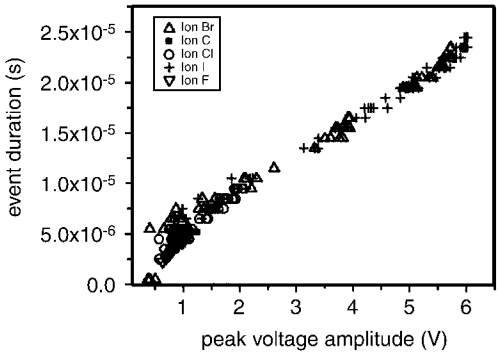

Fig. 24. ASET width as a function of amplitude for the LM124. The data points are for a variety of heavy ions spanning a wide range of LETs [39].

ASETs sometimes changes abruptly with small increases in capacitance, pulsed laser testing should not be confined to only one transistor. Instead, for each application, a scan of the entire IC must be undertaken to identify the most sensitive transistors for each application.

VIII. Data Presentation

The point has been made numerous times already that merely counting the number of events is not sufficient to characterize the ASET sensitivity of analog devices. What is needed in addition is specific information on pulse width and amplitude.

The best approach for doing ASET testing at accelerator, where the available time is severely limited, is to capture all the transients with a digital storage oscilloscope so that they may be analyzed once testing is complete. One is then faced with the prospect of having to analyze hundreds of transients with a variety of shapes and sizes. Only amplitude $(\Delta \mathrm{V})$ and width $(\Delta \mathrm{t})$ are needed to determine whether ASETs pose a problem for amplifiers and comparators. The fine details of the pulse shape are generally irrelevant. A convenient and compact way of presenting that information is needed. The first publication to address this issue suggested that plots of $\Delta \mathrm{V}$ versus $\Delta \mathrm{t}$ provide a useful way of presenting relevant ASET characteristics [39]. Fig. 24 is a plot of $\Delta \mathrm{V}$ versus $\Delta \mathrm{t}$ for the LM124 op-amp. The fact that all the data points fall on a straight line suggests the presence of only one type of ASET whose width increases in proportion to its amplitude. The method for displaying ASET characteristics described above was expanded upon in a subsequent publication. Fig. 25 is another plot of $\Delta \mathrm{V}$ versus $\Delta \mathrm{t}$ for the LM124. It includes data from many runs, each with a different ion LET [40]. For this case, both positive and negative pulses were included, and the different families of points reveal that ASETs from a single amplifier may have a variety of shapes. A point worth stressing is that the authors of the publication clearly identified the exact conditions under which the data were obtained. This is important because the distribution of points is not necessarily the same for different configurations.

Plots of $\Delta \mathrm{V}$ versus $\Delta \mathrm{t}$ are easily generated using a computer program that examines each pulse, measures its amplitude and width, and plots the data. Since some ASETs are bipolar, it is important that both positive and negative components of the transient are included.

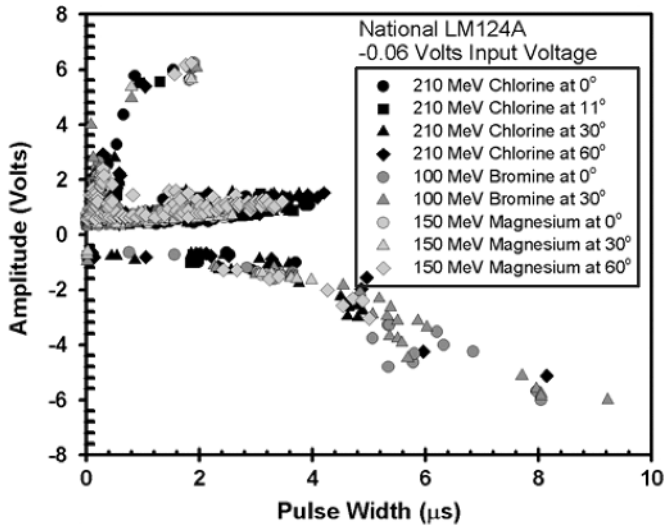

Fig. 25. Plot of amplitude versus width for the LM124 configured as a closed loop noninverting amplifier with gain (2X) [40]. Both positive and negative pulses were included.

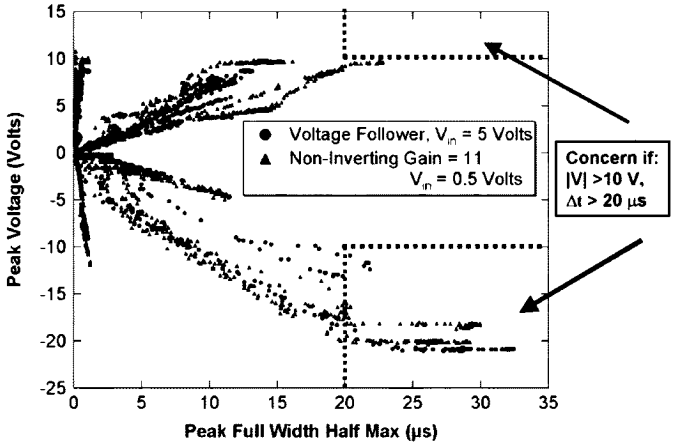

Fig. 26. Plot of amplitude versus width for ASETS originating in the LM124. When the LM124 is used in a particular application in which only those ASETs with amplitudes greater than 10 V and widths greater than 20 μs will propagate, the relevant phase space for propagation is indicated by the arrows, i.e., $|\Delta \mathrm{V}| > 10$ V, and $\Delta \mathrm{t} > 20$ μs [6].

The above analysis may be used to determine whether any of the ASETs pose a threat to a system containing the linear device being tested. The analysis involves determining the critical values of pulse amplitude $(\Delta V_{\mathrm{crit}})$ and width $(\Delta t_{\mathrm{crit}})$ for propagation through the system. Those values are included in the plots by drawing boundary lines that separate propagating ASETs from nonpropagating ASETs. The result is a "phase space" for ASETs whose shape varies depending on the device application.

Fig. 26 is a plot of $\Delta \mathrm{V}$ versus $\Delta \mathrm{t}$ for ASETs originating in the LM124 op-amp. For a particular application, the phase space for nonpropagating AESTs must be determined. In this example, only pulses with amplitudes greater than ± 10 V and widths longer than 20 μs can propagate [6]. The boundaries of the phase space separating propagating from nonpropagating ASETs are denoted by the dashed lines. To calculate the ASET cross section as a function of ion LET, this type of plot would

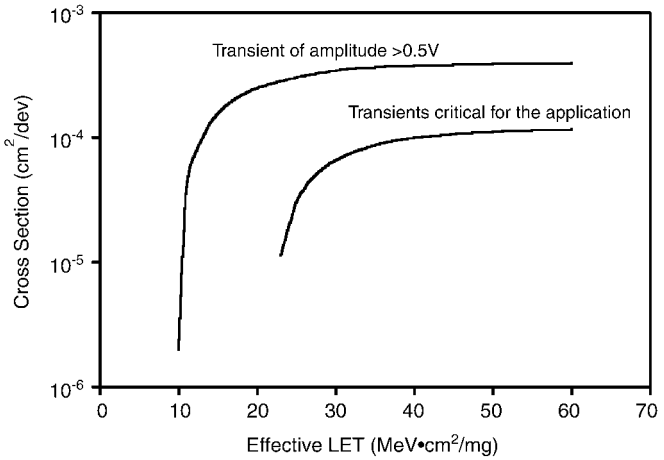

Fig. 27. ASET cross section as a function of ion LET for the LM139. The upper curve was obtained by counting all transients with amplitudes greater than 0.5 V. The lower curve was obtained by counting only those ASETs with amplitudes larger than 2.5 V [41]. The error rate calculated using the lower curve is approximately sixteen times smaller than if the upper curve had been used.

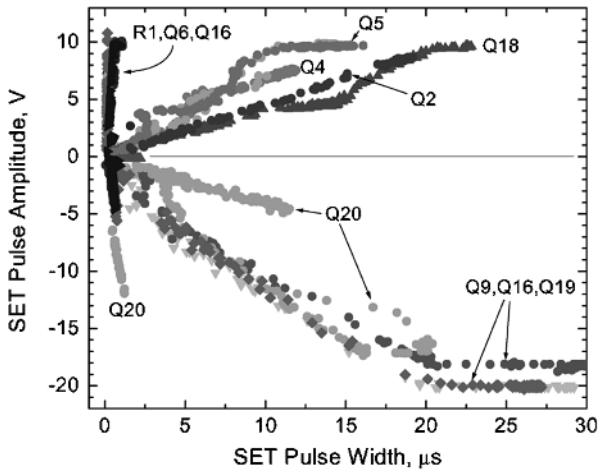

Fig. 28. Pulse amplitude versus pulse width for ASETs generated at various transistors in the LM124 op-amp obtained with a pulsed laser [6].

have to be generated for each ion LET and only points in the areas indicated by the arrows need by counted.

The next step is to plot σ (LET). The plot will depend on the application. Fig. 27 shows two plots for the PM139 voltage comparator manufactured by Analog Devices [46]. The differential input voltage was 1 V. The plot with the higher saturated cross section and lower LET threshold was obtained by counting all transients generated in the PM139 with amplitudes greater than 0.5 V. The second plot includes only those transients with amplitudes greater than 2.5 V that would produce resets in the processor. The saturated cross section in the second plot is a factor of four smaller than the first, and the LET threshold is a factor of two higher. One can use the figure-of-merit (FOM) approach to get a rough estimate of the change in the error rate. The error rate, given by the FOM, is proportional to the saturated cross section and inversely proportional to the square of the LET threshold [42]. Therefore, the actual error rate will be smaller by a factor of sixteen $(4 \times (2)^2)$ than the error rate calculated by counting all transients with amplitudes greater than 0.5 V.

The same kinds of plots may be generated using a pulsed laser. The laser light is focused on each sensitive transistor and all the ASETs are captured as the laser pulse energy is gradually increased. One has the option of plotting the data for a single transistor or for all the transistors in the IC. Fig. 28 shows the data points generated with the laser [6]. The usefulness of the laser data stems from the fact that, because the identity of each transistor in the IC is known, the source of each $(\Delta \mathrm{V}, \Delta \mathrm{t})$ point is known. A circuit designer can use this information to devise ways to harden the circuit.

The plots of $(\Delta \mathrm{V}, \Delta \mathrm{t})$ make it possible to compare directly ASETs produced by heavy ions and by laser light. All the data obtained from the two methods may be combined in a single plot to facilitate the comparison. The fact that the two sets of data overlap validates the approach of using the pulsed laser for hardness qualification discussed in a later section.

Presentation of ASET data is also a problem for those doing simulation. Large numbers of transients can be generated from computer simulations, and a compact and manageable way of presenting the data is necessary. All the information for ASET propagation in a system may be combined together into plots of $\Delta \mathrm{V}$ versus $\Delta \mathrm{t}$, just as was done for the data obtained from accelerator and pulsed-laser testing. The data from both simulation and experiments may be combined in a single $(\Delta \mathrm{V}, \Delta \mathrm{t})$ plot to assess the accuracy of the simulations

IX. Parameter Influence on ASETs in Operational Amplifiers and Voltage Comparators

This section introduces the reader to some of the unique aspects of ASETs in op-amps and voltage comparators.

A. Operational Amplifiers

Op-amps were among the first linear ICs tested for ASET sensitivity. It was recognized early on that op-amps contain multiple amplification stages capable of amplifying small voltage glitches in transistors located in input stages. By the time those glitches reach an output, they will have been magnified to such an extent that they may be able to induce errors in mixed-signal applications.

ASET amplitude and width are dependent on a number of factors, some internal and some external to the op-amp. These same factors also affect ASET sensitivity. In the next two subsections, external and internal factors will be considered.

1) External Factors: It seems reasonable to assume that ASETs will be affected by such external factors as operating configuration, supply voltage, input voltage, output load, and gain. Initial studies in a few op-amps indicate that some external factors have an effect and others do not. Additional studies are necessary in order to identify which factors are important, especially given the wide variety of op-amp designs available. The results presented in the following sections are for a small number of op-amps and are not meant to be definitive.

Device Configuration: Op-amps may be used in a number of different configurations, including voltage follower, inverter with gain and noninverter with gain. The LM124 was selected to determine whether changes in operating conditions affect ASET cross section. Fig. 29 shows the ASET cross section as

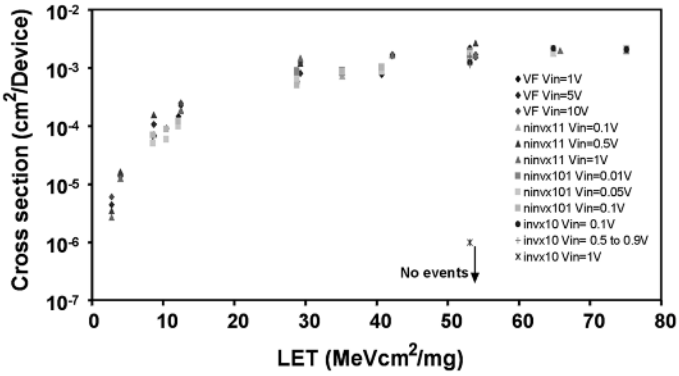

Fig. 29. ASET cross section as a function of ion LET for a number of different operating configurations and input voltages [41].

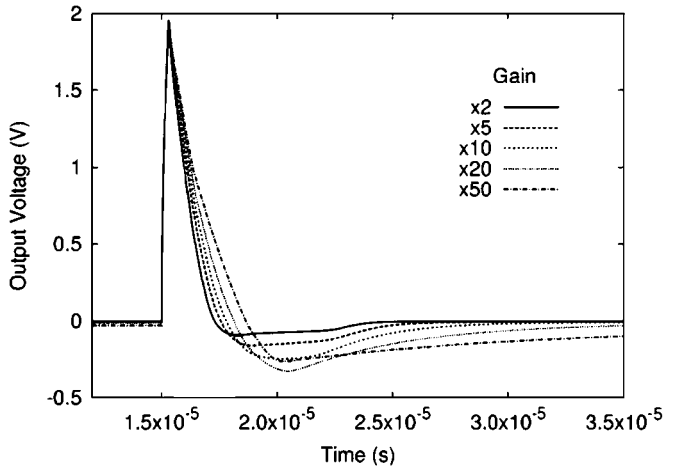

Fig. 30. Simulation of the effect of gain on the shape of an ASET generated at transistor Q14 in the output section of the LM124 op-amp [44].

a function of ion LET for three different configurations and for a variety of input bias conditions [41]. The figure surprisingly shows that the cross section is independent of configuration, supply voltage and input voltage. Unfortunately, it is impossible to draw any conclusions about the effects of different configurations on transient shape because the oscilloscope was set to trigger if the output deviated by ± 0.5 V from the dc level, regardless of ASET shape. If, in addition, ΔV versus Δt had been plotted for each configuration, one would be able to make a valid comparison. The data plotted in Fig. 30 imply only that the number of transients with amplitudes greater than 0.5 V is independent of operating configuration if the fluence and LET remain fixed. The ASET shapes may have changed, but the total number did not.

Confirmation that the ASET shapes for the LM124 were, in fact, unaffected by changes in operating conditions were obtained with a pulsed laser. The laser light was focused on the sensitive junction of a transistor in the LM124 configured as a voltage follower. The configuration was switched to that of an inverting amplifier with gain of ten without moving the device or changing the location or energy of the laser beam. No noticeable changes were observed in the ASET shape. In addition, the measured energy thresholds were also independent of configuration. The procedure was repeated for a number of different transistors in the LM124, and in each case, no obvious changes were detected. Not only did the pulsed laser confirm the data obtained with heavy ions, it also revealed that the ASET shapes were independent of configuration. Note that these results are for only two configurations, so they do not imply that this is universally true.

Power Supply Voltage: A unique aspect of operational amplifiers is that they are designed to operate over a wide range of power supply voltages. For example, the LM124 can be operated single-sided with 0 V and $+5$ V or with dual supplies of ± 15 V. Power supply affects ASETs in two ways. An increase in the power supply voltage causes an increase in $Q_{\rm crit}$, which makes the device less susceptible to ASETs. However, a larger power supply increases the available drive, which should magnify some of the smaller transients. Furthermore, a larger supply voltage permits ASETs with larger amplitudes because of the increased "overhead" between the dc output and the rail. A comprehensive study has not yet been undertaken to determine how supply voltage affects ASET shape or sensitivity.

Input Voltage: Fig. 29 suggests that input voltage has very little effect on cross section, i.e., $\rm LET_{th}$ and $\sigma_{\rm sat}$ (LET) appear to be independent of input voltage over a large range that extends from 0.01 V to 10 V. Because the cross section was determined by counting the total number of transients captured using an oscilloscope with a small trigger voltage, even large changes in ASET shape brought about by changing the configuration should have very little effect on the total number of ASETs and, thus, on the cross section.

Device input voltage may affect the magnitude of an ASET if the dc output level is close to a "rail". As an illustration, we consider the case of an amplifier with noninverting gain of two and voltage supply of 10 V. If the input signal is a dc voltage of 1 V, the output is at 2 V and the maximum amplitudes of positive and negative ASETs are $+8$ and -12 V, respectively. If the input signal is increased to 4 V, the maximum amplitudes are $+2$ and -18 V, respectively. For most ASETs, an increase in the amplitude is accompanied by an increase in the width. Therefore, in the example cited earlier, increasing the input signal level reduces the threat posed by positive ASETs to follow-on circuits, but increases the threat posed by negative ASETs.

Gain: An interesting and relevant question is whether gain affects ASETs. An attempt to answer this question involved an experiment to measure ASET cross section of the LM108 as a function of gain. The part was configured as an inverter with two different values of $\rm R_2/R_1$, i.e., -1 and -10. Gain was found to have no effect on the measured cross section. This is not surprising if the cross section is calculated by counting the number of ASETs captured with a fast oscilloscope set to trigger at a relatively low voltage [43].

The optimum method for studying how gain affects ASET shapes is computer simulation. Simulations were carried out for ASETs generated in the LM124 op-amp for different values of gain using a model validated with the results of pulsed-laser measurements. To ensure that the dc level would not affect the amplitude of the transients, the input was set to 0 V. The calculations were for ASETs generated in transistors located in the input, gain and output stages of the op-amp [44]. The largest effects were for transistors in the input stage where increasing

the gain from 2X to 50X caused a broadening of the transient from about 2.5 μs to 10 μs, a factor of about four. Transients originating in the gain exhibited a similar increase in width. However, transients originating in the output exhibited a much smaller increase. Fig. 30 shows that transient width increased from about 1 μs to 1.5 μs. The calculated transients for transistors in the input and gain stages showed very little change in shape as long as the gain increase was less than five. Larger increases caused proportionally greater increases in width. In all cases, changing the gain had no effect on the amplitudes of the transients.

The cross section depends on both the amplitude and width of the transient. Large increases in width caused by changing the configuration from one with a small gain to one with a large gain would require that the measurements be repeated.

Calculations were also performed to determine whether the transient shapes were affected by changing the values of the resistors R_1 and R_2, while keeping the gain $(\mathrm{R}_2/\mathrm{R}_1)$ fixed [44]. An increase in the values of resistors R_1 and R_2 caused a widening of the pulses generated at a transistor in the gain stage of the amplifier. Maximum width increases were a factor of two. Again, there was little effect on the amplitude. The explanation for the broadening of the transients with increasing gain in the LM124 has to do with the presence of a compensating capacitor that acts as a low-pass filter between in the input and gain stages. Increasing the gain means the bandwidth of the low-pass filter decreases resulting in a broadening of the pulses.

The above results explain why the measured cross sections did not depend on gain. Since only the width changed appreciably when the gain changed, the number of transients captured on an oscilloscope would not be expected to change. Whether gain is important for ASET cross sections for a particular configuration depends on the magnitude of gain. Very high values of gain will give rise to wide transients, and wide transients are more likely to cause upsets in mixed signal applications.

These findings are important because they serve to underscore the point that measurements of cross section as a function of ion LET are not sufficient to characterize an analog IC for ASET sensitivity. Transient amplitude and width are two criteria that should be used to judge whether ASETs could propagate through the subsystem of the intended application.

2) Internal Factors: Fig. 31 shows a simplified schematic of the LM124. Like most amplifiers, the LM124 consists of three stages—input, amplifier, and output stages. Resistors are added for negative feedback to obtain a stable output with a fixed gain determined by the values of the two resistors. An amplifier's internal gain and bandwidth also play a crucial role in determining ASET responses. Three transistors, one in each section of the amplifier, were selected as sources of ASETs to investigate how changes in the internal operating parameters affect ASET shape and sensitivity [44].

Compensating Capacitor: The LM124 contains a compensating capacitor between the input and gain stages to prevent oscillations [44]. Its value was found by physical analysis to equal 18 pF. The first transistor selected for investigation was Q4 in the input stage. By circuit simulation, an ideal current source was applied across the same junction as was irradiated with the pulsed laser. The amplitude and width of the current

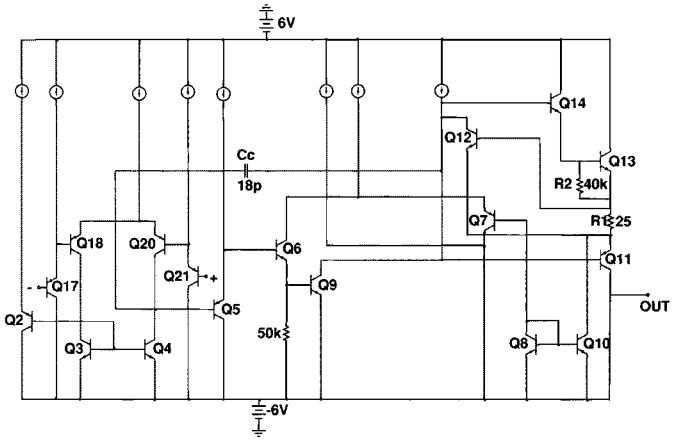

Fig. 31. Simplified circuit diagram for the LM124 [44].

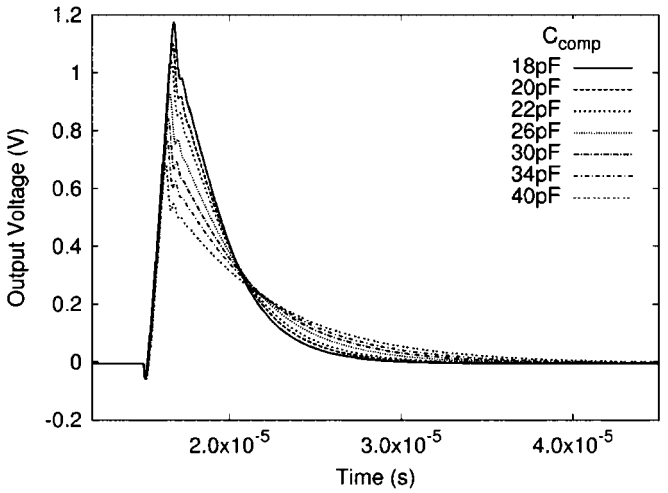

Fig. 32. Simulated ASET at transistor Q4 of the LM124. With increasing value of the compensating capacitor, the ASET's amplitude decreases and its width increases [44].

pulse were adjusted until the calculated ASET shape matched that obtained with the pulsed laser. Next, the size of the capacitor was increased in steps from 18 pF to 40 pF to determine how the ASET was affected. Fig. 32 shows that, with increasing capacitance, the ASET amplitude was reduced and the width increased. This is consistent with the gain and output sections acting as a low-pass filter with a cutoff frequency determined by the value of the capacitor.

The next transistor studied was Q9 in the gain stage. Fig. 33 shows how the shape of the ASET changes with capacitance. The ASET is complex with both fast and slow components. Changing the capacitance had no effect on the fast component, but did increase the recovery time for the slow component. The large amplitude produced by Q9 implies that it is the transistor most sensitive to ASETs.

The transistor in the output stage selected for investigation was Q14. The shape was not affected by changes in capacitance because it was beyond the influence of the capacitor.

The general conclusion from this work is that both internal and external factors affect the shape and sensitivity of ASETs.

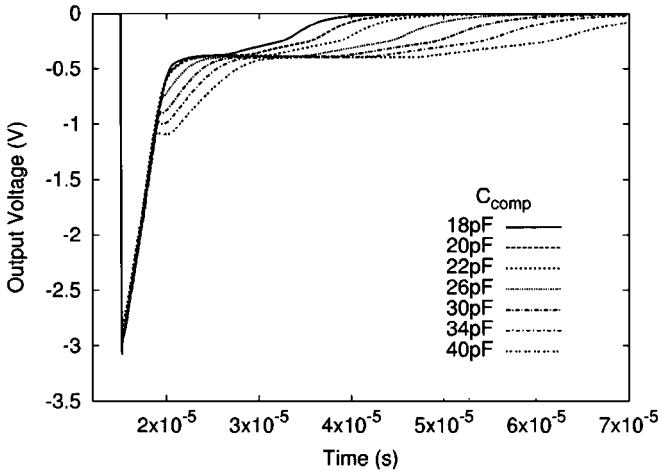

Fig. 33. Simulated ASET at transistor Q9 in the gain stage of the LM124. With increasing value of compensating capacitance, the ASET's width increases [44].

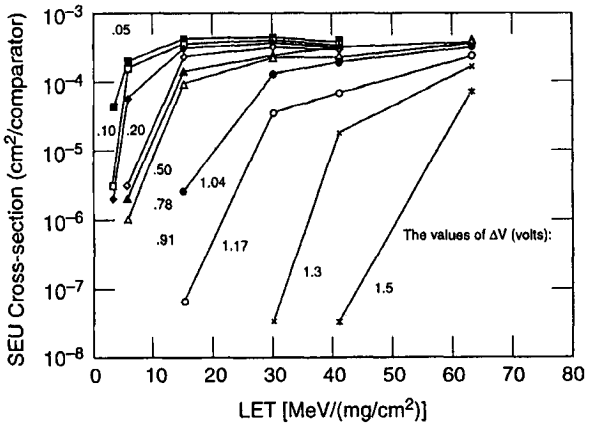

Fig. 34. ASET cross section as a function of ion LET for the LM139 for different values of ΔV_{in} [45].

Circuit simulation is the best way to determine what factors will affect ASET sensitivity.

B. Voltage Comparators

Voltage comparators are amplifiers without feedback. Their outputs are high for a positive value of differential input voltage $(\Delta V_{in} = V^+ - V^-)$ and low for a negative value. Analysis of experimental data points to the "off" input transistor as being the most AEST sensitive transistor. In fact, the ASET sensitivity of the comparator as a whole is largely dominated by that of the input transistor such that contributions from the rest of the circuit may be ignored.

Fig. 34 shows the dependence on ΔV_{in} for the LM139, a voltage comparator [45]. Increasing ΔV_{in} causes an increase in LET_{th} and a decrease in the saturated cross section. This behavior is consistent with a decrease in the sensitivity of the "off" transistor in the differential input pair as ΔV_{in} is increased.

X. Hardness Assurance and Qualification

The purpose of a hardness assurance (HA) program is to ensure that manufactured parts meet advertised levels of radiation hardness. That requires testing of a few parts from the latest production lot. When applied to transients, a HA program would require that a number of ICs (a minimum of three) be tested for their ASET sensitivity. It is impractical to do this at an accelerator because of limited access. However, a pulsed laser is ideally suited to monitor the ASET sensitivities of all the transistors in the ICs. It could be done by comparing the laser pulse energies needed to produce ASETs in ICs from the latest production lot with those from a reference lot that had previously been tested with both heavy-ions and a pulsed laser. Again, a minimum of three devices should be tested.

The pulsed laser could also be used to reduce the amount of heavy-ion testing needed to qualify parts. The process would involve collecting data on ΔV versus Δt for all ASETs [33]. Fig. 35 shows the steps involved.

The first step is to determine whether the part has previously been tested for ASETs *in the same operating configuration*. Data should include plots of σ (LET) together with complete waveforms for all the captured ASETs for each value of ion LET. These data may be used to generate plots of ΔV versus Δt as previously described.

In order to establish the minimum acceptable values of amplitude and width, it is necessary to consult a design engineer to determine the conditions under which ASETs will propagate through the system. There are two options, depending on the availability of ASET data.

A. No Heavy-Ion ASET Data Available

In the absence of ASET data, the first step would be to probe all the transistors on the chip using the laser to determine whether any of the ASETs lie outside the area in $\Delta V - \Delta t$ phase space defined by the threshold failure values of ΔV_{th} and Δt_{th}. If all the points lie inside the box, the part is deemed noncritical. To confirm that all SETs are within the area of nontransmission in $\Delta V - \Delta$ t phase space, accelerator testing can be done using only ions that result in the worst-case ASETs. If some of the ASETs are outside this window, a design engineer should be consulted to determine whether modifications could be made to the system to prevent ASET propagation. Such modifications may involve the addition of a filter, for example. If the modifications are possible, the device should still be tested for ASETs, but only with the highest LET ions, provided there are no bipolar transients that have been observed to decrease in width as the LET increases. If ASETs cannot be prevented, a complete characterization with heavy ions is necessary.

B. Heavy-Ion ASET Data Available

There are two possible courses of action when ASET data exist. One is for the case where the operating configuration is identical to the one of interest and examples of ASETs shapes are available. No further testing is required, and the decision on whether to accept the device is relatively straightforward. If the device meets all the requirements, it may be used as is. If it does not, either some form of mitigation must be used, or the part is deemed unacceptable.

A different course of action is required if the available data are for a different operating configuration. The first step is to scan all the transistors using the pulsed laser to determine maximum amplitude and width in order to determine whether any ASETs will propagate for the configuration of interest. If all the ASETs gen-

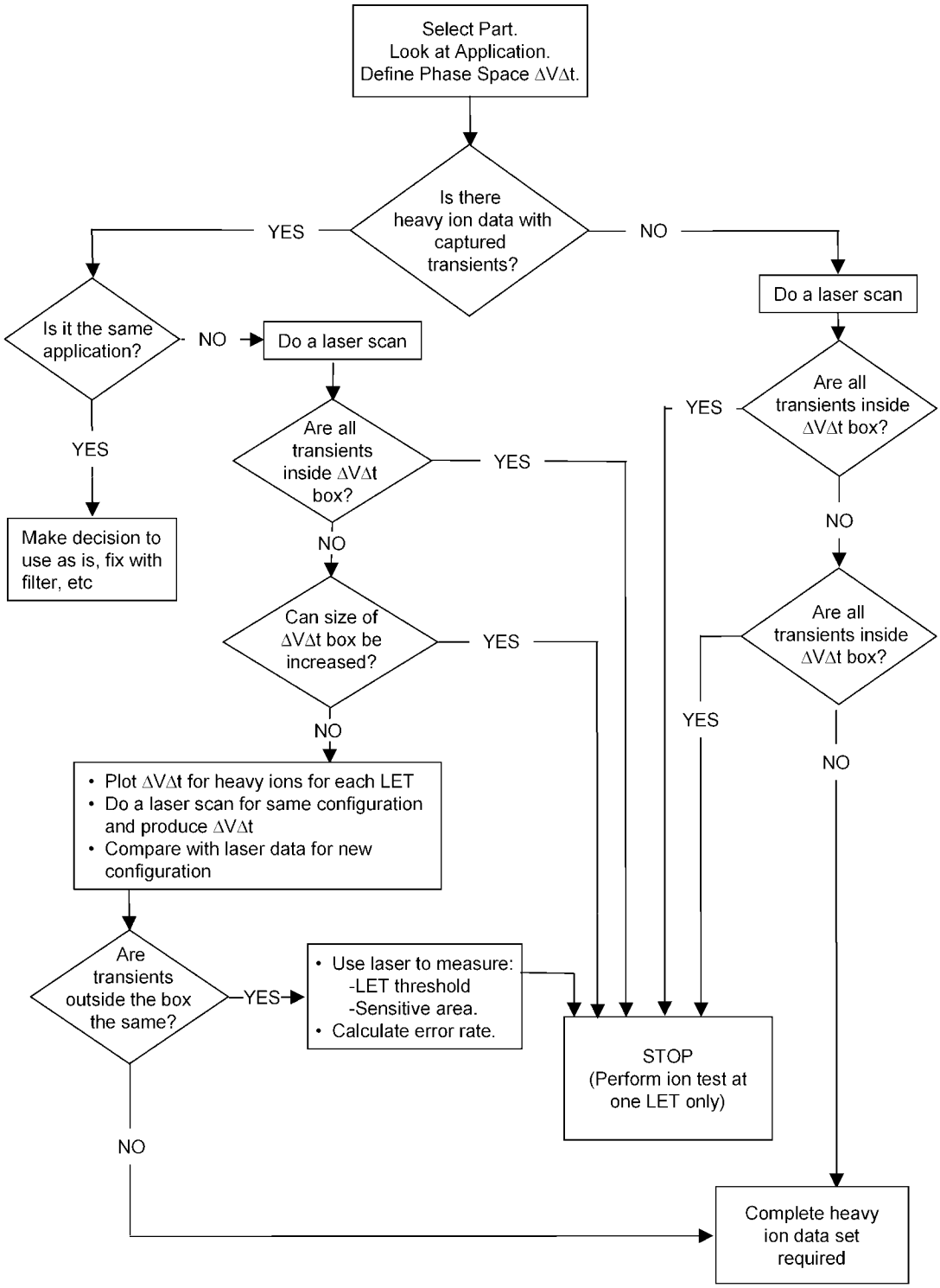

Fig. 35. Steps involved in using a pulsed laser to reduce the amount of ion-beam testing for a linear device [29].

erated by the pulsed laser have amplitudes and widths that are less than the threshold values for propagation, the part may be placed in the noncritical category. A limited accelerator test using ions that produce the worst case ASETs may be performed. If some of the measured transients have amplitudes and widths greater than the thresholds for propagation, the design engineer should be consulted to determine whether the propagation requirements on ΔV_{th} and/or Δt_{th} could be modified.

If the follow-on circuit cannot be modified to be tolerant of ASETs, a scan of all the transistors using the pulsed laser should be performed for the same configuration as for the heavy-ion data. The laser and ion data for the original configuration are then combined in a single plot of ΔV versus Δt and compared with a similar plot for the new configuration. If the loci of $(\Delta V, \Delta t)$ points are different for the two configurations, the laser cannot be used, and a complete heavy ion test must be done

to fully characterize the part. However, if the same transistors in both configurations are responsible for the $(\Delta V, \Delta t)$ points located beyond the minimum values for propagation, the pulsed laser can be used to obtain a rough measure of LET threshold and cross section for the new configuration.

The threshold is determined by calibrating the laser energy needed to produce an ASET in the new configuration against that in the old configuration. This is done by placing the laser light on the transistor responsible for the $(\Delta V, \Delta t)$ points just outside the box in the old configuration and measuring the pulse energy. The device is then set to the new configuration and the energy measured at that same transistor to produce a $(\Delta V, \Delta t)$ point just outside the box. Since the ion LET threshold for the old configuration is known, it can be calculated in the new configuration by taking the ratio of the laser energies and multiplying by the ion $\mathrm{LET_{th}}$ in the old configuration.

The saturated cross section may be obtained by increasing the laser energy and measuring the sensitive area surrounding every transistor that produces ASETs. (The increase in laser energy depends on the application, but is ultimately limited by physical damage due to excessive localized heating.) The sum of all the ASET sensitive areas gives a measure of the saturated SET cross section for that particular application. Previous results have demonstrated the validity of this approach [29].

The availability of linear devices hardened to the effects of ASETs would be of great interest to the aerospace industry. This could not be accomplished without implementing a HA program as described above, but the two main obstacles include the multitude of configurations in which op-amps are operated and the relatively small aerospace market that does not serve as an incentive to IC manufacturers. An alternate approach to a full-blown HA program is to use the pulsed laser in a judicious manner to screen parts for specific applications, as aforedescribed.

XI. ASET Mitigation

Most linear ICs are commercial-off-the-shelf (COTS) parts that are manufactured without regard to performance degradation by radiation. A few manufacturers do produce linear ICs that are designated "radiation hard" or "radiation tolerant," but those designations usually refer to the effects of total ionizing dose and not to ASETs. In fact, there are relatively few linear ICs available with immunity to ASETs, so the designer is forced to implement mitigation methods to eliminate or reduce the effects of ASETs on a system. ASET mitigation is achieved through modifications to the device, the circuit and the system.

A. ASET Mitigation at the Device Level

Hardening linear parts to ASETs at the device and circuit levels is the responsibility of circuit designers and manufacturers. There are two generally accepted ways of suppressing ASETs at the transistor level. The first is to increase the critical charge, $\mathrm{Q_{crit}}$. This approach has proved successful in SEU-hardened SRAMs, which incorporate resistors, capacitors or additional transistors in the feedback loop. In linear devices, increasing the size of a transistor and raising the supply voltage are two options. The second is to reduce the amount of collected charge $(\mathrm{Q_{col}})$ needed to produce an ASET. The widely accepted method for reducing $\mathrm{Q_{col}}$ is to use a very thin epitaxial silicon layer, such as silicon-on-insulator (SOI). The reduction in the collected charge will result in smaller ASETs with narrower widths.

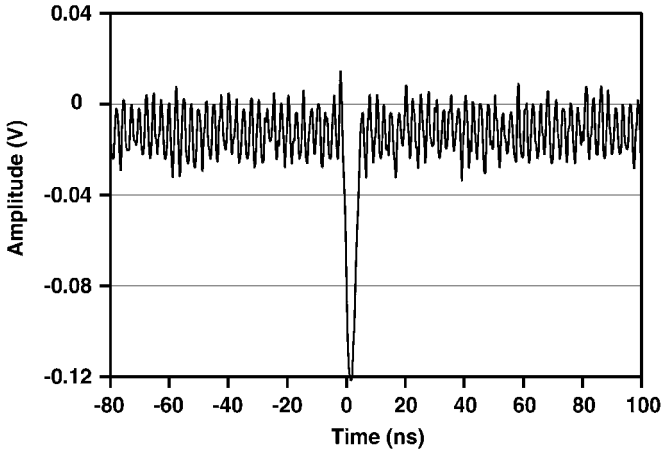

Fig. 36. ASET produced by pulsed laser light in the LMH6624 op-amp. The ASET amplitude is small (<120 mV) and of short duration (5 ns).

An example of a linear device manufactured in SOI is the LMH6624, an ultra low noise wideband (1.5 GHz) operational amplifier. Fig. 36 (unpublished data) illustrates the type of ASET produced in the LMH6624 with a pulsed laser. When the maximum laser pulse energy was used, the ASETs had amplitudes no greater than 0.3 V and widths of the order of 10 ns. A similar device, the LMH6702, was tested with heavy ions. Heavy ions having an LET of 96 MeV·cm^2/mg produced ASETs whose amplitudes were less than 400 mV and widths were approximately 20 ns. Depending on the application, these ASETs may or may not be of consequence.

B. ASET Mitigation at the Circuit Level

Another effective way of reducing ASET sensitivity is to reduce the part's bandwidth, thereby suppressing all the fast transients.

A different approach to circuit level hardening is to use triple modular redundancy (TMR). This approach was adopted for the IS-139ASRH, a hardened version of the widely used LM139 comparator [46]. The part was designed and manufactured using a triply redundant architecture, in which a single comparator was replaced with three parallel comparators. The three-comparator outputs drive a CMOS voting logic block that has been hardened to SETs by using oversized transistors. Fig. 37 shows a functional block diagram of the ASET hardened comparator.

The principle behind this hardening approach is that the majority voting logic produces an output that equals the state of two out of the three parallel comparators. If an ASET occurs in one of the comparators, the outputs of the other two will determine the output of the voting circuit, which will remain valid. The only way to get an erroneous output is for ASETs to be generated simultaneously in two or more of the comparators. Although this is highly unlikely, the probability is not zero, because an ion traveling at an oblique angle to the semiconductor surface could deposit sufficient charge in two adjacent comparators to cause an ASET in each one. In that case, two of the inputs

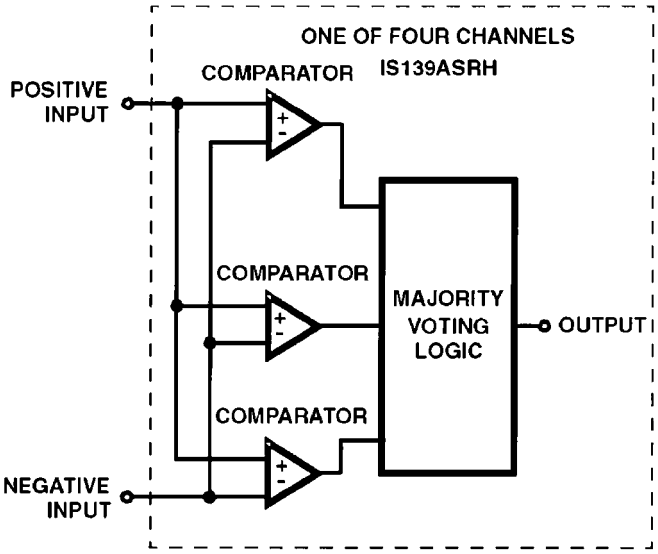

Fig. 37. Functional block diagram of the ASET-hardened IS-139ASRH voltage comparator [46].

to the voting logic would be in error, which would produce an ASET at the output.

To eliminate the possibility that an ion strike to a voltage reference would simultaneously affect all three redundant comparators, separate voltage references were used for each comparator. Replacing one comparator with three parallel redundant comparators has penalties, including an increase of 60% in the size of the silicon chip and a 50% increase in power.

Heavy-ion testing showed that, as long as the input overdrive voltage (ΔV_{in}) was relatively large (>1 V), the comparator operated as designed, i.e., no ASETs were observed for heavy-ion irradiation up to a LET of 83.9 MeV·cm^2/mg. However, when the overdrive voltage was reduced to the point where it became comparable to the input offset voltage (5 mV), ASETs would be generated. The maximum overdrive voltage at which ASETs occurred was 5.8 mV, which is 0.8 mV above the input offset voltage.

The explanation for this failure involves input capacitance and resistance. An ion strike to an input diode on the IS-139ASRH caused a voltage transient that induced a voltage drop across the input resistor. All the inputs to the redundant comparators are connected together, so that a voltage transient on the input resistor propagates to all three inputs. The result is an ASET on the output. The magnitude of the overdrive at which ASETs no longer occur depends on both the input resistance and capacitance. Fig. 38 shows how the minimum input overdrive for ASET-free operation depends on the input resistance for various values of input capacitance and supply voltage.

C. ASET Mitigation at the System Level

System mitigation can be very effective at reducing ASETs. A common approach is to add a low bandpass filter to suppress the propagation of fast ASETs. The value of the bandpass filter is determined by the system bandwidth. An example of an actual exercise in hardening is presented later.

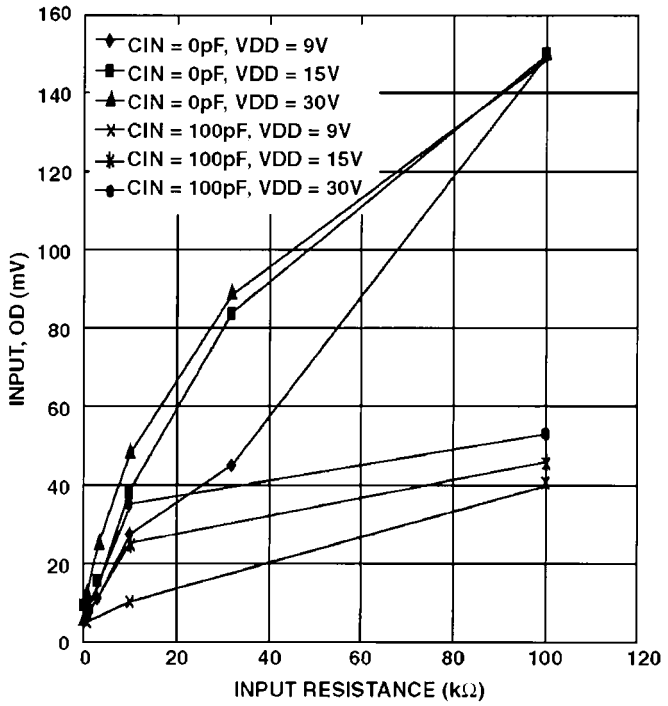

Fig. 38. Minimum input overdrive (ΔV_{in}) for SET-free operations as a function of input resistance, input capacitance, and supply voltage using Kr ions with an LET of 38 MeV·cm^2/mg [46].

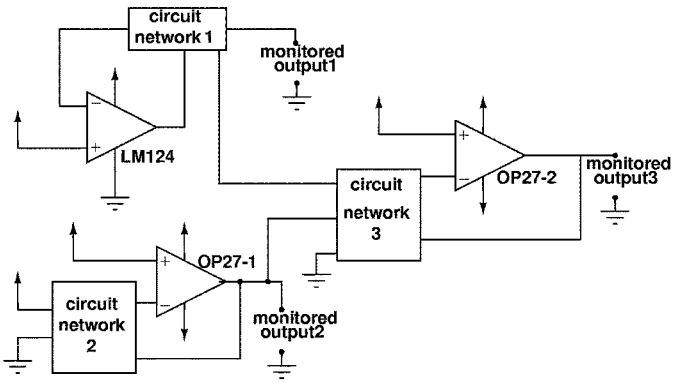

Fig. 39. Simplified circuit schematic of a specific application that contains two OP27's and one LM124 [47]. For proprietary reasons the other circuits are treated as black boxes.

Fig. 39 shows a circuit designed for controlling and monitoring the power distribution inside a spacecraft [47]. The part is designed to prevent a battery on board a spacecraft from being overcharged or undercharged. Analysis of the whole system determined that a system failure would occur if an ASET with amplitude greater than 1.8 V that lasts for more than 6 μs appeared at the circuit output (Monitored output 3).

Because of proprietary reasons, the details of the circuit were not revealed and were treated as "black boxes." The individual operational amplifiers were exposed to heavy ions and the ASETs produced were sampled at three different locations in the system. To validate the accuracy of the models used for computer simulation, "worst-case" ASETs were calculated both at the output of the IC being irradiated and at the system output (Output 3) and then compared with the actual ASETs obtained experimentally. Given the amount of work previously

done to model ASETs in the LM124 and the OP-27, it was not surprising that the calculated and measured ASET pulse shapes were essentially identical. It is important to note that this approach only works if the models have previously been validated by comparing calculated ASETs with those produced by heavy ions or pulsed-laser light.

Once the model for the whole circuit had been instantiated, ways of hardening the system were investigated. The restriction was that no new components could be added and the dc bias levels could not be changed. The first attempt at circuit hardening was to reduce the value of a resistor in "circuit network 1" from 1 kΩ to 100 Ω. The reduction in resistance strongly attenuated only the negative ASETs but not positive ones. Conversely, a reduction by an order of magnitude in the value of a resistor in "circuit network 2" attenuated positive ASETs but not negative ASETs. Finally, the values of two resistors in "circuit network 3" were reduced by a factor of five while keeping their ratio constant. The two resistors were in the feedback loop and a reduction in their values while keeping the ratio constant did not affect the gain. For this case, both positive and negative pulses were attenuated. The penalty associated with changing the resistor was an increase in power consumption by a factor of 3.5. This analysis shows how a combination of computer simulation, heavy-ion experiments and pulsed-laser experiments were used to harden a system to ASETs.

XII. Summary and Conclusions

This review has presented a detailed summary of our current level of understanding of ASETs in linear devices. To recapitulate, ASETs occur in all types of linear circuits and may take many different forms, from simple glitches in voltage comparators to missing pulses in pulse width modulators. The best way to study ASETs is to use a combination of circuit simulation and experiments (unfocused ion beam, focused ion beam and pulsed laser). Although circuit simulation requires a considerable investment of time, the rewards are great because it is possible to study factors affecting ASETs that cannot easily be studied experimentally. Testing with unfocused ion beams is necessary to obtain the ASET cross section as a function of ion LET. However, merely counting the number of ASETs is not adequate—an analysis of the waveforms is necessary to determine which transients actually pose a threat to a system. Only those that pose a threat are counted when calculating the cross section. The pulsed laser has proved to be a very useful technique for studying ASETs because of the spatial and temporal information it provides in a laboratory setting. Two-photon absorption makes it possible to produce ASETs by directing the light from the backside of a wafer, a novel approach that is still in its infancy. There are mitigation approaches that may be used successfully to reduce the threat posed by ASETs.

Finally, it is imperative to ensure that all linear devices intended for use in a spacecraft be checked for ASETs. Failure to do so could cause an unwanted anomaly that would jeopardize the successful completion of a mission.

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References

[1] R. Koga, S. D. Pinkerton, S. C. Moss, D. C. Mayer, S. Lalumondiere, S. J. Hansel, K. B. Crawford, and W. R. Crain, "Observation of single event upsets in analog microcircuits," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1838–1844, Dec. 1993.

[2] B. E. Pritchard, G. M. Swift, and A. H. Johnston, "Radiation effects, predicted, observed and compared for spacecraft systems," in *IEEE NSREC 2002 Data Workshop Proc.*, 2002, pp. 7–17.

[3] R. Harboe-Sorensen, F. X. Guerre, H. Constans, J. Van Dooren, G. Berger, and W. Hajdas, "Single event transient characterization of analog IC's for ESA's satellites," in *5th Europ. Conf. Radiation and Its Effects on Compon. Syst. (RADECS)*, France, Sep. 2000, pp. 573–581, Fontevraud.

[4] R. Harboe-Sorensen, E. Daly, F. Teston, H. Schweitzer, R. Nartallo, P. Perol, F. Vandenbussche, H. Dzitko, and J. Cretolle, "Observations and analysis of single event effects on-board the SOHO satellite," in *presented at 6th Europ. Conf. Radiation and Its Effects on Compon. Syst. (RADECS)*, Grenoble, France, Sep. 2001.

[5] C. Poivey, J. Barth, J. McCabe, and K. LaBel, "A space weather event on the microwave anisotropy probe (MAP)," in *presented at RADECS Workshop*, Padova, Italy, Sep. 2002.

[6] S. Buchner, D. McMorrow, C. Poivey, J. W. Howard, Jr., R. L. Pease, M. Savage, L. W. Massengill, and Y. Boulghassoul, "Comparison of single-event transients in an operational amplifier (LM124) by pulsed laser light and a broad beam of heavy ions," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, pp. 2776–2781, Oct. 2004.

[7] J. Howard, M. Carts, K. LaBel, J. Forney, and T. Irwin, "Single event effects testing of the linfinity SG1525A pulse width modulator controller," in *2003 IEEE Radiation Effects Data Workshop*, Monterey, CA, 2003, pp. 133–140.

[8] W. Chen, V. Pouget, H. Barnaby, J. Cressler, G. Niu, P. Fouillat, Y. Deval, and D. Lewis, "Investigation of single-event transients in voltage-controlled oscillators," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 2081–2087, Dec. 2003.

[9] D. K. Nichols, J. R. Coss, T. F. Miyahira, and H. R. Schwartz, "Heavy ion and proton induced single event transients in comparators," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 2960–2967, Dec. 1996.

[10] , [Online]. Available: http://www.st-andrews.ac.uk/~www_pa/Scots_Guide/audio/part8/Page1.html

[11] F. W. Sexton, "Measurement of single event phenomena in devices and ICs," in *IEEE NSREC Short Course*, New Orleans, LA, Jul. 13, 1992.

[12] R. Pease, A. Sternberg, L. Massengill, R. Schrimpf, S. Buchner, M. Savage, J. Titus, and T. Turflinger, "Critical charge for single-event transients (SETs) in bipolar linear circuits," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1966–1972, Dec. 2001.

[13] A. H. Johnston, G. M. Swift, T. F. Miyahira, and L. D. Edmonds, "A model for single event transients in comparators," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2624–2633, Dec. 2000.

[14] A. H. Johnston, T. F. Miyahira, L. D. Edmonds, and F. Irom, "Single-event transients in high-speed comparators," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3082–3089, Dec. 2002.

[15] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, R. L. Pease, S. Buchner, J. W. Howard, D. McMorrow, M. W. Savage, and C. Poivey, "Circuit modeling of the LM124 operational amplifier for analog single-event transient analysis," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3090–3096, Dec. 2002.

[16] A. L. Sternberg, L. W. Massengill, S. Buchner, R. L. Pease, Y. Boulghassoul, M. Savage, D. McMorrow, and R. A. Weller, "The role of parasitic elements in the single-event transient response of linear circuits," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3115–3120, Dec. 2002.

[17] C. Poivey, S. Buchner, J. Howard, K. LaBel, and R. Pease, Testing and hardness assurance guidelines for single event transients (SET) in linear devices Oct. 24, 2005 [Online]. Available: http://radhome.gsfc.nasa.gov/radhome/papers/SET_Linear05.pdf, NASA-GSFC Document

[18] E. L. Petersen, "The relationship of proton and heavy ion upset thresholds," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 6, pp. 1600–1604, Dec. 1992.

[19] F. W. Sexton, "Microbeam studies of single-event effects," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 687–694, Apr. 1996.

[20] R. Pease, A. Sternberg, Y. Boulghassoul, L. Massengill, S. Buchner, D. McMorrow, D. Walsh, G. Hash, S. Lalumondiere, and S. Moss, "Comparison of SETs in bipolar linear circuits generated with an ion microbeam, laser light and circuit simulation," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, Dec. 2002.

[21] S. Buchner, D. Wilson, K. Kang, D. Gill, J. A. Mazer, A. Petelin, W. D. Raburn, A. B. Campbell, and A. R. Knudson, "Laser simulation of single event upsets," *IEEE Trans. Nucl. Sci.*, vol. 34, no. 6, pp. 1228–1233, Dec. 1987.

[22] S. Buchner, K. Kang, W. J. Stapor, A. B. Campbell, A. R. Knudson, and S. Rivet, "Pulsed-laser induced seu in integrated circuits: A practical method for hardness assurance testing," *IEEE Trans. Nucl. Sci.*, vol. 37, no. 6, pp. 1825–1831, Dec. 1990.

[23] D. McMorrow, J. S. Melinger, N. Thantu, A. B. Campbell, T. R. Weatherford, A. R. Knudson, L. H. Tran, and A. Peczalski, "Charge-collection mechanchisms of heterostructure FETs," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, pp. 2055–2061, Dec. 1994.

[24] J. S. Melinger, S. Buchner, D. McMorrow, W. J. Stapor, T. R. Weatherford, A. B. Campbell, and H. Eisen, "Critical evaluation of the pulsed laser method for single event effects testing and fundamental studies," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, pp. 2574–2584, Dec. 1994.

[25] S. C. Moss, S. D. LaLumondiere, J. R. Scarpulla, K. P. MacWilliams, W. R. Crain, and R. Koga, "Correlation of picosecond laser-induced latchup and energetic particle-induced latchup in CMOS test structures," *IEEE Trans. Nucl. Sci.*, vol. 42, pp. 1948–1955, Dec. 1995.

[26] S. Buchner, D. McMorrow, J. Melinger, and A. B. Campbell, "Laboratory tests for single event effects," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 678–686, Apr. 1996.

[27] Y. Boulghassoul, S. Buchner, D. McMorrow, V. Pouget, L. W. Massengill, P. Fouillat, W. T. Holman, C. Poivey, J. W. Howard, M. Savage, and M. C. Maher, "Investigation of millisecond-long analog single-event transients in the LM6144 Op amp," *IEEE Trans. Nucl. Sci.*, vol. 51, pp. 3529–3536, Dec. 2004.

[28] S. Buchner, D. McMorrow, A. Sternberg, L. Massengill, R. L. Pease, and M. Maher, "Single event transient (SET) characterization of a LM119 voltage comparator: An approach to SET model validation using a pulsed laser," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 3, pp. 1502–1508, Jun. 2002.

[29] S. Buchner, J. Howard, C. Poivey, D. McMorrow, and R. Pease, "Pulsed-laser testing methodology for single event transients in linear devices," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3716–3722, Dec. 2004.

[30] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, and R. Pease, "Sub-bandgap laser-induced single event effects: Carrier generation via two-photon absorption," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3002–3008, Dec. 2002.

[31] J. S. Melinger, S. Buchner, D. McMorrow, W. J. Stapor, T. R. Weatherford, A. B. Campbell, and H. Eisen, "Critical evaluation of the pulsed laser method for single event effects testing and fundamental studies," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, pp. 2574–2584, Dec. 1994.

[32] D. McMorrow, T. Weatherford, A. Knudson, L. Tran, J. Melinger, and A. Campbell, "Single-event dynamics of high-performance HBTs and GaAs MESFETs," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1858–1866, Dec. 1993.

[33] D. McMorrow, J. S. Melinger, S. Buchner, T. Scott, R. Brown, and N. F. Haddad, "Application of pulsed laser for evaluation and optimization of SEU-hard designs," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 559–565, Dec. 2000.

[34] V. Pouget, D. Lewis, H. Lapuyade, R. Briand, P. Fouillat, L. Sarger, and M. C. Calvet, "Validation of radiation hardened designs by pulsed laser testing and SPICE analysis," *Microelectron. Reliab.*, vol. 39, pp. 931–935, 1995.

[35] P. E. Schmid, "Optical absorption in heavily doped silicon," *Phys. Rev. B*, vol. 23, pp. 5531–5536, 1981.

[36] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, J. D. Davis, R. K. Lawrence, N. Haddad, J. H. Bowman, R. D. Brown, D. Carlton, J. Pena, J. Vasquez, K. Warren, and L. Massengill, "Single-event upset in flip-chip SRAM induced by through-wafer, two-photon absorption," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2421–2425, Dec. 2005.

[37] R. Koga, S. H. Crain, K. B. Crawford, S. C. Moss, S. D. Lalumondiere, and J. W. Howard, "Single event transient (SET) sensitivity of radiation hardened and COTS voltage comparators," in *IEEE NSREC 2000 Data Workshop Proc.*, Reno, NV, 2000, pp. 53–60.

[38] A. L. Sternberg, L. W. Massengill, R. D. Schrimpf, and P. Calvel, "Application determinance of single-event transient characteristics in the LM111 comparator," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1855–1858, Dec. 2001.

[39] P. Adell, R. D. Schrimpf, H. J. Barnaby, R. Marec, C. Chatry, P. Calvel, C. Barillot, and O. Mion, "Analysis of single event transients in analog circuits," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2616–2623, Dec. 2000.

[40] M. W. Savage, Heavy Ion Analog SET Test of LM111 and LM124 Oct. 2002, NAVSEA CRANE Test Rep..

[41] C. Poivey, S. Buchner, J. Howard, K. LaBel, and R. L. Pease, Testing and hardness assurance guidelines for single event transients (SETs) in linear devices Jun. 30, 2003, NASA GSFC Rep.

[42] E. L. Petersen, "The SEU figure of merit and proton upset calculations," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2550–2562, Dec. 1998.

[43] R. Ecoffet, S. Duzellier, P. Tastet, C. Aicardi, and M. Labrunee, "Observation of heavy ion induced transients in linear circuits," in *IEEE NSREC 94 Data Workshop Proc.*, Tucson, AZ, Jul. 2000, pp. 72–77.

[44] A. L. Sternberg, L. W. Massengill, S. Buchner, R. L. Pease, Y. Boulghassoul, M. savage, D. McMorrow, and R. A. Weller, "The role of parasitic elements in the single-event transient response of linear circuits," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 3, pp. 1496–1501, Jun. 2002.

[45] R. Koga, S. H. Penzin, K. B. Crawford, W. R. Crain, S. C. Moss, S. D. Pinkerton, S. D. LaLumondiere, and M. C. Maher, "Single event upset (SEU) sensitivity dependence of linear integrated circuits (ICs) on bias conditions," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 2325–2332, Dec. 1997.

[46] N. W. van Vonno and B. R. Doyle, "Design considerations and verification testing of an SEE-hardened quad comparator," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 1859–1863, Dec. 2001.

[47] Y. Boulghassoul, P. C. Adell, J. D. Rowe, L. W. Massengill, R. D. Schrimpf, and A. Sternberg, "System-level design hardening based on worst case ASET simulations," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5, pp. 2787–2793, Oct. 2004.

[48] S. Buchner and D. McMorrow, "Single event transients in linear integrated circuits," in *Short Course presented at IEEE Nucl. Space Radiation Effects Conf.*, Seattle, WA, Jul. 11th, 2005.