Single Event Transients in Logic Circuits—Load and Propagation Induced Pulse Broadening

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***Abstract*—The generation and propagation of single event transients (SET) in logic gate chains is studied and modeled. Regarding SET generation, we investigate the dependence of the generated SET pulse width on the struck node capacitance. Rising node capacitance may lead to amplified pulse width, indicating that increasing load capacitance alone is not an option for radiation hardening. SET propagation in logic chains is also studied, and it is shown that significant broadening or attenuation of the propagated transient pulse width may be observed. It is shown that the chain design (propagation delay of high to low and low to high transitions) has a major impact on broadening or attenuation of the propagated transient pulse. For the first time a suitable model for SET broadening is provided.**

***Index Terms*—Digital single event transients, load-induced pulse broadening effect, propagation-induced pulse broadening effect, SET generation, SET propagation.**

I. Introduction

SINGLE-EVENT transients (SETs) caused by energetic particle strikes are of growing concern for advanced digital circuits designed for radiation environments [1]–[3]. Technology scaling has resulted in greater sensitivity to energetic particle strikes. Large transients may be generated and propagated through the logic chain, leading to errors in any logical path terminated with latch or memory elements.

Different design and modeling techniques have been proposed to help mitigate this problem. The use of gate cloning and gate resizing has been proposed as a less costly alternative compared to triple modular redundancy to enhance the SET tolerance of combinational logic in CMOS technology [4]–[7]. These techniques evaluate the most vulnerable nodes of a circuit based on the probability of SET electrical, logical and latching window masking. Once the most sensitive gate nodes are selected, the gates are resized in such way that the capacitance of the node is increased to reduce the probability of SET occurrence. The problem is that increasing the node capacitance may not always lead to a reduced SET width.

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This work studies both the generation and the propagation of SETs in logic circuits.

Regarding SET generation, this work evaluates the impact of node capacitance (capacitive load) on SET pulse width, based on device and circuit simulations, as well as on the light of experimental results recently made available in the literature [8], [9]. Two different technologies, 250 nm Bulk and 130 nm SOI CMOS, are chosen as case studies to allow comparison to relevant experimental data. Circuit and mixed-mode simulations are highly valuable tools for studying the generation and propagation mechanism of SETs, as well as elucidating the impact of process parameters and design practices. The objective is to understand the phenomena, allowing the adequate modeling and proposition of solutions to reduce the probability of SET pulse broadening. Results have shown that, depending on the incident particle and process technology, rising node capacitance may lead to either amplified or compressed transient width. Hence, increasing load capacitance alone is not an option for radiation hardening.

Regarding SET propagation, it was experimentally observed that a SET may also suffer pulse broadening as it propagates through logical chains [8], [9]. Pulse broadening would lead to increased probability of a SET turning into an error, increasing soft error rates [15]. These experiments did show that a SET may suffer a significant broadening as well as a significant degradation, depending on technology, circuit topology and loading of the logic chain. However, in these works the origin of this behavior was not studied in detail, and a suitable model was also not proposed. A model suitable to describe the observed behavior is lacking in the literature. In this work we analyze through electrical simulations the behavior of the SET propagation presented in [8] and [9], showing reasons for the occurrence of this behavior, and present an extension of the model presented in [12], adequately modeling this effect. The model is simple and analytical, suitable for implementation in a soft error analysis tool. Effects unique to SOI technology such as local floating body and thermal effects are not the focus of this work.

II. Set Generation: Load Induced Broadening

Recent experimental results from pulsed-laser and heavy-ion measurements of SETs in chains of inverters reveal significant load induced pulse broadening [8], [9]. The broadening factor depends on the number of inverters in the chain and on the capacitive load of each inverter. Based on these significant experimental results, it is important to investigate the reasons of the SET broadening and compression effects and how the capacitive load may play an imperative role in the pulse width of the generated SET.

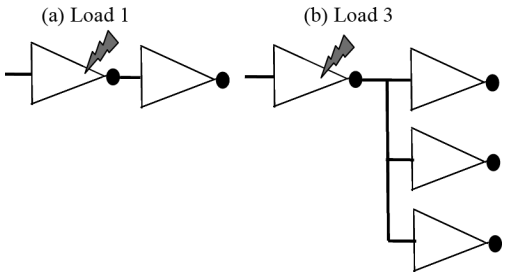

Fig. 1. Schematic of the inverter circuit used for the analysis of SET generation: a) A standard design with a fan-out (load) of one; and b) With fan-out (load) of three. In both cases, the struck transistor is part of the first inverter in the chain.

To allow the comparison to experimental results from the literature, the case study circuits and technology parameters are chosen to closely match the ones published in [8], [9] and were evaluated in a Mixed mode simulation. Two technologies are analyzed. The first one is a 0.25 μm CMOS bulk technology, with a supply voltage of 1.8 V. The second one is a 0.13 μm partially depleted SOI CMOS technology, with supply voltage of 1.2 V. The silicon film is 0.14 μm thick, and the buried oxide has a thickness of 0.4 μm. The equivalent gate oxide thickness is 2 nm.

For both technologies, the case study logical circuits are the same. The first circuit is an inverter circuit in a standard linear design, where the struck inverter is connected only to a single inverter, as shown in Fig. 1(a). This standard structure is labeled "Load 1". The second circuit, labeled "Load 3", allows investigating the effect of a load on the chain response. In this circuit the output of the struck inverter is connected to the input of three inverters, as shown in Fig. 1(b).

For both circuits (Load 1 and Load 3), inverter designs with different transistor sizes are investigated. For the SOI technology, the transistor gate length is always the same (0.13 μm). For the Bulk technology, transistor gate length is always 0.25 μm. In both cases (Bulk and SOI), the gate width $(W_{\rm N})$ for NMOS transistors varies from 0.3 μm to 2.7 μm, and the PMOS width $(W_{\rm P})$ is twice the NMOS width.

The single event transients are simulated using the Synopsys Taurus Medici package [10]. Mixed mode (level) simulations are performed using the Circuit Analysis Advanced Application Module. The charge collection and current generation mechanism are simulated in three dimensions at the device level, while the circuit response is simulated at the circuit level. To simulate the environment of the transistor operating in a real circuit and allow comparison to recent experimental data, the struck transistor is simulated as being part of an inverter.

For all results presented in this section, the input of the first inverter is connected to the electrical ground. Hence, the gate contact of the struck NMOS is fixed at ground. The source contact is also connected to ground. The drain contact is connected to the output node of the inverter. For the bulk technology the bulk is connected to ground, and for the SOI technology the body is connected to ground. The struck transistor is then in the off state. These voltages reverse bias the struck drain-substrate junction.

To study the SET generation mechanism, a 100 MeV argon ion passing through the drain of the NMOS transistor is simulated in three dimensions. The charge generation rate versus depth of penetration of the energetic particle is obtained from [11]. The LET of a 100 MeV argon ion is approximately 17 MeV-cm^2/mg.

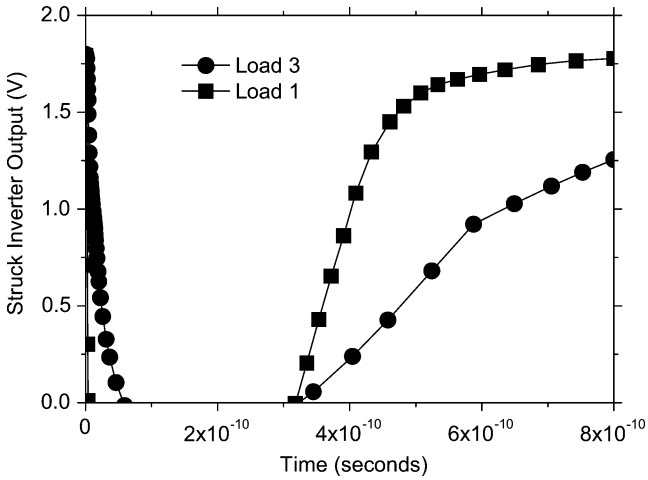

Fig. 2. Voltage at the drain contact of the struck PMOS transistor. Circles (•) are the simulation results for the Load 3 chain. Squares (■) correspond to the simulation results for Load 1 chain. The results correspond to the 0.25 μm Bulk technology with $W_{\rm N} = 0.3$ μm and $W_{\rm P} = 0.6$ μm.

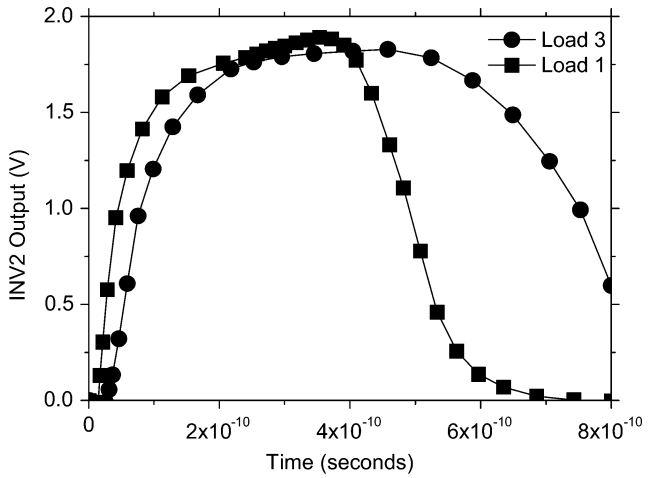

Fig. 3. Voltage at the output of the second inverter. Circles (•) are the simulation results for the Load 3 chain. Squares (■) correspond to the simulation results for Load 1 chain. The results correspond to the 0.25 μm Bulk technology with $W_{\rm N} = 0.3$ μm and $W_{\rm P} = 0.6$ μm.

The particle strikes at the reverse biased drain junction, at position $x = 0.05$ μm and $z = 0.05$ μm, perpendicular to the silicon surface. During the upset process, the conductive charge track generated by the passage of the energetic particle temporarily short circuits the drain-substrate junction and pulls the drain down to the lower potential of the substrate. This voltage change at the drain node is known as single event transient (SET) at the circuit level, and may lead to circuit faulty behavior. The first 800 picoseconds (ps) of the transient response are simulated. The particle strike occurs at time $t = 0$.

Device simulation results for the 0.25 μm Bulk technology are shown in Figs. 2 and 3. Fig. 2 shows the voltage at the drain contact of the struck transistor, from $t = 0$ to $t = 800$ ps, while Fig. 3 shows the output voltage of the second inverter.

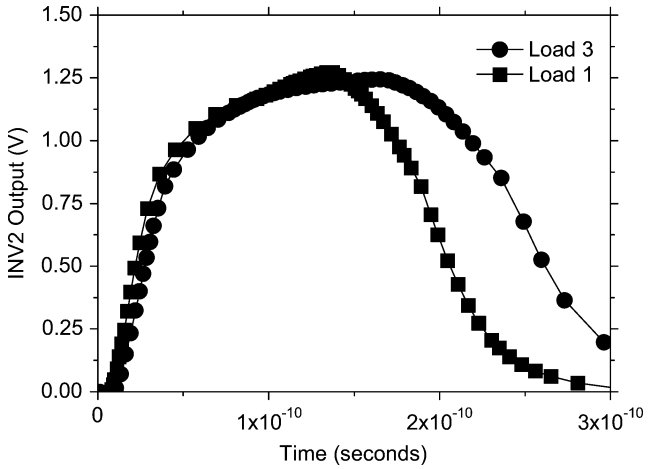

Fig. 4. Voltage at the output of the second inverter. Circles (•) are the simulation results for the Load 3 chain. Squares (■) correspond to the simulation results for Load 1 chain. The results correspond to the 0.13 μm SOI technology with $W_{\rm N} = 0.3\ \mu{\rm m}$ and $W_{\rm P} = 0.6\ \mu{\rm m}$.

Circuit Load 3 has an increased capacitive load at the struck node, while the drive strength of the PMOS transistor is kept the same. The PMOS transistor of the struck inverter drives a current that attempts to restore the node voltage. An increased capacitive load means that a larger charge has to be delivered to the node in order to restore its voltage from ground to $V_{\rm DD}$. Since the charge delivered is the integral of current over time, increasing the capacitive load while keeping the same drive strength leads to an increase in the time needed to restore the voltage. This behavior can be clearly seen from Fig. 2. At around 300 ps the conductive path between drain and substrate is extinguished, and the drain circuit node is pulled up to $V_{\rm DD}$ through the PMOS transistor of the first inverter. For a smaller load capacitance the restoring PMOS transistor pulls the node voltage back to $V_{\rm DD}$ much faster.

As it can be seen from Fig. 3, if the pulse width is measured at $V_{\rm DD}/2$, the SET width at the output of the second inverter increases from approximately 500 ps in the Load 1 circuit to approximately 750 ps in the Load 3 circuit, a 50% increase in pulse width. If the capacitive loading at the struck node is increased further, the transient width broadening will also be increased. If the sizes of the transistors in the first inverter are properly increased to match the fan-out, the load induced pulse broadening is avoided.

For the 0.13 μm SOI technology, similar results are obtained, as can be seen from Fig. 4. A 100 MeV argon ion strikes at the drain of the NMOS transistor in the first inverter (same as for the 0.25 μm Bulk technology).

One can conclude that, if the charge generated by the ion track is greater than the charge stored at the struck node, increasing the node capacitance may lead to increased transient width. This is due to increased charged collection at the equivalent capacitance of the struck node.

The collected charge is calculated as the numerical integral of the transient current generated at the drain of the stuck transistor. The charge generated by the ion track is given by the device simulator, as the integral over time of the generated electron-hole pairs.

The original voltage at the struck node is recovered by the restoring transistor, which is in the on-state and drives a current that opposes the current generated by the particle strike.

The duration of the SET may be determined by the relation between the drive strength of the restoring transistor and the nodal capacitance. If extra capacitance is connected to a node, although this can increase the node critical charge, it provokes a worse response at voltage restoring, which ends up broadening the SET pulse width. These results show the importance of performing a careful transistor sizing in order to enhance SET tolerance.

To further study the impact of generated charge and node capacitance on the SET pulse width, we now study the strike of a 5.5 MeV alpha particle at the drain of the NMOS transistor, also by simulation in three dimensions, under the same conditions as above. The LET of a 5.5 MeV alpha particle is approximately 0.6 MeV-cm^2/mg. In this case, the transient voltage at the struck node does not reach ground, and increasing node capacitance may decrease the SET width. The reason is that, in this case the node capacitance avoids large voltage changes, and the strength of the transistors connected to the stuck node can rapidly restore the node voltage completely avoiding a SET or sustaining short SET widths. In the case of the 5.5 MeV alpha particle the amount of charge collected does not depend on the node capacitance. In these cases almost all charge generated by the ion track is collected at the node capacitance, regardless of the node capacitance.

However, in the case of the 100 MeV argon ion, the collected charge depends on the node capacitance. In this case the node capacitance is completely discharged, as can be seen in Fig. 2. Hence, an increase in the node capacitance leads to an increase in the amount of charge removed from the capacitance, which has to be restored by the restoring transistor.

Analysis of the collected charge shows that increasing node capacitance leads to the collection of an increasing fraction of the generated charge. In the case of the Load1 circuit in the 0.25 μm technology, the amount of charge effectively collected at the node capacitance is 3.0×10^{-14} C. For the Load3 circuit in the same technology, the amount of charge effectively collected at the node due to the same 100 MeV argon ion strike increases to 5.5×10^{-14} C. Furthermore, if the node capacitance is increased further, charge enhancement due to bipolar amplification as shown in [14] may be observed, further increasing the SET duration.

Although all presented results are for input at logical zero in the first inverter, simulations were also performed for input at logical one. In this case, the particle strike occurs at the drain of the PMOS transistor. The results of these simulations lead to the same conclusions.

III. SET Propagation: Propagation Induced Pulse Broadening

In the previous section the SET generation mechanism was studied. In this section we study the propagation of the generated SET through the circuit's logic chain.

V. Ferlet-Cavrois *et al.* and D. McMorrow *et al.* performed experimental studies and characterization of SET propagation in chains of inverters, using the two different CMOS technologies:

the 0.25 μm Bulk CMOS technology and the SOI CMOS 0.13 μm technology [8], [9].

The case study circuits are similar to the ones studied in the previous sections. The difference is that now long chains of inverters are studied. Two chains of inverters were designed and fabricated for performing that experimental work. The first chain was called Load1, and presents a chain of inverters with fan-out 1 at each circuit node. The second chain was called Load3, and presents a chain of inverters in which the odd nodes of this chain are fan-out 3, while the even nodes are fan-out 1.

In these experiments V. Ferlet-Cavrois *et al.* and D. McMorrow *et al.* did inject SETs through laser pulses. The laser spot was initially focused close to the chain input, on the tenth inverter, and then moved to different positions along the inverter chain. The experimental results showed a behavior that should be reviewed and investigated further, as it was observed that the duration of the transient pulse at the output node of the chain of inverters strongly depends on the position of the struck node and on the circuit topology [8], [9].

It was found that if the laser strikes at a node close to the input node of the chain of inverters, the duration of the SET appearing at the output node may be broadened, if compared to the SET injected at other positions. The authors did conclude that, in this case, the duration of the SET increased as it was propagated through the chain of inverters [8], [9].

For the Load3 chain, SET broadening occurs only if the input of chain is kept at the logical value "0", i.e., ground. If the input of the chain of inverters is kept at the logical value "1", i.e., $V_{\rm DD}$, the transient pulse injected into the circuit has its amplitude and duration degraded. The authors did conclude that, in this case, the duration of the SET was attenuated as it was propagated through the chain of inverters [8], [9].

However, the reasons for the observation of such behavior were not studied in detail in that works, and a suitable analysis and model is lacking in the literature. Here we analyze this behavior by means of electrical simulations, intending to develop a suitable model.

In this work, a SET is defined as a particle strike induced voltage change that changes the node voltage by at least $V_{\rm DD}/2$. The duration of the transient pulse at node $n(\tau_n)$ is the time during which the voltage change is greater than $V_{\rm DD}/2$ [12]. The propagation delay is defined as t_{pLH} for an output transition from logical "0" (low) to a logical "1" (high), while t_{pHL} refers to a high to low output transition. The propagation delay is measured between the 50% transition points of the input and output waveforms [16].

In order to allow fast and accurate analysis of SET propagation, electrical simulations were run for the 0.25 μm Bulk technology [13], using Hspice. As in the discussion of SET generation in the previous section, two distinct chains of inverters were simulated, as shown in Fig. 5. The first chain of inverters is called Load1. In this chain all nodes have fan-out equal to 1. The second chain of inverters is called Load3. All odd nodes of the chain have fan-out equal to three, while all even nodes of the chain have fan-out equal to one.

The transistors sizes used in the electrical simulations are shown in the Table I. The first column of Table I shows the name used to identify each inverter chain through this work. The second column shows the type of chain used in the simulation, and the third column shows the channel width of the NMOS transistors. The NMOS transistor channel width $(W_{\rm N})$ varies from 0.3 μm to 1.8 μm, and the PMOS channel width is *always twice* the NMOS channel width. In all cases, the NMOS and PMOS channel length (L) is 0.25 μm. The supply voltage used for the 0.25 μm Bulk technology was 1.8 V.

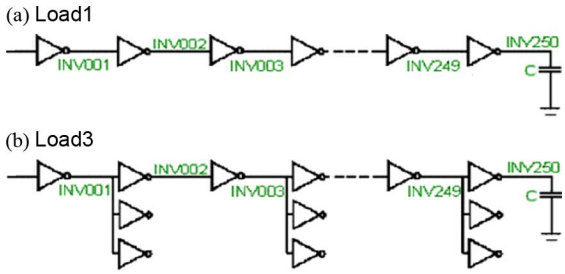

Fig. 5. Schematic description of the chain of inverters used for the analysis of SET propagation: (a) A standard design, and (b) With every other inverter triplicated to simulate the load of more complex designs.

TABLE I
INVERTERS CHAINS IN THE 0.25 μm BULK TECHNOLOGY.

Chain Name	Load	NMOS width
Chain1-L1	*Load 1*	*0.3 µm*
Chain2-L1	*Load 1*	*0.6 µm*
Chain3-L1	*Load 1*	*1.8 µm*
Chain1-L3	*Load 3*	*0.3 µm*
Chain2-L3	*Load 3*	*0.6 µm*
Chain3-L3	*Load 3*	*1.8 µm*

TABLE II
PROPAGATION DELAY.

Chain	tp_{LH} (ps)	tp_{HL} (ps)	Δtp (ps)
Chain1-L1	86.20	70.90	15.30
Chain2-L1	82.60	72.10	10.50
Chain3-L1	78.90	71.30	7.60
Chain1-L3 Even Node	86.20	70.90	15.30
Chain1-L3 Odd Node	129.95	101.13	28.82
Chain2-L3 Even Node	82.60	72.10	10.50
Chain2-L3 Odd Node	126.28	104.46	21.82
Chain3-L3 Even Node	78.90	71.30	7.60
Chain3-L3 Odd Node	122.32	104.68	17.64

Table II shows the propagating delays t_{pLH} and t_{pHL} of an inverter in each one of the chains, as well as the difference Δt_p between them. Please note that for the Load3 chains the propagation delay at even nodes is different from the propagation delay at odd nodes. This is due to the fan-out of three at every other node.

For better understanding the results obtained by means of the electrical simulations, the results are divided into subsections, according to the fan-out at the chain nodes.

TABLE III
SET PROPAGATION IN INVERTER CHAINS.

Node	τ_n (ns) for Chain2-L1 Input at "0"	τ_n (ns) for Chain2-L3 Input at "0"	τ_n (ns) for Chain2-L3 Input at "1"
INV001	0.73	0.83	0.79
INV002	0.76	0.84	0.85
INV003	0.75	0.88	0.84
INV004	0.76	0.87	0.85
INV017	0.78	0.98	0.74
INV018	0.77	0.97	0.75
INV019	0.78	0.99	0.73
INV020	0.77	0.98	0.74
INV067	0.78	1.33	0.37
INV068	0.77	1.32	0.38
INV069	0.78	1.34	0.35
INV128	0.77	1.74	0
INV129	0.78	1.76	0
INV249	0.78	2.59	0
INV250	0.77	2.58	0

A. Load1 Circuits

The three Load1 chains of inverters were simulated with the input of the first inverter at logic "0", as well as with the input of the first inverter at logic "1".

We observed that, for the simulated 0.25 μm Bulk technology, SET broadening did not occur for any of the three chains, regardless of the sizing of the transistors (transistors sizes for chain1, chain2 and chain3 are shown in Table I) or input value for the first inverter.

The second column of Table III presents the results obtained when a transient pulse $1 \longrightarrow 0 \longrightarrow 1$ is injected at the first node, labeled 'INV001' (please see Fig. 5), for the Chain2 Load1 circuit with input fixed at logical "0" (ground). The first column of this table specifies the circuit node, while the second column shows the transient pulse duration (τ_n) at the specified node. In this case, negligible pulse broadening or attenuation is observed at the SET propagates through the chain.

The same behavior is observed for the Chain1 Load1 and the Chain3 Load1 circuits. The same behavior is also observed if a transition pulse $0 \longrightarrow 1 \longrightarrow 0$ is injected at the 'INV001' node, with the input of the Load1 circuit fixed at logical "1" $(V_{\rm DD})$. We will show that this behavior is related to the loading at the circuit nodes and the sizing of the transistors.

B. Load3 Circuits

For the Load3 circuits the behavior is different. Either broadening or attenuation is observed, depending on the state of the input of the chain.

The third column of Table III presents the results obtained if a transient pulse $1 \longrightarrow 0 \longrightarrow 1$ is injected at the 'INV001' node of the Chain2 Load3 circuit with its input fixed at logical "0" (ground). It can be seen that the SET broadening effect occurs. The duration of the transient pulse (τ_n) increases as the SET propagates through the chain of inverters. This behavior is also observed for the Chain1 Load3 and the Chain3 Load3 circuits. As shown in Fig. 5, the Load3 circuits have two types of nodes: the even nodes with fan-out 1 and odd nodes with fan-out 3. Because of this there is a significant unbalance between the propagation delays of subsequent nodes, as shown in Table II.

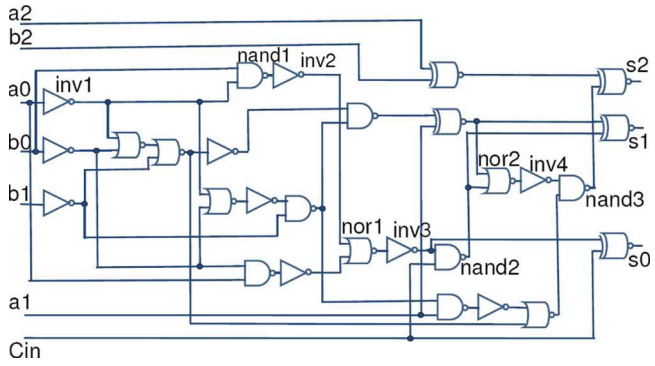

Fig. 6. Three bit adder.

The fourth column of Table III presents the results obtained if a $0 \longrightarrow 1 \longrightarrow 0$ transient pulse is injected at the 'INV001' node of the Chain2 Load3 circuit with its input fixed at logical "1" $(V_{\rm DD})$. It can be seen that the duration of the transient pulse is degraded as it is propagated through the chain, in agreement with the experimental results reported in [8] and [9]. The behavior is also observed for the Chain1 Load3 and the Chain3 Load3 circuits with its input fixed at logical "1".

C. Unbalanced Load1 Circuit

The unbalanced Load1 circuit has fan-out 1 for all nodes in the chain of inverters. The transistor sizes of the *even* nodes are as shown in Table I, where the PMOS transistors channel width is twice the NMOS width. However, to assure unbalance in propagation delays between nodes, the transistors in the *odd* nodes are 1.2 times larger than the transistors in even nodes.

Simulations show that for this circuit the broadening effect occurs in the same way as observed for the Load3 circuit. If the circuit input is fixed at logical "0" (ground) and a transient pulse $1 \longrightarrow 0 \longrightarrow 1$ is injected at the 'INV001' node, the broadening effect is observed as the SET is propagated through the unbalanced Load1 circuit. However, if the circuit input is fixed at $V_{\rm DD}$, the duration and amplitude of the transient pulse decreases as it propagates along the chain of inverters. This confirms that the delay unbalancing is a cause of the broadening effect.

D. Three-Bit Adder

Although it is easy to find complex tree path structures with many logical levels for control or clock signals, in which gate sizes and loads vary many times along the logic path, we also perform propagation analysis in more typical circuits. We also used a three-bit adder circuit to examine the SET propagation, as shown in Fig. 6.

The SET propagation behavior is shown in Table IV. It refers to the situation in which a $1 \longrightarrow 0 \longrightarrow 1$ SET is inserted at the node labeled Inv1 (see Fig. 6). The logical inputs where (010 100 1), for the inputs $(\mathrm{a_0 a_1 a_2\ b_0 b_1 b_2\ c_{in}})$, respectively.

As can be seen from results shown in Table IV, the transient pulse broadening effect occurs, although it is not as significant as in the Load3 circuit, which has 250 logical levels.

TABLE IV
SET PROPAGATION THROUGH A THREE BIT ADDER: MODEL AND SIMULATION.

Node	Gate tp_{LH} (ps)	Gate tp_{HL} (ps)	SET Width Model (ps)	SET Width Simulation (ps)
inv1				752.09
nand1	157.18	178.27	773.18	773.17
inv2	117.31	79.59	810.90	810.89
nor1	151.32	86.14	745.72	745.71
inv3	174.45	171.38	748.79	748.78
nand2	112.69	170.25	806.35	806.35
nor2	240.70	109.35	937.70	937.69
inv4	93.51	93.53	937.72	937.71
nand3	130.00	142.24	925.48	924.46
s2	154.46	152.29	927.65	925.21

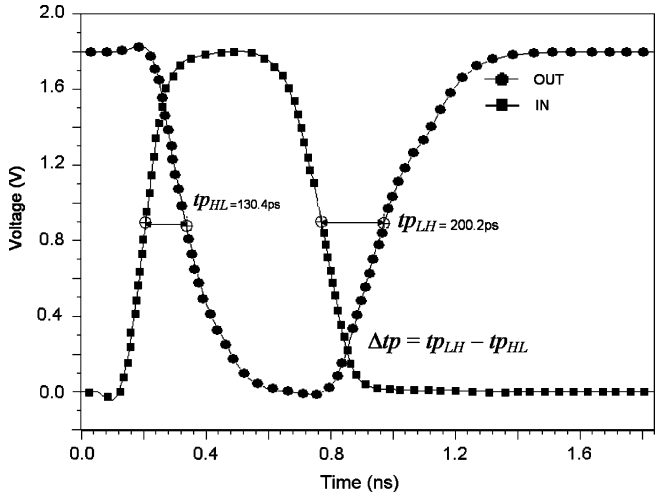

Fig. 7. Propagation induced pulse broadening. If the propagation delay for the first transition is shorter than the propagation delay for the second transition, the pulse is broadened, as shown in this figure.

As can be seen, this effect occurs due to the delay unbalance at different circuits nodes. There is a difference between propagation delays t_{pHL} and t_{pLH} for some gates. The transient pulse broadening at a node is approximately the difference between the propagation delays, as can be seen from the results shown in Table IV.

If the transistors of the gates are resized to achieve very similar t_{pHL} and t_{pLH} delays at all nodes, pulse broadening is avoided.

In the case of a transient pulse at a node, if the delay for propagating the first transition is shorter than the delay for propagating the second transition, the SET is broadened. If the delay for propagating the second transition is shorter than the delay for propagating the first transition, the SET is attenuated.

Fig. 7 shows the situation for a $0 \longrightarrow 1 \longrightarrow 0$ transition at the input of a gate ($1 \longrightarrow 0 \longrightarrow 1$ output transition), for which t_{pLH} is larger than t_{pHL}. It can be seen that in this case the duration of the pulse is broadened (Δt_p is positive). If t_{pLH} is shorter than t_{pHL}, the pulse is attenuated (Δt_p is negative).

In the case of the propagation of a SET through a long logic chain, if all stages present the same t_{pLH} and t_{pHL}, SET pulse broadening is not expected. In this case, even if t_{pLH} and t_{pHL} are different, Δt_p of subsequent logic stages has the same magnitude but opposite signal. Hence, broadening and attenuation alternate between subsequent stages. Such a situation may be found in the Load1 circuits.

However, if Δt_p of subsequent logic stages is different, SET broadening may happen. This is the case of the Load3 circuits. Please note that in the Load3 circuits the same transition ($0 \longrightarrow 1 \longrightarrow 0$ or $1 \longrightarrow 0 \longrightarrow 1$) always happens on odd nodes. At even nodes the complementary transition happens. Hence, the value of Δt_p for odd and even nodes will be different, and SET broadening may happen, as experimentally observed in [8].

We may then define the following equations for the difference in propagation delay Δt_p at a given node.

For a $1 \longrightarrow 0 \longrightarrow 1$ transition at the n-th node, Δt_p is defined as:

$$\Delta t_p = t_{pHL} - t_{pLH}. \tag{1}$$

For a $0 \longrightarrow 1 \longrightarrow 0$ transition at the n-th node, Δt_p is defined as:

$$\Delta t_p = t_{pLH} - t_{pHL}. \tag{2}$$

Note that for the Load3 circuits with its input at logic "0", the equation that models SET propagation at even nodes is (1), while the equation that models SET propagation at odd nodes is (2). Since the magnitude of the positive Δt_p at odd nodes is greater than the magnitude of the negative Δt_p at even nodes, SET broadening occurs.

However, for the Load3 circuit with its input at logic "1", (2) models SET propagation at even nodes, while (1) models SET propagation at odd nodes. In this case SET attenuation is expected, as experimentally observed.

IV. PROPOSED MODEL FOR PROPAGATION INDUCED SET PULSE BROADENING

The model presented in this section is the extension of the model proposed in [12], in order to adequately model the propagation induced pulse broadening effect, described in Section III. The model is extended to include the unbalance in propagation delays Δt_p. The main contributions of this work are elucidating the origin of the load induced pulse broadening effect of the generated SET, and the propagation induced pulse broadening effect, as well as its modeling.

The Hspice simulation and model results shown in this section are for the 0.25 μm Bulk technology [13].

The model is divided into four regions, according to the relationship between τ_n (duration of the transient pulse at the n-th logic stage) and the gate delay t_p. Where t_p will be equal to t_{pHL} for a $0 \longrightarrow 1 \longrightarrow 0$ transition at the n-th node, or, equal to the t_{pLH} for a $1 \longrightarrow 0 \longrightarrow 1$ transition.

The first region represents the situation where the transient pulse is filtered out. The model evaluates the duration of the transient pulse, defined as the time during which the voltage change at the node is greater than $V_{\rm DD}/2$. For a transient pulse to be propagated to the next logic stage, the ratio τ_n/t_p, must be equal to or greater than k. k is a fitting parameter which depends

on the technology of interest. For transient pulses with duration τ_n smaller than k times t_p, the voltage at the next node changes less than $V_{\rm DD}/2$. It is then considered that the transient is filtered out, i.e., not propagated to the $(n+1)$th stage. Thus, the model for this region is:

$$if\ (\tau_n < kt_p) \longrightarrow \tau_{n+1} = 0. \quad (3)$$

The second region represents the situation in which the transient pulse is not degraded by electrical masking, but may have its duration broadened or attenuated as it propagates through the chain of logical gates, due the unbalance between t_{pLH} and t_{pHL}. This occurs if the input pulse has duration (τ_n) greater than $(k+3)$ times t_p:

$$if\ (\tau_n > (k+3)t_p) \longrightarrow \tau_{n+1} = \tau_n + \Delta t_p. \quad (4)$$

Note that in this situation no pulse degradation is assumed to occur if the propagation delays t_{pLH} and t_{pHL} are equal. Any SET broadening or attenuation will arrive from the unbalance between t_{pLH} and t_{pHL}.

The third and fourth regions model the situation in which electrical masking occurs.

It is found that the pulse may degrade faster in the last logic stages before being filtered out. Hence, it is appropriate to model pulse attenuation into two regions, with different equations modeling the degradation in each one of these two regions.

The model for the third region, where electrical masking may start, was obtained by curve fitting, and is:

$$if\ ((k+1)t_p < \tau_n < (k+3)t_p) \longrightarrow \tau_{n+1} = \frac{(\tau_n^2 - t_p^2)}{\tau_n} + \Delta t_p. \quad (5)$$

The fourth region models the situation where stronger degradation occurs. In the last stages before being filtered out, the pulse degrades faster if compared to the pulse decreasing in the early stages, and the model for the third region loses its validity for these pulses that are being almost filtered out. The model for the fourth region is obtained:

$$if\ (kt_p < \tau_n < (k+1)t_p) \longrightarrow \tau_{n+1} = (k+1)t_p\left(1 - e^{(k-(\tau_n/t_p))}\right) + \Delta t_p. \quad (6)$$

The model is validated by comparing the results obtained using model equations to Hspice circuit simulation for the 0.25 μm Bulk technology node.

Several simulations are performed, being some of them presented in the Tables IV and V, for the three-bit adder circuit and the Load3 circuit, respectively. For the results shown in Table IV, a $1 \longrightarrow 0 \longrightarrow 1$ SET is inserted at the node labeled Inv1 (see Fig. 6), while the logical inputs where (010 100 1), for the inputs ($\rm a_0 a_1 a_2\ b_0 b_1 b_2\ c_{in}$), respectively. For the results shown in Table V, the input of the chain is kept at logical zero. These tables show the propagation induced pulse broadening effect and compare Hspice simulation results to model prediction, as given by (4). The parameter k was set equal to 1.5. Good agreement is found for the main region of interest for modeling the pulse broadening effect, which is the second region of the model. For the other regions good agreement between model and simulation is also found. If techniques common to timing analysis are used, the accuracy of the model can be further improved. For instance, if the slew rate of the transition at the input of a logic gate is modeled in detail, the accuracy can be significantly improved by properly modeling its propagation delay. In this case the propagation delays of the even nodes of a Load3 chain would be different from the propagation delays of the corresponding Load1 chain. If the inverter at the preceding node is loaded with a fan-out of three, the slew rate may be degraded and affect the delay at the subsequent stage. In the validation of the model here performed this was not taken into account (see Table II). If the model is built into a timing analysis like tool, this effect can be easily accounted for.

TABLE V
PROPAGATION INDUCED PULSE BROADENING: COMPARING MODEL TO SIMULATION.

Node	τ_n (ns) for Chain1-L3 Simulation	τ_n (ns) for Chain1-L3 Model	τ_n (ns) for Chain2-L3 Simulation	τ_n (ns) for Chain2-L3 Model
INV002	0.73	0.71	0.84	0.83
INV003	0.77	0.74	0.88	0.85
INV004	0.75	0.72	0.87	0.84
INV017	0.88	0.83	0.98	0.93
INV018	0.87	0.82	0.97	0.92
INV019	0.90	0.84	0.99	0.94
INV020	0.88	0.83	0.98	0.93
INV067	1.29	1.17	1.33	1.21
INV068	1.28	1.15	1.32	1.20
INV069	1.31	1.18	1.34	1.22
INV128	1.76	1.56	1.74	1.54
INV129	1.80	1.59	1.76	1.56
INV249	2.76	2.41	2.59	2.25
INV250	2.74	2.38	2.58	2.23

V. CONCLUSION

The impact of process parameters and design practices on SET width is studied through device and circuit simulations.

It is shown that, depending on the incident particle and process technology, increasing node capacitance (capacitive load) may lead to either broadening or compressing the generated transient pulse width. Proper driving strength of the transistors, making them able to restore the voltage at the struck node, is important to ensure a fast voltage recover and maintain short SET widths.

The broadening of single event transients, as they propagate through the logic gates, is also analyzed. To prevent the effect of propagation induced broadening of SETs in combinatorial circuits, the logic gates should be designed to present balanced high to low and low to high propagation delays, since SET broadening may lead to increased soft error rates. A simple model for single event transient propagation is proposed. It is shown that transient propagation can be properly modeled by

considering the gate propagation delays and a constant k, which depends on the technology of interest. The model is suitable for automated evaluation of the sensitivity of digital circuits to transient faults and radiation hardening.

Besides the relevance of pulse broadening for integrated circuits running in specific applications, the conclusions of this work are also of relevance for test structures used in test campaigns under ion irradiation. In such test structures long chains are often used, and an anomalously broad range of SET pulse widths may be observed at the output of the test circuit, due to the SET broadening effects here described.

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