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ABSTRACT

SEU is studied in SOI transistors and circuits with various body tie structures. The importance of impact ionization effects, including single-event snapback, is explored. Implications for hardness assurance testing of SOI integrated circuits are discussed.

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I. INTRODUCTION

Single-event upsets (SEUs) are caused by charge collection at sensitive circuit nodes following an incident energetic particle strike. One method for hardening against SEU is to reduce the amount of charge collection, for instance through the use of silicon-on-insulator (SOI) substrates [1]. In this case the collection volume is reduced because the device is fabricated in a thin silicon layer that is dielectrically isolated from the substrate.

Unfortunately, charge deposited in the body region of SOI transistors (the active silicon region underneath the gate) can trigger a bipolar mechanism that limits the SEU hardness of SOI circuits [2]. In n-channel SOI transistors, for example, holes left in the body following an ion strike can raise the body potential (known as a floating body effect, or FBE), turning on the lateral parasitic bipolar transistor inherent to SOI transistors. In extreme cases, FBEs can also trigger a high-current state referred to as single-event snapback (SES) or single-transistor latch if the channel conduction is sustained through regenerative impact ionization effects [3,4].

Proper body tie design to prevent FBEs is a key element for achieving SEU-hard circuits in SOI. In this summary, we use numerical simulations to study charge collection and SEU in SOI transistors and simple memory circuits with various body tie structures. The importance of impact ionization effects, including single-event snapback, will be discussed for deep submicron devices. The results have implications for hardness assurance testing of SOI integrated circuits.

II. SIMULATION TECHNIQUE

Simulations were performed using the three-dimensional device/circuit simulator Davinci [5]. 3D simulations are necessary in order to define realistic body tie structures. We have performed charge-collection simulations of single transistor structures, and SEU threshold calculations for CMOS SRAMs using Davinci's mixed-level device/circuit capabilities [6]. Physical models used in the simulations included carrier concentration-dependent minority carrier lifetimes, Auger recombination, and mobility models which

included doping, electric field, and carrier-carrier scattering dependence. To determine its impact on the results, simulations were performed both with and without Davinci's impact ionization model active.

The technology modeled in this study is a 0.35- μm , 3.3-V partially-depleted SOI technology (CMOS7) currently under development at Sandia National Laboratories and largely based on Sandia's CMOS6r bulk technology [7]. Because this technology is still under development, not all parameters have been finalized. For the simulations in this summary, the gate oxide thickness was 80 Å, the as-drawn gate length was 0.35 μm , and the gate width was 0.75 μm . The simulated top silicon thickness was 1800 Å, and the buried oxide (BOX) thickness was 3700 Å. For the modeled n-channel transistors a retrograde well profile was used with a surface concentration of $\sim 1.5 \times 10^{17} \text{ cm}^{-3}$ and a back-channel concentration at the silicon/BOX interface of $\sim 1 \times 10^{18} \text{ cm}^{-3}$. For circuit simulation parameters, the p-channel transistors were assumed to be the same size as the n-channels. A worst-case strike location at the center of the "off" n-channel gate was used for all simulations [8].

Two basic types of body ties were studied: a conventional Body-Tied-to-Source (BTS) configuration [9], and structures based on combining BTS body ties with the Body-Under-Source FET (BUSFET) proposed at last year's NSREC [10]. The only difference between the simulated BTS and BUSFET structures is that in the BUSFET the source junction is at a depth of 900 Å, while in the BTS structure the source doping extends to the silicon/BOX interface. The shallow source gives the BUSFET a body tie underneath the source along the entire width of the channel [10].

For each style of body tie, ideal and non-ideal versions were simulated, as shown in Figure 1. For the ideal structures (Fig. 1a), the source and body regions are directly tied together (for instance, by silicidation [9]), and the body contact is immediately adjacent to the body region. For strings of transistors connected in series (such as might be found in a multiple-input NAND gate), several transistors may be connected to a single body tie, in which case the furthest transistor may

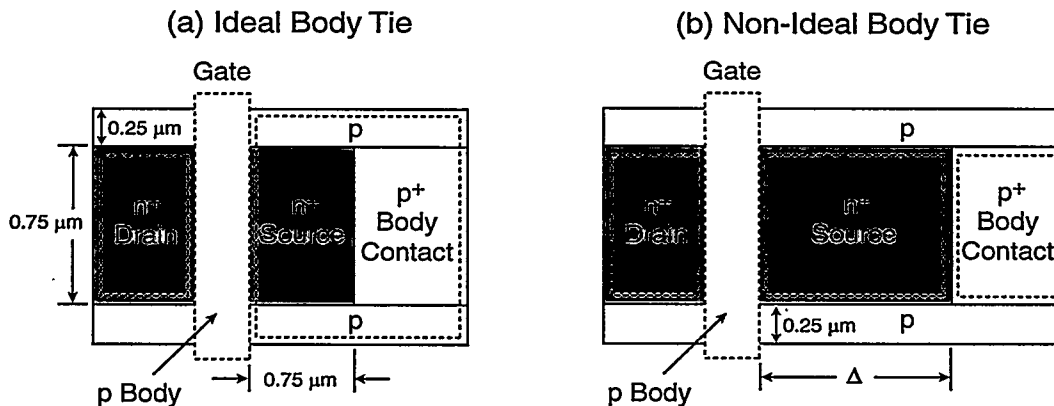


Figure 1. Plan views of simulated body tie structures, with dotted outlines denoting contact regions. (a) Ideal structure with a single silicided region forming both source and body contacts. (b) Non-ideal structure with separate source and body contacts.

lie at some distance from the body tie contact[†]. This is reflected in the non-ideal structure of Fig. 1b, where the body contact and the body region are separated by a silicon body tie region of width $0.25\ \mu\text{m}$ whose length Δ was varied in the simulations. In this summary, this region was assumed to have a doping level equal to the channel region. In the full paper the impact of increasing the body tie region doping will be shown, as well as results for larger transistor and body tie region widths.

III. RESULTS

Charge-Collection Simulations

Figure 2 shows the simulated total charge collection in conventional BTS n-channel transistors with a drain bias of 3 V with and without including the effects of impact ionization (II). The simulated ion strike deposits about 11 fC of charge in the active silicon layer (equivalent to an LET of about $6\ \text{MeV}\cdot\text{cm}^2/\text{mg}$). With impact ionization “turned off” in Davinci (blue circles), we see gradually increasing charge collection as the distance from the p^+ body contact to the body region is increased (the ideal case of Fig. 1a is plotted as a distance to body contact of 0, and for the non-ideal case the distance to body contact corresponds to the parameter Δ in Fig. 1b). This increase in charge collection is due entirely to the bipolar mechanism [2], which increases in importance as body tie effectiveness falls off with distance [8]. Note that even for the ideal case, the bipolar effect causes charge multiplication and more than twice the charge that was initially deposited in the top silicon is collected. As the distance to the body contact increases we approach the case for non-body-tied (i.e., floating body) transistors. This is a

[†] Devices such as pass transistors may also require independent body contacts that lie at some distance from the body region [9].

useful result because we can’t in general simulate SOI transistors without body ties directly due to convergence problems with the simulator for floating body devices.

For simulations including impact ionization (red squares in Fig. 2), the results are dramatically different. At body contact distances of $1.75\ \mu\text{m}$ and above the transistor enters snapback for the ion strike simulated here. This snapback mode occurs within 1 ns after the strike, when the drain current becomes constant at about 0.2 mA and is self-sustaining through impact ionization at the drain junction. The transistor becomes latched in this high-current condition, resulting in infinite charge collection at the drain. In Figure 2, the charge collection in cases where snapback occurs has been arbitrarily plotted as 320 fC, with arrows indicating that the collection is actually much higher. It is important to note that in these simulations, the drain bias is artificially maintained at 3 V, which helps sustain impact ionization due to the large drain electric field. Whether this

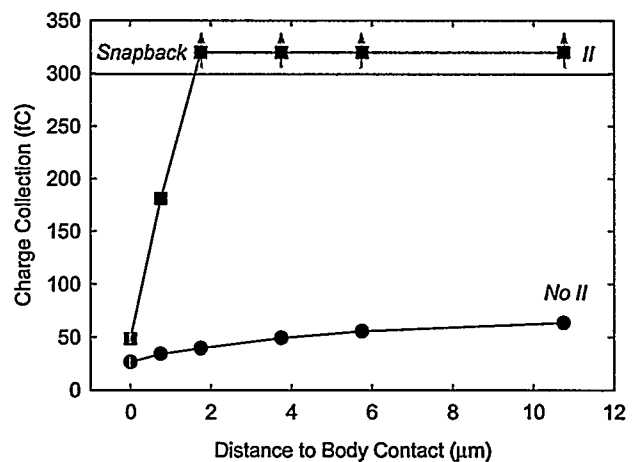


Figure 2. Simulated total drain charge collection in n-channel transistors with BTS body ties. Results are shown with and without including the effects of impact ionization.

snapback mode would actually be observed in circuit operation will be discussed in the next section.

Simulated drain charge collection for n-channel BUSFETs that also have BTS body ties is shown in Figure 3. The characteristics are similar to those of the BTS alone, but due to the considerably more effective BUSFET body tie, snapback is not observed until the body contact is 7.75 μm from the body. This represents a more than fourfold increase in the maximum body contact spacing before the onset of snapback.

Single-Event Upset and Snapback in SOI SRAMs

SRAM cells incorporating the same n-channel body-tied transistors were also simulated in Davinci. Gate strikes to the “off” biased n-channel transistor in a six-transistor SRAM cell were simulated, with the other transistors modeled in the circuit domain. Impact ionization was included in all SRAM simulations.

The calculated SEU thresholds as a function of distance to the body contact for BTS structures are shown in Figure 4 for SRAMs with no feedback resistors and with 100 k Ω resistors. As expected, the upset threshold drops as the distance between the body and the body contact increases, because the body tie becomes less effective at preventing the body potential from floating. Again, the results at long distances are indicative of the expected behavior of non-body-tied transistors. For body contacts farther than 5.75 μm from the body, simulations predict that single-event snapback (SES) will indeed occur in these SRAM circuits. For SES to occur, the SES threshold must be below the SEU threshold, creating a window of SES vulnerability. Once

the SEU threshold is passed, snapback no longer occurs because the drain bias switches from 3 V to 0 V and is unable to sustain impact ionization. The onset of SES occurs at the same LET for both cells with and without feedback resistors. The onset of SES appears to have no dependence on resistor value, thus the window for SES vulnerability increases as the upset threshold increases. For example, without feedback resistors SES is predicted to occur for LETs between 2 and 6 MeV-cm²/mg, but with 100 k Ω resistors, the window opens to LETs between 2 and 20 MeV-cm²/mg.

Figure 5 shows the results of similar simulations for SRAMs using the BUSFET structure. For the body contact spacings simulated here, we do not see SES in the BUSFET SRAMs, but at larger body contact spacings it is expected that SES would eventually occur.

IV. DISCUSSION

The simulations clearly show the dramatic effects of various body tie configurations on the single-event susceptibility of SOI circuits. Not surprisingly, it is very important to consider impact ionization effects in deep submicron SOI circuits, with the simulations predicting the occurrence of SES for cases where the body contacts are too far away from the body region. This result has implications for commercial SOI circuits that may not use body ties. In the full paper we will report the results of experiments to determine if presently available SOI ICs exhibit SES. The results also have implications for present hardness assurance screens, where current-monitoring latchup tests (which might also be capable of

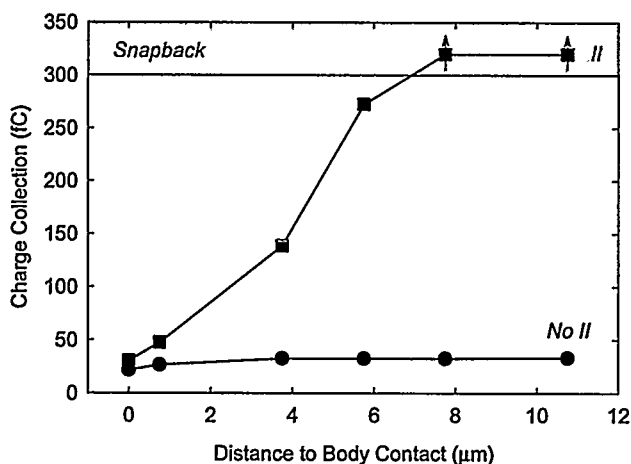


Figure 3. Simulated drain charge collection in n-channel BUSFETs with BTS body ties with and without impact ionization effects.

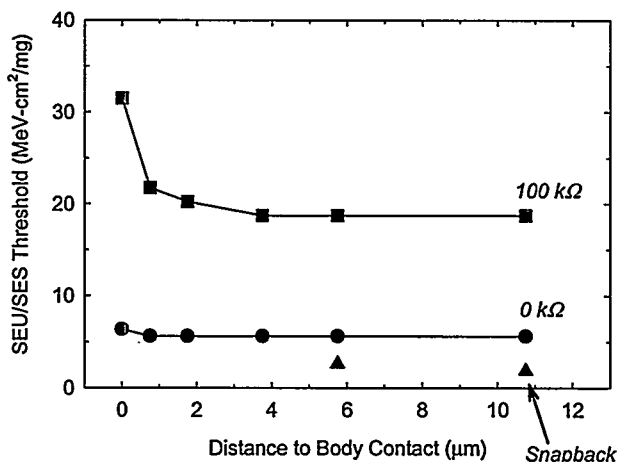


Figure 4. Simulated SEU and SES thresholds for SOI SRAMs using BTS body ties as a function of body contact distance from body. The threshold for SES (red triangles) is the same for both the 0 k Ω and the 100 k Ω SRAMs.

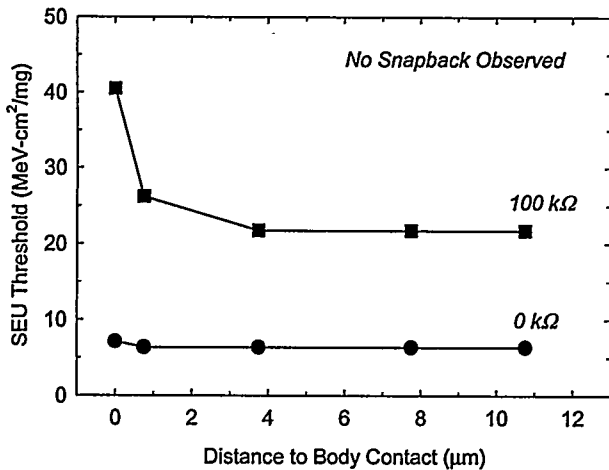


Figure 5. Simulated SEU threshold for SOI SRAMs using BUSFETs in combination with BTS body ties.

detecting snapback) may not even be performed on SOI devices because they are assumed to be latchup immune. Even if latchup tests are performed, they may not probe the window of SES vulnerability, which exists only below the SEU threshold. Note also that the present simulations were performed at worst-case bias for SEU (nominal voltage minus 10%), but the worst-case bias for SES is actually nominal voltage plus 10%, further opening the SES window.

In cases where SES occurs, the simulations predict degraded logic levels (drain voltage drops from 3 V to a level when latched of 2.4 V). In this case, the memory cell contents would be read correctly, but power consumption would increase as the SRAM cell draws a static current after SES of about 0.2 mA. A write of the cell to the opposite state would clear the snapback condition [3]. Whether the increase in static power consumption would be a serious problem depends on the individual application, and how many SES events might accumulate before being cleared. However, continued operation in this impact ionization regime is not desirable as it leads to hot-carrier induced degradation of the gate oxide [11] and possible charging of the BOX.

In this summary, we have simulated very narrow channel devices (0.75 µm). In conventional BTS structures that are tied only at the ends of the channel, body tie effectiveness depends not only on the distance from the body tie contact to the body region, but also the distance from the edge of the channel to the center of the gate. An inherent tradeoff thus exists between device width and body tie proximity. For the results shown in Fig. 4, the maximum total distance from the body tie

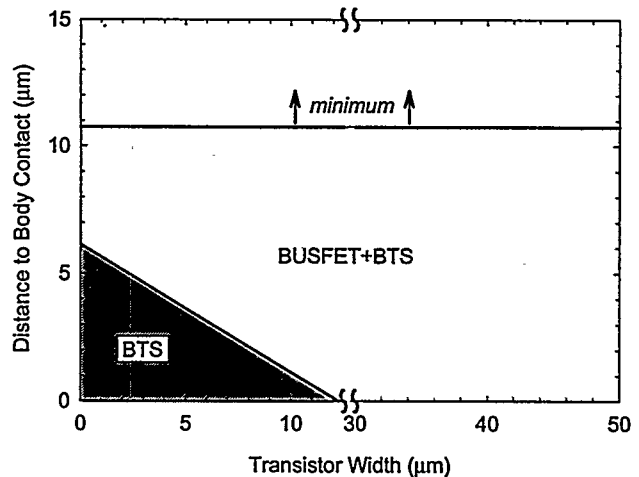


Figure 6. Design tradeoff between transistor width and distance to body contact for BTS and BUSFET structures.

contact to the center of the gate ($\Delta + W/2$) before SES is observed is about 6 µm. For wider transistors, Δ must be reduced to prevent SES. This “design window” is presented graphically as the triangular hatched region in Figure 6. For the BUSFET, width is not really an issue since the transistor is tied underneath the source at a distance Δ no matter the transistor width. This gives the BUSFET a much wider design space, as depicted by the shaded region in Figure 6. Impacts of device width will be explored further in the full paper.

V. CONCLUSIONS

Body tie layout greatly affects the SEU characteristics of SOI ICs. Simulations predict that for deep submicron SOI devices with poor or no body contacts, single-event snapback is likely to occur, resulting in degraded logic levels and increased static power consumption. Device width is coupled to body tie design for conventional body ties and can result in small design windows. The BUSFET may give a larger design space, but with some increase in fabrication complexity.

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