Single hole quantum dot transistors in silicon

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Novel *p*-channel quantum-dot transistors were fabricated in silicon-on-insulator. Strong oscillations in the drain current as a function of the gate voltage have been observed at temperatures over 81 K and drain biases over 66 mV. The oscillations are attributed to holes tunneling through the discrete single hole energy levels in the quantum dot. Measurements show that the average energy level spacing is ~35 meV. Simple modeling indicates that about two thirds of the energy level spacing come from the Coulomb interaction between holes (i.e., hole Coulomb blockade) and one third from the quantum confinement effect. The realization of single hole quantum-dot transistors opens new possibilities for innovative circuits that utilize complementary pairs of quantum-dot transistors. © *1995 American Institute of Physics.*

In exploring the limits of semiconductor transistors and searching for innovative devices, several electron quantum-dot transistors in silicon have been demonstrated.[1–3] The strong oscillation in the drain current is due to interplay between the quantum confinement effect and Coulomb blockade effect of electrons.[2] The possibility of hole Coulomb blockade has been speculated for some time,[4] however, it has not been demonstrated in any transistor albeit some studies on hole effects in Si–SiGe diodes.[5,6] Here, we report novel *p*-channel quantum-dot transistors in silicon that have shown single hole Coulomb blockade as well as hole quantum size effect at temperatures over 81 K.

The *p*-channel quantum-dot transistors were fabricated on a silicon-on-insulator (SOI) wafer that was made using separation by implanted oxygen (SIMOX). The top silicon thickness is 70 nm and has a boron concentration of 3×10^{15} cm^{-3}. However, as shown later, the quantum dot is virtually undoped due to its extremely small dimensions. In fabrication, the quantum dot with an abacus bead shape was first etched into the top silicon layer, using electron beam lithography and reactive ion etching, as shown in Fig. 1. It was followed by oxidation of 41 nm thick gate oxide, and deposition and patterning of a rectangular polycrystalline silicon gate to cover the entire quantum dot and constrictions as seen in Fig. 1. The fabrication process is identical to that of the electron quantum-dot transistors in silicon,[2] except that the source, the drain, and the polycrystalline silicon gate were doped with BF_2 implantation. After the fabrication, the actual size of the silicon bead was studied by etching away the gate oxide in diluted HF and was found to be ~10 nm wide, 30 nm long, and 30 nm thick (Fig. 2). The average dopant inside the quantum dot can then be calculated by multiplying the quantum dot volume with the average doping concentration which becomes 0.03 dopant per quantum dot. In other words, the quantum dots are virtually undoped and the effects observed in the transistors have nothing to do with the dopants in the channel.

The *p*-channel quantum-dot transistors were measured in dc with an HP4145B and in a variable temperature chamber. The gate was biased negatively, inducing holes in the quantum dot channel, while the drain was biased negatively to drive holes from the source to the drain. As the gate voltage was scanned, the drain current (i.e., the hole current) oscillated (Fig. 3). The oscillation is due to holes tunneling through the discrete single hole energy levels in the quantum dot. The current peaks when the Fermi level in the source is aligned with a single hole energy level in the quantum dot. The current valleys when the Fermi level is in between two hole energy levels. Since the hole current oscillation persists at temperatures over 81 K and thermal broadening is about $4k_BT$, where k_B is the Boltzman constant and T is the temperature, the average hole energy level spacing in the quantum dot is estimated to be over 30 meV. The energy level spacing can also be estimated from the temperature dependent study of the thermal activation of the valley current,[7] from which we found the energy level spacing to be 33 meV in agreement with the thermal broadening study.

The drain bias effect on the oscillation is shown in Fig. 4. Due to the large energy level spacing, the ratio of the peak to valley current at 1 mV drain bias can be well over 10 000, and the oscillation can be clearly observed at a drain bias over 66 mV.

The hole QDTs with a variety of quantum-dot sizes were fabricated. It has been observed that the operating temperatures as well as the peak-to-valley current ratio depend on the

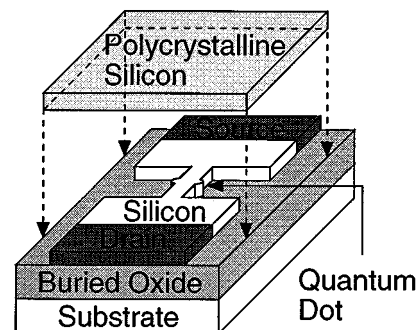

FIG. 1. Schematic of the single hole transistors with the quantum dot separated from the source and drain by two constrictions. The polycrystalline silicon covers the entire quantum dot.

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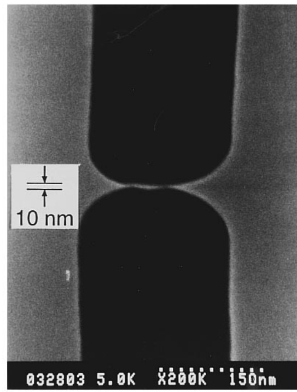

FIG. 2. Scanning electron micrograph of the silicon quantum dot after oxidation and removal of the gate oxide. The dot is 10 nm width, 30 nm long, and 30 nm thick.

dot size. The smaller the dot size, the higher the operation temperatures and the larger the peak-to-valley ratio will be. The details of the quantum-dot size effects will be discussed elsewhere.[8]

One of the key issues here is the cause for the large energy level spacing in the single hole quantum dot. As shown below, approximately two thirds of the energy level spacing are due to the single hole Coulomb blockade effect and one third is due to the hole quantum confinement effect in the silicon quantum dot. The Coulomb charging energy can be estimated from the total device capacitance, which roughly consist of the three capacitances: the capacitance from the quantum dot to (a) the gate, (b) the source, and (c) the drain. From the average oscillation period in the current versus gate voltage characteristics, 83 mV, the capacitance between the quantum dot and the gate capacitance can be roughly estimated to be 1.9 aF. This capacitance also can be estimated from the quantum dot size (~10 nm by 30 nm by 30 nm) and the gate oxide thickness, and the result is consistent. The capacitance between the quantum dot and the source is roughly estimated from the Coulomb gap in the drain current versus the drain voltage plot,[1] and was found to be 2.3 aF, assuming it is the same as that between the quantum dot and the drain. Summing up all the capacitances, the total capacitance is 6.5 aF and the Coulomb energy is 25 meV or approximately two thirds of the total energy level spacing.

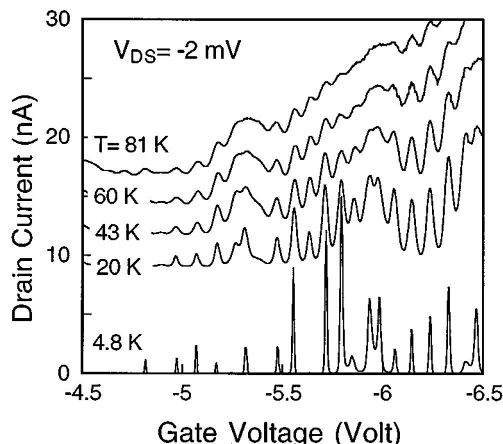

FIG. 3. The drain current vs the gate voltage of a hole quantum dot transistor in silicon at various temperatures. The curve has been displaced for clarity.

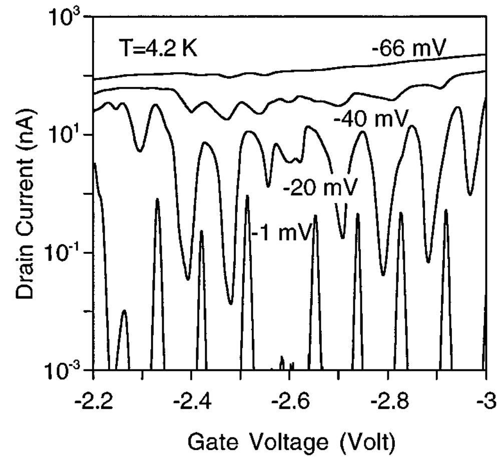

FIG. 4. The drain current vs the gate voltage at different drain biases up to 66 mV at 4.2 K.

The spacing between the hole quantum confinement energy levels is calculated to be about 10 meV from the dot size using simple quantum box model and by assuming hole effective mass to be half of the free-electron mass. It can also be estimated from the peaks splitting seen at higher drain bias due to the hole quantum confinement energy levels.[9] From Fig. 4, we observe that at 20 mV drain bias, each peak in general splits into two or three peaks indicating there are two or three hole quantum confinement energy levels.Therefore, the hole quantum confinement energy level spacing is ~7–10 meV in agreement with the simple quantum box model. It is also approximately one third of the total energy level spacing.

Undoubtedly, the realization of single hole quantum-dot transistors opens new possibilities for innovative circuits which utilize complementary pairs of quantum-dot transistors.

In summary, novel single hole quantum-dot transistors in silicon have been fabricated with the processes which are compatible with that of single electron quantum-dot transistors. Strong drain current oscillations due to hole tunneling through the discrete single hole levels in the quantum dots have been observed at temperature over 81 K and a drain bias over 66 mV. The energy level spacing inside the quantum dot is about 35 meV, and roughly two thirds of the energy are due to Coulomb interaction and one third is due to quantum confinement effect. We believe that the operation temperature and bias of the hole quantum-dot transistors can be further increased by reducing the quantum dot size.

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