*Research Article*

# Single-Input Four-Output Current Mode Filter Using Operational Floating Current Conveyor

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This paper presents operational floating current conveyor (OFCC) based single input four output current mode filter. It employs only three OFCCs and two grounded capacitors and resistors each. The MOS based grounded resistors implementation is used, which adds feature of electronic tunability to the filter parameters. The filter also enjoys low component spread and low sensitivity performance. The effect of finite transimpedance and parasites of OFCC on the proposed circuit is also analyzed. The functionality of the proposed circuit is demonstrated through SPICE simulations using $0.5\,\mu$m CMOS process model provided by MOSIS (AGILENT).

## 1. Introduction

The development of current mode continuous time filters has received growing interest due to its applications in sampled data systems, communications, and control systems [1, 2]. This is also in consonance with the trend of operating circuits at lower supply voltages where the current mode concept is more useful. The circuit operation in current mode circuits is decided by current which enables the system design to have wider dynamic range [3]. These circuits are also simple and compact as current addition/subtraction does not require additional circuit elements. Owing to the advantages of current mode filters, considerable research has directed towards the realization of single-input multiple output filters. A variety of current mode building blocks [4–10], namely, current follower transconductance amplifier [4], current conveyor [5–7], operational transconductance amplifier [8], $Z$ copy current follower transconductance amplifier [9], and $Z$-Copy Current Inverter Transconductance amplifier [10], have been used to implement these filters [1, 4–22]. The structures—use excessive number of elements [6, 7, 13, 15] some of the references cited in [17], do not present low input impedance [1, 8, 13–16, 19] which is necessary for a current mode filter, employ multiple inputs to provide

output responses [15, 16], put matching constraint [7, 10, 15, 16] to obtain all five responses of universal filter, has less than three simultaneous output responses [4, 8, 15, 16, 21], employ different type of active blocks [12, 19, 20]. The operational floating current conveyor (OFCC) [23, 24], which was introduced as operational floating conveyor (OFC) [25], combines the features of current conveyor and the current feedback op-amp along with additional current outputs that add flexibility in the circuit design. Literature survey on OFCC based circuits [26–32] shows that voltage mode filter [26–28], variable gain amplifier [29], wheatsone bridge [30], and instrumentation amplifier [31] and read out circuit [32] are available. The study of current mode filters [1, 4–22] shows that no OFCC based current mode filter is available in the literature. Therefore, this paper aims at presenting a single-input four-output OFCC based current mode filter. The proposed filter uses three OFCCs, two grounded capacitors and two grounded resistors. The resistors are implemented using MOSFETs so as to achieve electronic tunability of filter parameters. The filter enjoys low component spread and low sensitivity performance. The proposed circuit is also analyzed to take finite transimpedance and parasites of OFCC into account. The functionality of the proposed circuit

TABLE 1: Transistors aspect ratios of the circuit shown in Figure 2.

| Transistor | $W\,(\mu m)/L\,(\mu m)$ |
|---|---|
| $M1, M2$ | 50/1 |
| $M3, M4, M11, M12, M14$ $M16, M18, M20, M22, M24$ | 50/2.5 |
| $M5, M7, M10, M15, M17, M19$ $M21, M23, M25$ | 20/2.5 |
| $M6, M8$ | 40/2.5 |
| $M9, M13$ | 100/2.5 |

is demonstrated through SPICE simulations using $0.5\,\mu m$ CMOS process model provided by MOSIS (AGILENT).

## 2. Circuit Description

*2.1. OFCC.* The circuit symbol of operational floating current conveyor (OFCC) [23, 24] is shown in Figure 1. It has a low impedance current input port $X$ and a high impedance voltage input port $Y$. It also has a low impedance voltage output port $W$ and high impedance current output ports $Z1$, $Z2$, $Z3$, and $Z4$. The output voltage at port $W$ is multiplication of input current at port $X$ and the open loop transimpedance gain $Z_t$. The port relationships of the OFCC is characterized by the following matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ V_W \\ I_{Z1} \\ I_{Z2} \\ I_{Z3} \\ I_{Z4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ I_W \\ V_{Z1} \\ V_{Z2} \\ V_{Z3} \\ V_{Z4} \end{bmatrix}. \tag{1}$$

It may be noted that the voltage at port $X$ is the same as input voltage at port $Y$, so voltage tracking action is available at input port. The output current flowing through port $W$ is copied to ports $Z1$ and $Z2$ in phase and to ports $Z3$ and $Z4$ out of phase, thereby offering current tracking at the output ports. Figure 2 shows the CMOS based schematic of OFCC which is based on topology proposed in [29].

*2.2. Proposed Filter.* In this section the implementation of OFCC based current mode single-input four-output filter, as shown in Figure 3, is proposed. It employs three OFCCs, and two grounded capacitors and resistors each. The analysis of the circuit gives the following transfer functions:

$$T_{\text{LPF1}} = T_{\text{LPF2}} = \frac{I_{\text{LPF1}}}{I_{\text{in}}} = \frac{I_{\text{LPF2}}}{I_{\text{in}}} = \frac{-1}{D(s)}, \tag{2}$$

$$T_{\text{BPF}} = \frac{I_{\text{BPF}}}{I_{\text{in}}} = \frac{-sC_2 R_2}{D(s)},$$

$$T_{\text{HPF}} = \frac{I_{\text{HPF}}}{I_{\text{in}}} = \frac{-s^2 C_1 C_2 R_1 R_2}{D(s)}, \tag{3}$$

$$T_{\text{NOTCH}} = \frac{I_{\text{NOTCH}}}{I_{\text{in}}} = \frac{s^2 C_1 C_2 R_1 R_2 + 1}{D(s)},$$

where

$$D(s) = s^2 C_1 C_2 R_1 R_2 + sC_2 R_2 + 1. \tag{4}$$

Thus the proposed circuit provides low pass, band pass, and notch (band stop) response simultaneously at high impedance. It may be noted that the current $I_{\text{HPF}}$ is not explicitly available at high impedance and therefore cannot be used directly. However, by connecting $I_{\text{NOTCH}}$ and $I_{\text{LPF1}}$, the high-pass response can be made available at high output impedance. This arrangement makes low pass, band pass, and high-pass responses available simultaneously. Similarly, the all pass function can easily be obtained by connecting band pass and notch output currents, that is, $I_{\text{AP}} = I_{\text{BP}} + I_{\text{NOTCH}}$, and the corresponding transfer function is obtained as

$$T_{\text{AP}} = \frac{I_{\text{AP}}}{I_{\text{in}}} = \frac{s^2 C_1 C_2 R_1 R_2 - sC_2 R_2 + 1}{D(s)}. \tag{5}$$

It may be noted that all the five filter responses can be made simultaneously available by adding $Z$ stages in 2nd OFCC (Figure 3). Further, there is no matching constraint for realization of filter responses.

All the responses are characterized by pole frequency ($\omega_0$), bandwidth ($\omega_0/Q_0$), and quality factor ($Q_0$) given as

$$\omega_0 = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}},$$

$$\text{BW} = \frac{\omega_0}{Q_0} = \frac{1}{R_1 C_1}, \tag{6}$$

$$Q_0 = \sqrt{\frac{R_1 C_1}{R_2 C_2}}.$$

Equation (6) reveals that the pole frequency ($\omega_0$) and quality factor ($Q_0$) can be adjusted by $R_2$, without disturbing $\omega_0/Q_0$. The orthogonal adjustability of $\omega_0$ and $Q_0$ can be achieved by simultaneous adjustment of $R_1$ and $R_2$ such that the product $R_1 R_2$ remains constant and the quotient $R_1/R_2$ varies and vice versa. With moderate values of ratios of component values $((R_1/R_2) = (C_1/C_2) = Q_0)$, that is, from low component spread [34], high values of $Q$-factor can be obtained. Hence the component spread is of the order of $\sqrt{Q_0}$.

The proposed filter uses grounded resistors which can easily be implemented using the MOS based structure given in Figure 4 [33]. It uses two diode connected matched transistors, operating in saturation region. Assuming $V_1 = -V_2$, the value of resistor is given by

$$R = \frac{L}{2\mu C_{\text{ox}} W (V_1 - V_T)}, \tag{7}$$

where $\mu$ is carrier mobility, $C_{\text{ox}}$ is gate capacitance per unit area, $V_T$ is threshold voltage, and $W$, $L$ are the channel width and length respectively.
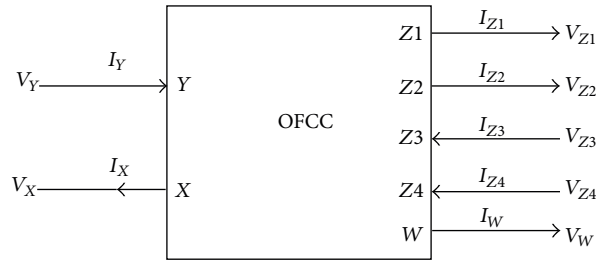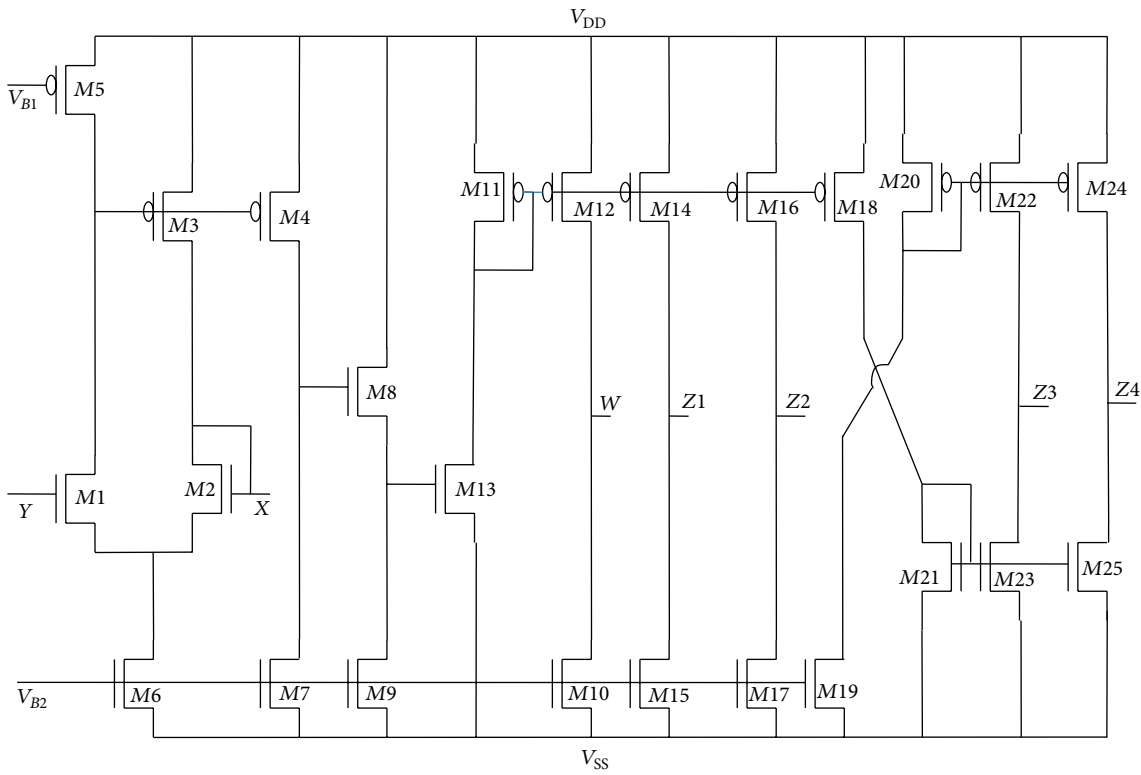
FIGURE 1: Circuit symbol of OFCC.
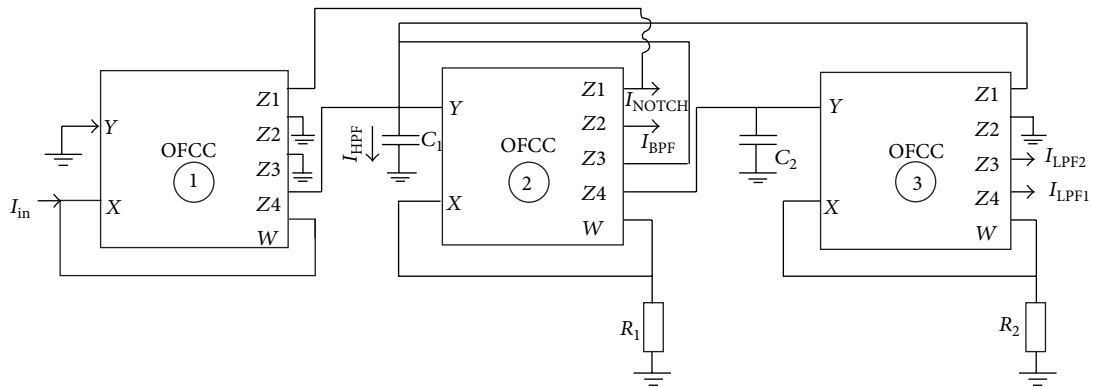


FIGURE 2: CMOS schematic of OFCC [29].



FIGURE 3: Proposed OFCC based single-input four-output current mode filter.

TABLE 2: Bias voltages/resistor values for orthogonal adjustment of $f_0$ and $Q_0$.

| $V_{11}$ *(V) | $V_{21}$ *(V) | $R_1$ (KΩ) | $V_{12}^*$(V) | $V_{22}^*$(V) | $R_2$ (KΩ) | $Q$ | $F$ (KHz) |
|---|---|---|---|---|---|---|---|
| 1.310 | −1.310 | 1 | 1.310 | −1.310 | 1 | 1 | 1590 |
| 0.869 | −0.869 | 2 | 0.869 | −0.869 | 2 | 1 | 800 |
| 0.726 | −0.726 | 5 | 0.726 | −0.726 | 5 | 1 | 320 |
| 0.711 | −0.711 | 10 | 0.711 | −0.711 | 10 | 1 | 160 |

*$V_{1i}$ and $V_{2i}$ refer to bias voltages corresponding to resistance $R_i$.

TABLE 3: Bias voltages/resistor values for orthogonal adjustment of $Q_0$ with $f_0$.

| $V_{11}$ *(V) | $V_{21}$ *(V) | $R_1$ (KΩ) | $V_{12}$ *(V) | $V_{22}$ *(V) | $R_2$ (KΩ) | $C_1$ (nF) | $C_2$ (nF) | $Q$ | $F$ (KHz) |
|---|---|---|---|---|---|---|---|---|---|
| 1.310 | −1.310 | 1 | 0.869 | −0.869 | 2 | 0.1 | 0.2 | 0.5 | 800 |
| 0.869 | −0.869 | 2 | 0.869 | −0.869 | 2 | 0.1 | 0.1 | 1 | 800 |
| 0.869 | −0.869 | 2 | 1.310 | −1.310 | 1 | 0.2 | 0.1 | 2 | 800 |

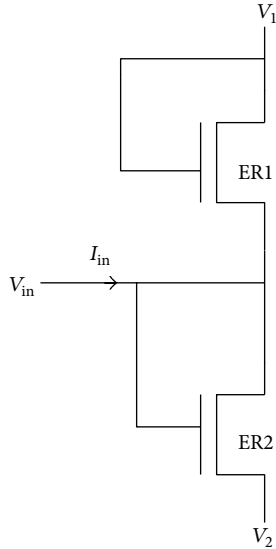*$V_{1i}$ and $V_{2i}$ refer to bias voltages corresponding to resistance $R_i$.



FIGURE 4: MOS realization of a resistor [33].

The sensitivity analysis of the proposed circuit is as follows:

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_2}^{Q} = S_{C_2}^{Q} = -\frac{1}{2},$$

$$S_{R_1}^{Q} = S_{C_1}^{Q} = -S_{R_2}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}. \qquad (8)$$

Thus the all passive sensitivities are not more than unity in magnitude. So the proposed filter circuit can be classified as insensitive.

### 2.3. Effect of Finite Transimpedance Gain.
In this section the effect of finite transimpedance gain of OFCC is considered and compensation is employed for high frequency applications. Ideally the transimpedance gain $Z_t$ is assumed to approach infinity. However, in practice, $Z_t$ is a frequency dependent finite value. Using single pole model for transimpedance gain, $Z_t(s)$ is expressed as [29]

$$Z_t(s) = \frac{Z_{to}}{1 + (s/\omega_{tc})}. \qquad (9)$$

The parameter $Z_{to}$ is the DC open loop transimpedance gain and $\omega_{tc}$ is the transimpedance cutoff frequency. For high frequency applications, the transimpedance gain, $Z_t(s)$, is approximated as

$$Z_t(s) \cong \frac{1}{sC_p}, \qquad (10)$$

where

$$C_p = \frac{1}{Z_{to}\omega_{tc}}. \qquad (11)$$

Taking single pole model of $Z_t(s)$ into account, the low pass transfer function of (2) modifies to

$$T_{LPF1} = T_{LPF2} = \frac{I_{LPF1}}{I_{in}} = \frac{I_{LPF2}}{I_{in}} = \frac{-1}{D_n(s)}, \qquad (12)$$

where

$$D_n(s) = s^2 R_1 \varepsilon_1(s) R_2 \varepsilon_2(s) C_1 C_2 + sR_2\varepsilon_2(s) C_2 + 1,$$

$$\varepsilon_1(s) = \frac{1}{1 + sC_p R_1}, \qquad \varepsilon_2(s) = \frac{1}{1 + sC_p R_2}. \qquad (13)$$

The inclusion of a capacitor of value $C_p$ connected between the terminal $W$ and ground in second and third OFCCs cancels the coefficient of "$s$" thereby making both $\varepsilon_1(s)$ and $\varepsilon_2(s)$ equal to unity. Thus the transfer function of low pass filter after compensation reduces to (2). Similar analysis is valid for other responses as well.

### 2.4. Effect of Other Nonidealities.
The second group of non-idealities comes from parasites of OFCC comprising of resistances and capacitances connected in parallel at terminals
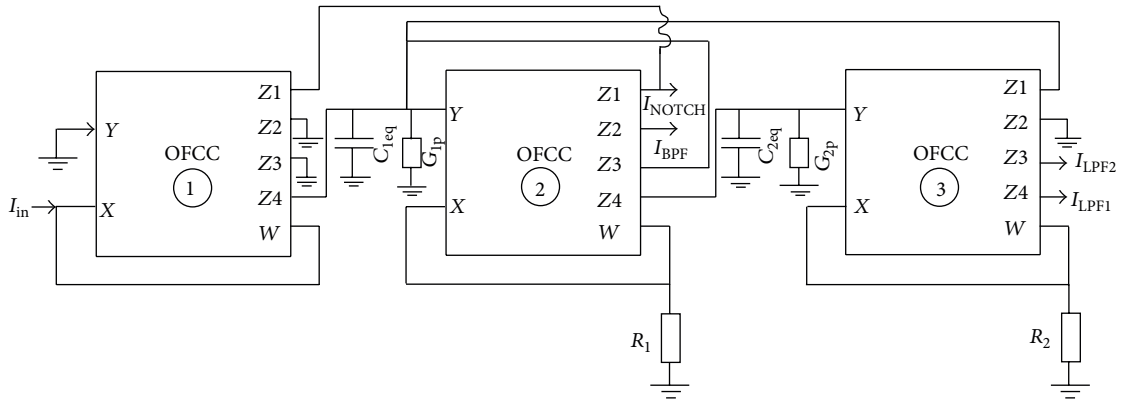
FIGURE 5: Proposed OFCC based current mode filter with parasites.
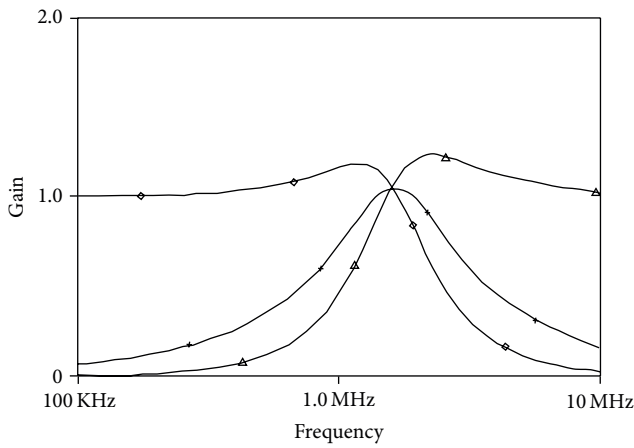


FIGURE 6: Simulated low pass, band pass, and high-pass responses.
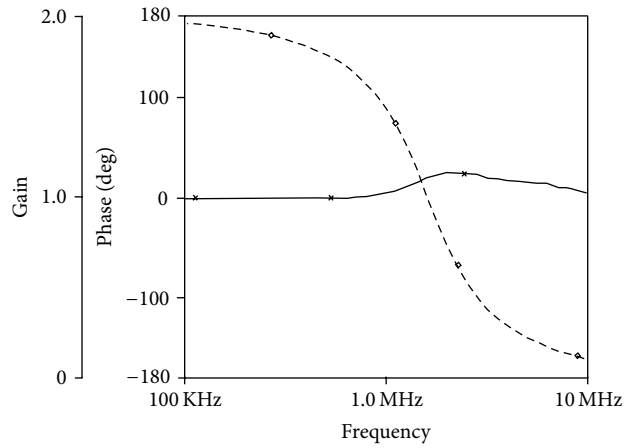


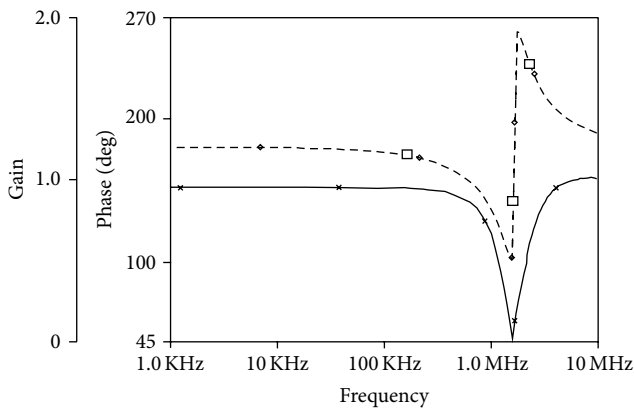FIGURE 8: Magnitude and phase plots for all-pass response.



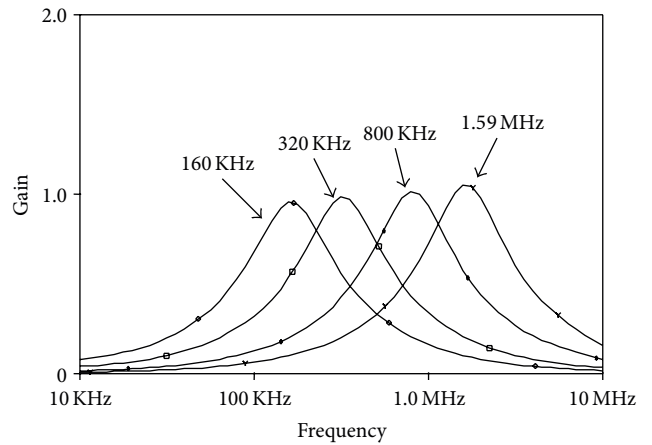FIGURE 7: Magnitude and phase plot for notch response.



FIGURE 9: Tuning of $f_0$.

$Y$, $Z1$, $Z2$, $Z3$, and $Z4$ (i.e., $R_Y$, $C_Y$, $R_z$, $C_Z$). The effects of these parasites on filter response depend strongly on circuit topology. The proposed filter topology of Figure 3 in the presence of these parasites modifies to Figure 5 where $C_{1eq} = C_1//C_{Y1}//C_{Z41}//C_{Z31}//C_{Z13}$, $C_{2eq} = C_2//C_{Y3}//C_{Z42}$, $G_{1p} = 1/(R_{Z41}//R_{Z31}//R_{Z13})$, and $G_{2p} = 1/(R_{Y3}//R_{Z42})$;

the subscript $i$ (=1, 2, 3) refers to parasites of $i$th OFCC and $j$ denotes $j$th $Z$ terminal. It may be noted that effect of parasitic capacitances can be accommodated by pre adjusting the value of external capacitor. The parasitics introduce poles at $G_{1P}/C_{1eq}$ and $G_{2P}/C_{2eq}$. So by choosing operating frequencies
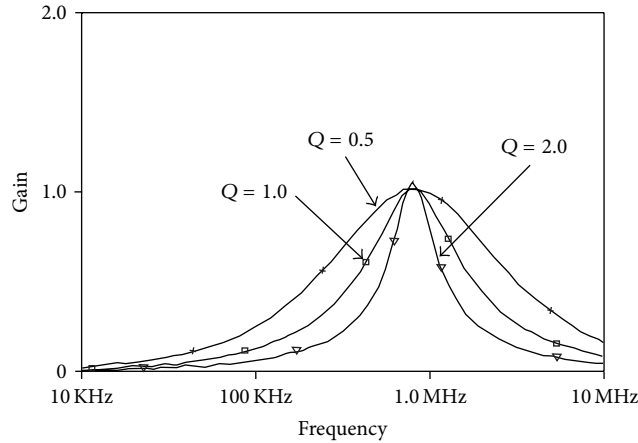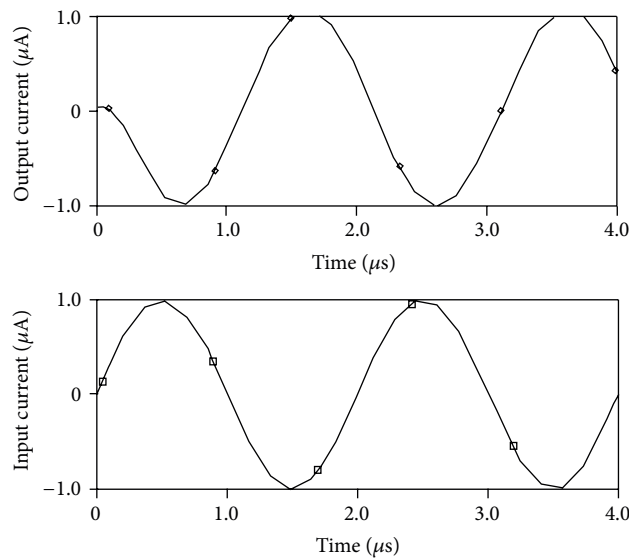
FIGURE 10: Tuning of $Q_0$.



FIGURE 11: Transient response for low pass output.

## 3. Simulation Results

To verify the functionality of the proposed OFCC based current mode filter, SPICE simulations have been carried out using 0.5 $\mu$m CMOS process model provided by MOSIS (AGILENT) and CMOS schematic of Figure 2 with power supply voltage of $V_{DD} = -V_{SS} = 1.5$ V and $V_{B1} = -V_{B2} = 0.8$ V. The aspect ratios of the transistor are reported in Table 1 [29].

The simulations have been performed for a pole frequency of 1.59 MHz with component values as $C_1 = C_2 = 100$ pF and MOS based resistors of value 1 $k\Omega$ by selecting bias voltages as ±1.310 V. Figure 6 shows the simulation results for low pass, band pass, and high-pass responses. The phase and magnitude plots for notch and all pass responses are depicted

in Figures 7 and 8, respectively. The responses confirm the theoretical predictions.

The orthogonal adjustment of $f_0$ with $Q_0$ is depicted in Figure 9 where the value of $Q_0 = 1$ is considered. The capacitors $C_1$ and $C_2$ are taken as 100 pF and the bias voltages along with the resistor values for different values of $f_0$ as given in Table 2. Figure 10 shows orthogonal adjustment of $Q_0$ with $f_0 = 800$ kHz. The values of $Q_0$ for constant value of $f_0$ as obtained with $C_1 = C_2 = 100$ pF and bias voltages and resulting resistor values are listed in Table 3.

To study the time domain behavior of the proposed filter, an input sinusoidal signal of 500 KHz frequency and amplitude 2 $\mu$A is applied. The transient response for low pass output is shown in Figure 11. To show the effectiveness of proposed filter a mixed sinusoidal signal of frequencies of 50 KHz, 500 KHz, and 4 MHz having amplitude of 2 $\mu$A each is applied at the input of the filter. The transient response with its spectrum for input and output signals is shown in Figures
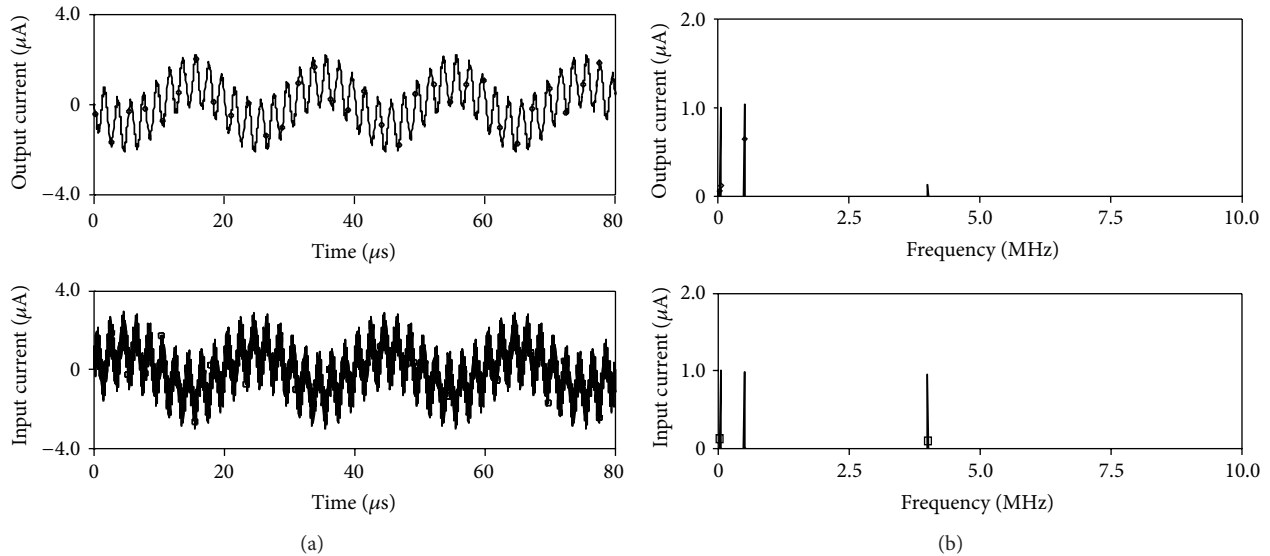
Figure 12: (a) Transient response of input and output signals (b) Spectrum of input and output signals.

12(a) and 12(b). It is clear that the 50 KHz, and 500 KHz signals are passed without attenuated and 4 MHz signal is significantly attenuated.

## 4. Conclusion

In this paper, a single-input four-output current mode filter based on OFCC is presented. The circuit uses only three OFCCs, two grounded resistors, and two grounded capacitors. The low pass, band pass and notch responses are available at high impedance whereas high-pass and all pass responses can be obtained by adding $Z$ stages in the second OFCC. The filter parameters are tuned electronically via MOS based grounded resistor. The effect of finite transimpedance and parasites on filter parameters is also included.

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