Single-Phase Inverter with Common Grounded Feature and Connected into Grid

Naser Vosoughi Kurdkandi
Faculty of Electrical and Computer Engineering
University of Tabriz
Tabriz, Iran
Naser.vosoughi@tabrizu.ac.ir

Milad Ghavipanjeh Marangalu
Faculty of Electrical and Computer Engineering
University of Tabriz
Tabriz, Iran
M.ghavipanjeh@tabrizu.ac.ir

Yahya Naderi
Department of Electronics and Electrical Engineering
University of Strathclyde
Glasgow, United Kingdom
Yahya.naderi@strath.ac.uk

Seyed Hossein Hosseini,
Faculty of Electrical and Computer Engineering
University of Tabriz
Tabriz, Iran
Hosseini@tabrizu.ac.ir

Mehran Sabahi
Faculty of Electrical and Computer Engineering
University of Tabriz
Tabriz, Iran
Sabahi@tabrizu.ac.ir

***Abstract*—Transformer-less inverters are widely used in grid-tied photovoltaic (PV) applications due to their characteristics such as higher efficiency and lower price. In common-ground transformer-less PV inverters, the neutral point of grid is connected to the negative polarity of the PV panel directly to bypass the parasitic capacitances and to mitigate the leakage current. In this study, a single phase transformer-less grid-tied inverter is proposed and to obtain the unique characteristics of the recommended grid-connected topology, the series-parallel switching technique of the switched capacitor module in a packed unit is applied. Also, by utilizing the common grounding method, the leakage current is eliminated. The provided inverter can generate three-level output voltage waveform. To generate the switching gate pulses of utilized power switches, the peak current controller method is applied. The injected power flows (active and reactive powers) are adjusted using peak current control (PCC) method. Finally, a completely adjusted sinusoidal current can be delivered to power grid. In the next section, the operation procedure, comparison results are presented. Finally, to verify the accurate operation and the theoretical equations of the proposed inverter, simulation results are presented.**

***Keywords* — common-ground topology, transformer-less inverter, grid-tied inverter, and switched-capacitor module.**

I. Introduction

Transformer-less PV inverters have an important role in grid-tied applications [1-3]. The main advantages of these kind of inverters compared with the transformer topologies are affordable price, higher efficiency, and appropriate power density [4, 5]. Controlling the leakage current injected to the power grid is one of the most important issues in the grid-tied inverters. The variable high frequency common mode voltage (CMV) of the inverter can produce as undesirable leakage current which can be clamped between the null of ac grid and the parasitic capacitor of the negative terminal of PV panel with the value of about 100nF per 1KW [6, 7]. Here, a resonant path is introduced between the output filter inductor and the parasitic capacitor. So that the quality of injected grid current will be bring down and the power losses will be increased. Regarding the above mentioned issues, to reduce the undesirable value of the leakage current, several effective techniques are presented. One of the simplest methods is using the bipolar pulse width modulation (PWM) technique or half-bridge (HB) topologies in lieu of full-bridge (FB) one [7]. In the HB topologies the neutral point is connected to the central point of split capacitors directly. Accordingly, the CMV is close to half of input voltage [8]. To decrease the unwanted value of leakage current, the common grounded inverts are presented in [1-3]. By connecting the neutral point of power grid to the negative polarity of the PV panel directly, the common mode voltage is clamped to zero. The aim of this study is to propose a new type of single-phase common grounded inverter without using any isolated transforms. Also, it can enhance the efficiency of the proposed inverter by its voltage boosting feature and unipolar PWM technique. Also, through a switched-capacitor module and the virtual dc link method, a two times voltage boosting feature can be achieved without using any additional bulky inductors. To improve the quality of injected grid current and control the active power flow, a peak current controller (PCC) method is applied. This study is organized as: the proposed inverter topology and its operation modes are presented in section II in details. Section III explains the applied PCC strategy in full. Section IV, presents the calculation of utilized circuit components. The comparison of the provided topology with other conventional grid-connected inverters is presented in section V. To confirm the performance of the provided inverter, some simulation results are obtained by Matlab/Simulink software in section VI. Last but not the least, the conclusion of the paper is made in section VII.

II. Proposed Topology

The proposed three-level grid-tied inverter shown in Fig.1consists of 6 power switches (S_1~S_6), 3 diodes (D_1~D_3), and 3 capacitors (C_1~C_3). This new topology is modulated using single-bound hysteresis technique. Integrating switched-capacitor based module in the structure, the proposed inverter can boost the amplitude of input dc voltage source (PV panel) within a single stage. All of the utilized power switches in this structure are unidirectional. As shown in Fig.1, the negative polarity of the PV panel is connected to the null of the power grid directly. As a result, the provided inverter can be considered as a common grounded topology. To smooth the waveform of output current, an inductor is used as an L-type filter. In the proposed inverter the capacitor C_1 is charged to V_{PV} and both of the capacitors C_2 and C_3 are charged to $2V_{PV}$. Also, the peak value of the output voltage is equal to $2V_{PV}$. Assuming the same polarity for current and voltage of the grid, four operation modes can be considered

for the provided structure. The operation modes of the proposed three-level inverter are described in Fig. 2 (a) ~ (d).

Positive half cycle:

A) First operation mode

The equivalent electrical circuit of this operation mode is shown in Fig. 2(a) in which switches S_1, S_3, S_5 are in ON-state and the power diode D_2 is conducting. Here, the capacitor C_1 is in series with the input power supply (V_{PV}). The capacitor C_2 is charged to $2V_{PV}$ trough the input voltage power supply and capacitor C_1. Also, the input dc source and capacitor C_1 inject the power to the grid which will make the output voltage equal to $2V_{PV}$.

B) Second operation mode

The electrical circuit of this mode is depicted in Fig. 2(b). As shown in this figure, the switch S_2 is in ON-state and capacitor C_1 is charged to V_{PV}. Since in the previous operation mode the capacitor C_2 was charged to $2V_{PV}$, the energy of the capacitor C_2 is transmitted to capacitor C_3. So, the capacitor C_3 is charged to $2V_{PV}$. In order to generate the zero voltage level, the switches S_2, S_4 and S_5 are turned on in this mode. Also, the freewheeling current passes through switches S_4 and S_5.

Negative half cycle:

C) Third operation mode

Fig. 2(c) shows the equivalent electrical circuit of this mode. To produce the $-2V_{PV}$ level at the output voltage waveform, the switches S_1, S_3 and S_6 are in ON-state. In this mode, capacitor C_2 is charged to $2V_{PV}$ though the input dc source and capacitors C_1.

D) *Forth operation mode*

Fig. 2(d) indicates the electrical circuit of this mode. In this mode, the switch S_2 is turned on and capacitor C_1 is charged to the input voltage ($V_{C1}=V_{PV}$). The energy of the capacitor C_2 is transmitted to capacitor C_3. Therefore, the capacitor C_3 is charged to $2V_{PV}$. The freewheeling current passes through switches S_4 and S_5 which also generates the zero level of the output voltage waveform. It should be noted that during negative half cycle, the power injection into the grid is done by the capacitor C_3.

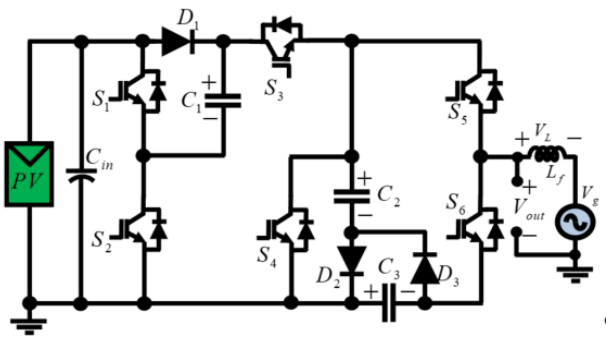
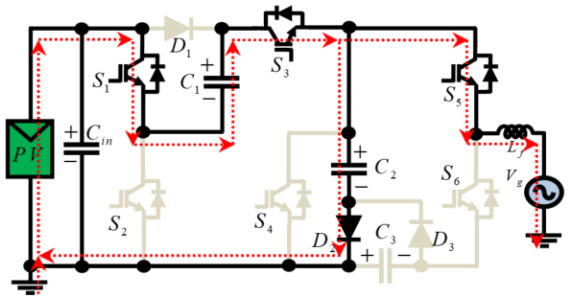


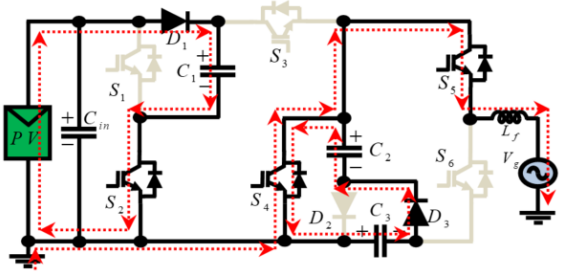
Fig. 1. Provided grid connected inverter.

III. Peak Current Control Strategy of the Proposed Grid-Tied Inverter

In the provided structure to obtain the switching gate pulses and adjust the injected grid power flows, a peak current control method is applied to the proposed inverter. The suggested controlling technique is depicted in Fig.3. In the provided structure, PV array is assumed as input power supply of the provided inverter. To obtain the maximum output power of PV panel, the maximum power point tracker (MPPT) unit is utilized in the provided control strategy. In order to detect the desired magnitude and phase angle of the grid, a phase locked loop (PLL) unit is required [1-3]. Here, by measuring the voltage and current of the PV panels and using the conventional perturb & observation (P&O) strategy, the maximum power of PV panel is obtained. Therefore, with respect to the required value of injected power flows, the needed phase and amplitude of injected grid current (the current reference (i_{ref})) are obtained. The obtained i_{ref} is delivered to the current controller unit, using which the peak current controller strategy is implemented. Comparing i_{ref} with the measured injected grid current (i_g), the switching gate pulses of the IGBTs are obtained. The operating of the provided inverter is a function of the polarity of the instantaneous value of the grid voltage (v_g). By allocating a given sampling time (T_{samp}), the grid current is compared with the i_{ref} obtained by the MPPT and PLL units within a T_{samp}. Considering the presented controlling technique, the grid current can follow the sinusoidal waveform of appropriate reference current accurately.



(a)



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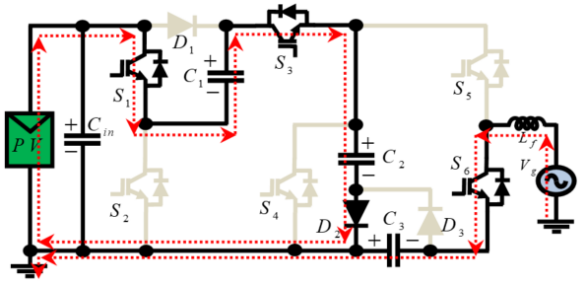
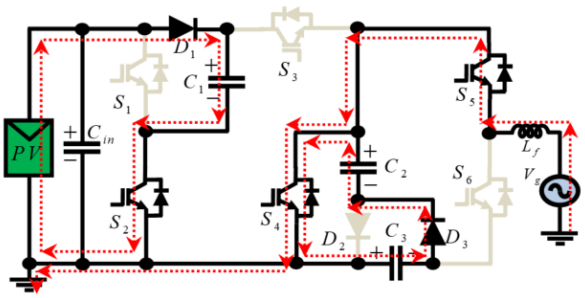


(c)



(d)

Fig. 2. Operational modes of the provided topology.

IV. Design Guide Lines

This section of the paper presents the desirable values of the output filter (L_f) and values of utilized capacitors (C_1~C_3).

A) Calculation of inductance of L-type filter

The equation of inductor output filter ($i_{Lf}(t)$) according to its across voltage ($V_L(t)$) and initial current ($i_{L_f}(0)$) can be written as;

$$i_{L_f}(t) = \frac{1}{L_f}\int_0^t V_L(t)dt + i_{L_f}(0) \tag{1}$$

The current ripple of the output filter (L_f) is obtained as;

$$\Delta I_{L_f} = \frac{(V_{out} - v_g).d}{f_s.L_f} \tag{2}$$

Using the inductor volt-second balanced technique for the voltage of the output filter during the full cycle of the switching period, the duty cycle and voltage gain of the proposed topology can be obtained as follows;

$$\int_0^{dT_s} (2V_{PV} - v_g)dt + \int_{dT_s}^{T_s} (-v_g) = 0 \tag{3}$$

$$d = \frac{v_g}{2V_{PV}} = \frac{V_{m,g}\sin\omega t}{2V_{PV}} \tag{4}$$

$$g = \frac{v_g}{V_{PV}} = 2d \tag{5}$$

Here, V_{out} indicates the inverter output voltage. Replacing (4) into (2), the current ripple of output filter can be calculated as follows;

$$\Delta I_{L_f} = \frac{(2.v_g.V_{PV}) - v_g^2}{2L_f.V_{PV}}.T_s \tag{6}$$

$$T_s = 2T_{samp} \tag{7}$$

Here, the T_s and f_s denote to time period of switching and switching frequency, respectively. When the grid voltage waveform is at its maximum value ($V_{m,g}$), the ripple of inductor current reaches its peak value and can be calculated as follows;

$$L_f = \left(\frac{2V_{PV}.V_{m,g} - V^2{}_{m,g}}{2V_{PV}.\Delta I_{L_{f,\max}}}\right).T_s \tag{8}$$

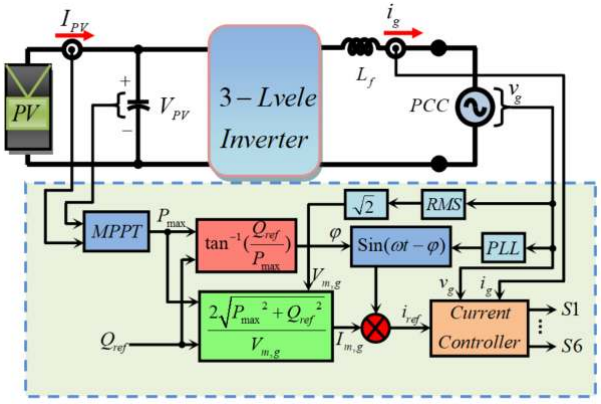


Fig. 3. Controlling system for provided inverter

B) Determination of capacitance of utilized capacitors

With regard to Fig. 2(a), during the first operation mode, the passing current of capacitor C_1 is equal to the inductor current. The capacitor voltage is written as follows;

$$V_{C_1}(t) = V_{C_1}(0) + \frac{1}{C_1}\int_0^t i_{C_1}(t)dt \tag{9}$$

Moreover, the capacitor C_1 voltage ripple is calculated as;

$$\Delta V_{C_1} = \left(\frac{i_L.v_g}{2V_{PV}.C_1}\right).T_s \tag{10}$$

The maximum value of the voltage ripple of capacitor C_1 is obtained when the grid voltage and the injected grid current are at their maximum values. Therefore, the value of C_1 is calculated as;

$$C_1 = \left(\frac{I_{m,g}\times V_{m,g}}{2\Delta V_{C_1,\max}\times V_{PV}}\right).T_s \tag{11}$$

By replacing the average values of grid voltage and current of output inductor filter during the half cycle of grid voltage waveform, the accurate value of capacitor C_1 can be written as;

$$C_1 = \left(\frac{4I_{m,g}\times V_{m,g}}{2\Delta V_{C_1}\times V_{PV}}\right).\frac{T_s}{\pi^2} \tag{12}$$

V. Comparison Results

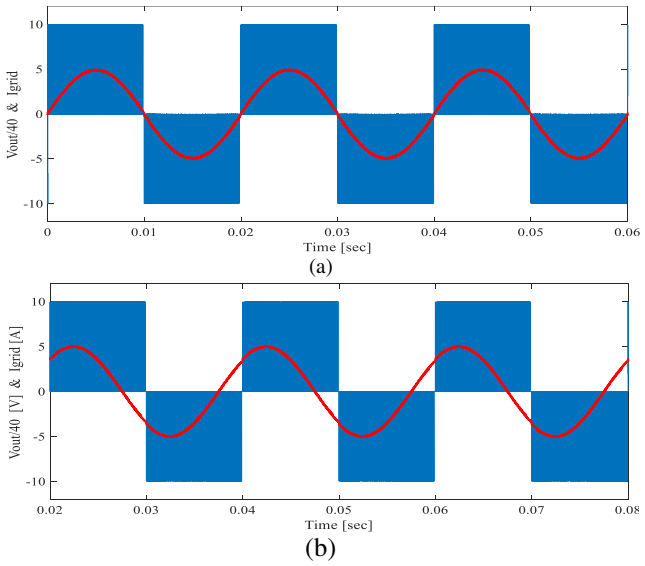
In this section to highlight the advantages of the suggested structure, the proposed grid-tied inverter is compared with other recently proposed grid-connected topologies. The summary of this comparison is presented in Table I. Hereon, number of all the utilized elements containing active and passive components besides some specifications such as voltage boosting capability, type of pulse width modulation (PWM) of inverters, number of ON-state power switches per each instant of the switching frequency, and the measured leakage current in different structures have been compared. With respect to Table I, none of the compared structures have step-up voltage feature. However, the proposed topology can increase the input voltage without any extra boosting stage. Considering Table I, the topologies cannot totally repress the generated leakage current whereas, the proposed inverter can eliminated the leakage current completely. It can be concluded that, the proposed topology is a suitable topology for grid-tied PV applications.

Table I. comparison of the proposed inverter with some other grid-tied inverters

topology	NO. of switches	NO. of diodes	NO. of capacitors	NO. of inductors (L_f)	PWM modulation	Boosting capability	leakage current
H6 [9, 10]	6	2	1	2	unipolar	NO	46mA
HERIC	5	2	-	2	unipolar	NO	83mA
OH5 [11]	6	-	1	2	unipolar	NO	45mA
H5	5	-	-	2	unipolar	NO	88mA
HB-ZVRB [12]	5	5	1	1	unipolar	NO	28mA
proposed	6	3	3	1	unipolar	YES	About zero

VI. SIMULATION RESULTS

The simulation analysis of the 3-level grid-tied inverter is carried out utilizing Matlab/Simulink. The value of the capacitors C_1, C_2, and C_3 are equal to $220\mu F$, $560\mu F$, and $560\mu F$ respectively. Also, the value of the input power dc supply has been assumed 200V. The inductance of filter inductor is about 3mH. The inverter output voltage with peak value of 400V and sinusoidal injected current at unity (PF=1), leading and lagging power factors are depicted in Fig. 4(a), (b) and (c), respectively. So, it is validated that the provided system has the ability of tracking the reference current through the output filter. It is confirmed that proposed structure and its corresponding peak current control strategy could work together suitably. Using common grounding removes the leakage current. It can be seen that the voltage across of capacitors C_1, C_2, and C_3 have been adjusted to 200V, 400V,
and 400V, respectively. Also, the voltage ripple of the capacitors is within an acceptable range. The suggested grid-tied inverter also has the capability to control the reactive power. Therefore, under different conditions of power factor (PF) the injected current to grid and voltage of grid are indicated in Fig.6. It is shown that, the presented grid-tied inverter using the peak current control strategy can inject the sinusoidal waveform of current under different conditions of desirable PF. The grid voltage and injected current under the unity, leading and lagging power factors are depicted in Fig. 6 (a), (b) and (c), respectively. With respect to this figure, the value of injected power to the grid is equal to 0.77KW. In addition, the voltage stress on some of the utilized power switches (S_3~S_6) are presented in Fig. 7 (a)-(d). In this figure, the standing voltage of switch S_3 and S_4 are equal to $400V$ and standing voltage of switches S5 and S6 are about $800V$. Finally, with regard to obtained simulation results, the accurate performance of the suggested is confirmed.



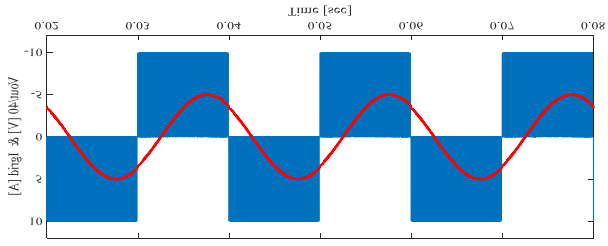


Fig. 4. Simulation results of inverter output voltage and the injected current to grid under different PFs (a) unity PF (b) leading PF (c) lagging PF.

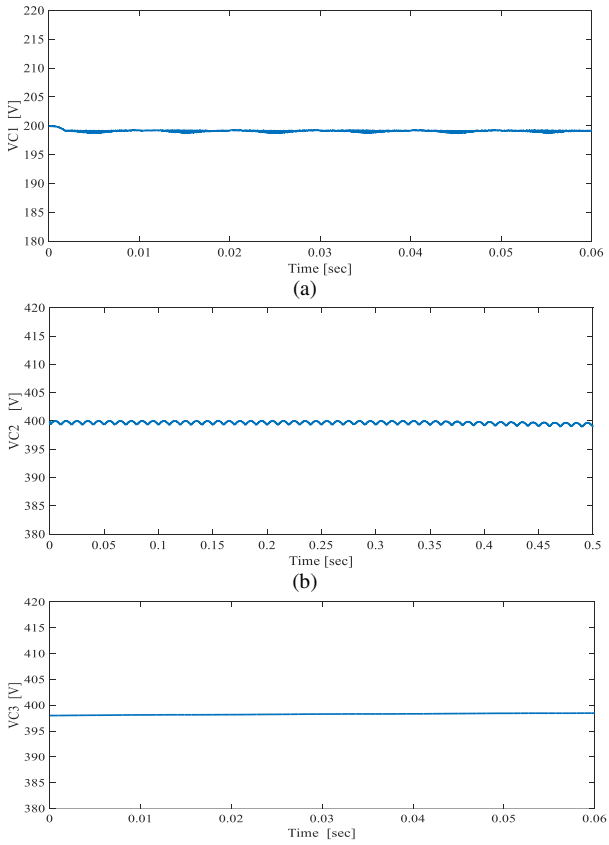
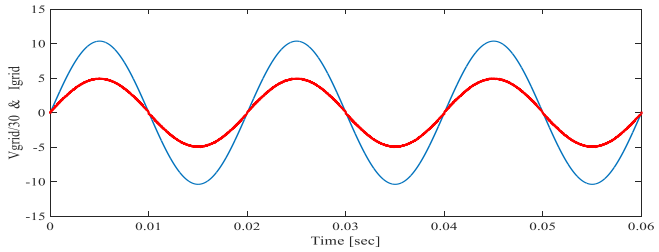


Fig. 5. Across voltage of capacitors (a) C_1 (b) C_2 (c) C_3.

VII. CONCLUSION

In this paper, a new single phase 3-level grid-tied inverter is proposed. The Suggested inverter proposes the voltage boosting and common grounded characteristics. In order to control the charging and discharging of the capacitors in the switched-capacitor module, series-parallel switching method has been applied. Also, the proposed topology can provide a boosting feature within a single stage process. In this paper, to inject current to grid with high quality and control the active power flow, the PCC method is applied. With respect to this method, a sinusoidal current can be injected to the power grid under different values of PFs. Since the negative polarity of the PV panel is connected directly to the null of ac power grid, the leakage current is eliminated completely.

Design considerations have also been included in this paper. The provided structure is compared with other conventional grid-connected inverters in the literature. Finally, to confirm the accurate operation of the inverter and the mathematical equations, simulation results based on Matlab/Simulink software are provided.



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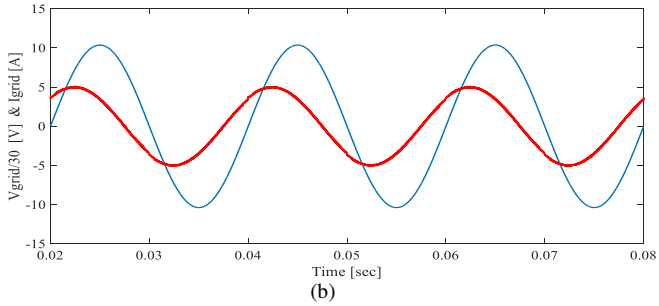

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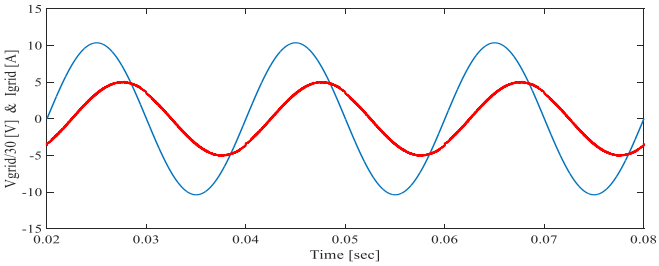
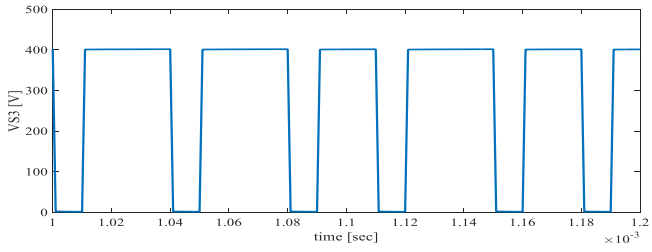
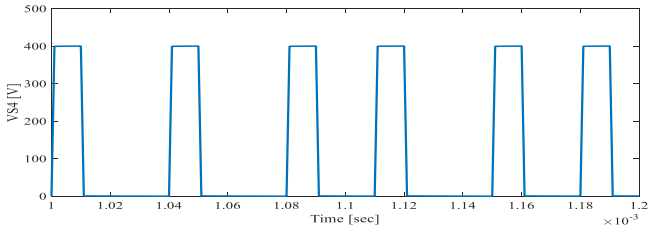


(c)

Fig. 6. The voltage and current of grid (a) unity PF (b) leading PF (c) lagging PF.



(a)



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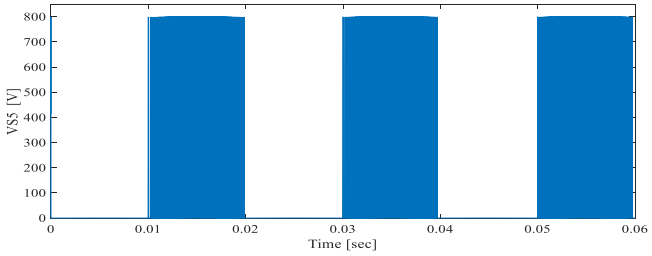

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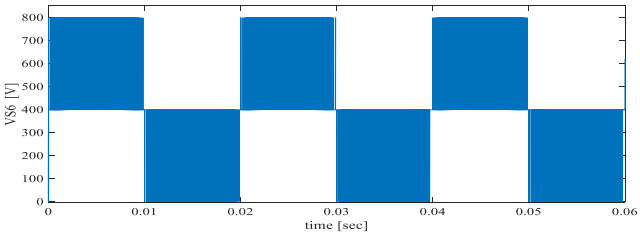

(d)

Fig. 7. The voltage waveform across the utilized power switches (a) V_{S3} (b) V_{S4} (c) V_{S5} (d) $V_{S6.}$

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