Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs and GaN HEMTs

Emre Gurpinar, *Student Member, IEEE,* Alberto Castellazzi

***Abstract*—In this paper, benchmark of Si IGBT, SiC MOSFET and GaN HEMT power switches at 600V class is conducted in single-phase T-type inverter. Gate driver requirements, switching performance, inverter efficiency performance, heat sink volume, output filter volume and dead-time effect for each technology is evaluated. Gate driver study shows that GaN has the lowest gate driver losses above 100kHz and below 100kHz, SiC has lowest gate losses. GaN has the best switching performance among three technologies that allows high efficiency at high frequency applications. GaN based inverter operated at 160kHz switching frequency with 97.3% efficiency at 2.5kW output power. Performance of three device technologies at different temperature, switching frequency and load conditions shows that heat sink volume of the converter can be reduced by 2.5 times by switching from Si to GaN solution at 60^{o}C case temperature, and for SiC and GaN, heat sink volume can be reduced by 2.36 and 4.92 times respectively by increasing heat sink temperature to 100^{o}C. Output filter volume can be reduced by 43% with 24W, 26W and 61W increase in device power loss for GaN, SiC and Si based converters respectively. WBG devices allow reduction of harmonic distortion at output current from 3.5% to 1.5% at 100kHz.**

***Index Terms*—Multilevel systems, Power conversion, Power electronics, Power MOSFETs, Insulated Gate Bipolar Transistors, Power Semiconductor Switches, Inverters.**

NOMENCLATURE

$\triangle I_{OUT}$	Output current ripple
$\triangle T$	Maximum temperature rise
$\triangle V_{(neg)}$	Negative bias voltage for GaN HEMT
A_p	Area-product
Att_{req}	Required attenuation
B_{max}	Maximum flux density
C_{DC}	DC link capacitance
C_f	Output filter capacitance
C_g	Gate-source capacitance
$C_{gs(ext)}$	External gate-source capacitance
C_{iss}	Input capacitance
CMR	Common mode rejection
C_{oss}	Output capacitance
C_{rss}	Reverse transfer capacitance
C_s	Series gate capacitance
D	Duty cycle
DC	Direct current
f_s	Switching frequency
GaN	Gallium nitride
$HEMT$	High-electron-mobility transistor
IC	Integrated circuit
$\widehat{I}$	Peak inductor current
I_{DS}	Drain-source current
I_g	Gate current
$IGBT$	Insulated-gate bipolar transistor
I_{OUT}	Inverter output current
$JFET$	Junction gate field-effect transistor
k_c	Capacitor volume constant
K_i	Current waveform factor
k_L	Inductor volume constant
k_u	Window utilisation factor
L_f	Output filter inductance
$MOSFET$	Metaloxide semiconductor field-effect transistor
NPC	Neutral point clamped
P_{GaN}, P_{SiC}, P_{Si}	Device power loss
P_g	Gate driver loss
P_{Diss}	Maximum power dissipation
P_{MAX}	Maximum output power
P_y	Total semiconductor loss
PWM	Pulse width modulation
Q_{C_g}	Charge across Cg
Q_{C_s}	Charge across Cs
Q_g	Gate charge
r_{ch}	Case-to-heat sink thermal resistance
R_{DS-on}	Drain-source on-state resistance
R_{gate}	External gate resistance
$R_{gate(turn-off)}$	Turn-off gate resistance
$R_{gate(turn-on)}$	Turn-on gate resistance
r_{h-r}	Required heat sink thermal resistance
r_{jc}	Junction-to-case sink thermal resistance
SBD	Schottky barrier diode
Si	Silicon
SiC	Silicon carbide
SJ	Super junction
T_a	Ambient temperature
T_h	Heat sink temperature
THD	Total harmonic distortion
T_j	Junction temperature
Vol	Volume
V_{CE-sat}	Collector-emitter saturation voltage
V_{DC}	DC link voltage
V_{DS}	Drain-source blocking voltage
V_g	Rail-to-rail gate driver voltage

E. Gurpinar and A. Castellazzi are with the Power Electronics, Machines and Control (PEMC) research group, Tower Building, University of Nottingham, University Park, Nottingham, NG7 2RD, UK. Email: emre.gurpinar@nottingham.ac.uk; alberto.castellazzi@nottingham.ac.uk

V_{gs}	Gate-source voltage
V_{nom}	Nominal voltage of capacitor
V_{OUT}	Inverter output voltage
V_{th}	Minimum gate threshold voltage
WBG	Wide-bandgap

I. Introduction

DELIVERY of generated power from energy sources to end user with maximum efficiency is crucial for electricity generation sources and utilities for maximum utilization of the source and minimisation of the payback time for initial system cost. Power electronic converters are the key elements of the energy systems for integration of the source to electrical grid and delivery of the generated power to end user. Efficiency of the power electronic converter has a significant impact on the system efficiency and has to be kept at maximum due to the reasons mentioned above.

The literature review clearly shows that SiC and GaN devices are promising advancements in power semiconductor technology that can enable very high efficiencies and very high power density by increased switching frequencies [1]. In this paper, performance analysis of three different device technologies (SiC, GaN and Si) at 600V blocking voltage range is discussed based on a three level single phase inverter. There are limited SiC and GaN power devices at 600V blocking voltage range and the performance analysis of these devices against state of the art Si IGBTs provides insight into wide-bandgap device potential and limits for high efficient power converters.

Application of SiC devices in renewable energy converters has been widely discussed in literature and papers show the potential of achieving very high efficiency figures with SiC devices for photovoltaic applications specifically. Performance of SiC JFET devices for PV applications is discussed in detail in [2]–[4]. In [2], designed converter achieved 98.8% peak efficiency and in [3], HERIC converter with SiC devices achieved 99% peak efficiency. According to [4], overall losses in a PV inverter can be halved by just replacing Si IGBTs with SiC JFETs. The performance of 650V SiC MOSFETs is also evaluated for H6 topology in [5]. The results show that replacing Si IGBT with SiC MOSFETs can bring up to 1% efficiency gain for same switching frequency. In addition to these, synchronous rectification capability of SiC MOSFETs is utilized for 3-level ANPC inverter in [6] and the inverter is successfully operated with grid connection up to 80kHz. Performance evaluation of 1200V and 650V SiC MOSFETs and comparison with Si IGBTs is discussed in [7]. The evaluation proves the performance stability of SiC MOSFETs under different ambient temperatures and all SiC inverter achieves 98.3% peak efficiency at 16kHz switching frequency.

Normally-off GaN HEMTs have been introduced by Panasonic at 600V. In [8], GaN HEMTs are implemented in a DC/DC converter for maximum power point tracking for PV applications and converter operated with 98.59% peak efficiency at 48kHz switching frequency. Same devices have been used in different applications such as resonant LLC DC/DC converter, three phase inverter and synchronous buck converter that show the high switching and conduction performance of the devices in different operating conditions [9]–[11]. In [9], GaN devices are operated at 1MHz switching frequency in LLC resonant converter and achieved 96.4% efficiency at 1kW output power. In [10], GaN devices are used at low frequency three phase inverter and the inverter achieved 99.3% efficiency at 900W output power and 16kHz switching frequency. Normally-on GaN HEMTs at 600V voltage class with and without cascode structure are discussed in [12] and [13] for hard-switching topologies. Performance improvement in a synchronous buck topology is presented in [12] and it is shown that smaller reverse recovery charge and output capacitance of GaN HEMT lead to reduction in turn-on losses and up to 2% efficiency improvement in comparison to Si MOSFET. The current collapse phenomena for 600V normally-on GaN HEMT is presented in [13] and although the device is statically rated at 600V, the experimental results are presented up to 50-60V due to increase in on-state voltage drop during dynamic testing.

GaN HEMT power devices have been presented in the literature for different topologies but this is the first time 600V GaN devices are implemented as bi-directional switch in a multilevel inverter. The converter is operated at different switching frequencies, different ambient temperatures and different load conditions in order to fully evaluate performance of Si, SiC and GaN device technologies. In view of the above considerations, grid connected power converters are one of the most interesting applications for high performance power semiconductors such as SiC and GaN.

In the section II, T-type inverter and selected PWM modulation is explained. In section III, device characteristics of Si IGBT, SiC MOSFET and GaN HEMT from manufacturer datasheets are presented and discussed. Gate driver requirement for each technology is discussed and gate drive loss analysis is presented in section III-A. In section V, experimental results from the converter with different devices are presented. In section VI, the impact of wide-bandgap devices in reduction of volume of passive components and cooling requirements is presented to show the potential of wide-bandgap technology in next generation power converters. In the final section VI-C, effect of dead-time to output current harmonics with high frequency inverters and wide-bandgap devices are discussed.

II. T-Type Inverter

T-Type inverter, also known as Neutral Point Piloted inverter, is a member of neutral-point-clamped inverter topologies with three output voltage levels [14]. It is one of the interesting topologies for single-phase three-level inverter systems and is used in commercial products [15]. The schematic of the converter and switching strategy signals are presented in Fig. 1a and 1b respectively. Switches that are forming the half bridge S_1 and S_4 are rated at V_{DC} and bi-directional

switch S_2 and S_3 are rated at $V_{DC}/2$. Control and implementation of T-type converter in various applications such as renewable converters and fault-tolerant systems are discussed in literature [16]–[21]. The switching strategy for this topology is published in [22]. The commutation of output current takes place between S_1 and S_2 in the positive half and between S_3 and S_4 in the negative half wave. S_3 is completely on during positive half and S_2 is completely on during negative half of the output current in order to utilize the reverse conduction capability of MOSFETs and HEMTs. The anti-parallel diode across each device is optional for SiC MOSFET and GaN HEMTs due to intrinsic body diode and bidirectional current capability of SiC MOSFETs; and due to bidirectional current capability and freewheeling capability of GaN HEMTs. For Si IGBT, high performance anti-parallel diode has to be used in order to minimize additional turn-on losses caused by reverse recovery charge of anti-parallel diode [23]. The dead-time between S_1, S_2 and S_3, S_4 switches should be as small as possible for SiC and GaN devices in order to minimize the conduction losses across bi-directional switch. Reverse conduction performance of S_2 and S_3 is crucial in comparison to S_1 and S_4 with unity power factor operation and has a significant impact on overall conduction losses. With unity power factor operation, the current flow through S_1 and S_4 will be always from drain to source terminals; therefore body diode of the devices will not conduct under nominal operation. On the other hand, one of the devices in bi-directional will be in reverse conduction mode at any zero-state switching instant. Furthermore, minimization of dead-time for all device technologies will reduce output current harmonic distortion that will be discussed in final section of the paper. In this setup, 1200V SiC MOSFETs for S_1 and S_4 switches are used without anti-parallel diodes. Si IGBT, SiC MOSFET and GaN HEMT are tested in S_2 and S_3 switches. For Si IGBT, 600V SiC diodes are used as anti-parallel diodes due to necessity of reverse current conduction and high efficiency.

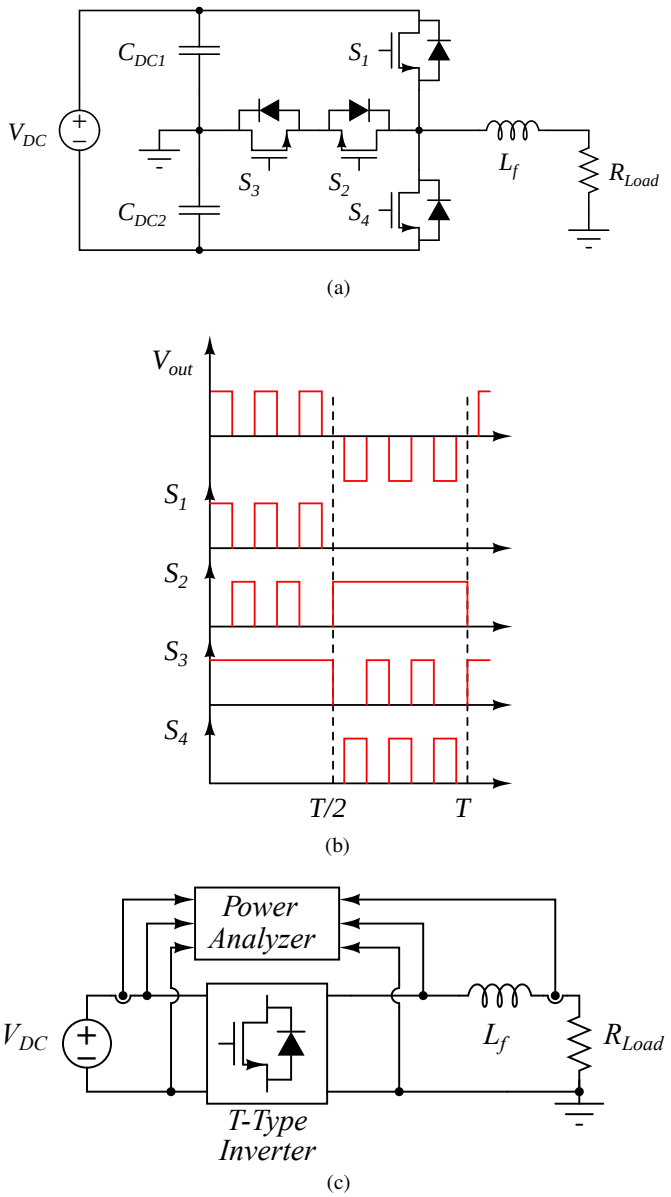


Fig. 1. (a) T-type inverter topology , (b) switching pattern and (c) test setup.

III. 600V Si IGBT, 650V SiC MOSFET and 600V GaN HEMT Devices

In this paper, three different power device technologies for single-phase power converters are investigated: Si IGBT, SiC MOSFET and GaN HEMT. Super-junction MOSFETs at 600V class can also be counted as alternative device type due to good on-state performance. However, non-linear behaviour of output capacitance of super-junction devices places large transient load on the complementary switch and extensive reverse recovery charge increases turn-on losses in hard-switching topologies [24], [25]. Parallel connection of SiC Schottky diode to SJ MOSFET does not solve reverse recovery problem as the on-state voltage drop of SJ-MOSFET body diode is lower than SiC Schottky diode [26]. Different half-bridge topologies, gate driver and auxiliary circuit concepts have been introduced in literature that mitigate the problems associated with output capacitance and reverse recovery charge but it should be noted that the proposed concepts increase complexity and design of the converter [24], [26]. In literature, reliability, control methods and applications of 1200V SiC MOSFETs and JFETs have been discussed [27]–[34] but there is limited information for wide-bandgap devices at 600V blocking voltage range as 650V SiC MOSFET and 600V GaN HEMT became available in the last years.

Main device parameters of tested Si IGBT, SiC MOSFET and GaN HEMT are listed in Table I. In order to simplify the comparison, drain and source terms used for HEMT and SiC can be replaced with collector and emitter for Si IGBT. The SiC MOSFET that is used in this paper is commercially available and GaN HEMT is available as samples at the time of publication. Comparison table shows that GaN HEMT has smallest continuous current capability at 25^{o}C with 15A. The current capability of GaN HEMT is related to maximum power dissipation capability of the package at 25^{o}C, which is half of SiC MOSFET and Si IGBT due to insulated tab. In terms of

conduction performance, GaN HEMT and SiC MOSFET do not have offset voltage during turn-on like Si IGBT and the on-state resistance of GaN-HEMT is approximately half of SiC MOSFET at room temperature. On the other hand, Drain current at 100^{o}C case temperature is 20A for SiC MOSFET and Si IGBT, and 11A for GaN HEMT. It is clear that Si IGBT has to be de-rated significantly in order to operate at high ambient temperatures. At 150^{o}C, the voltage drop of across GaN HEMT, SiC MOSFET and Si IGBT is 3V, 3.5V and 2.2V respectively. On-state voltage drops at different case temperatures show that Si IGBT has the best conduction performance at high case temperature values and GaN HEMT has the best conduction performance at ambient temperature. The device datasheets show that SiC and GaN devices have very stable switching loss performance over different junction temperatures unlike Si IGBT. This property makes wide-bandgap devices interesting at high switching frequencies with high case temperatures. Regarding gate requirements, it is clear that GaN HEMT has the minimum gate drive requirement among these three devices due to smallest gate charge. Gate driver requirements will be discussed in the next topic in detail. The output capacitances are similar for all three devices and the reverse transfer capacitance of GaN HEMT is approximately 8 times and 20 times smaller than SiC MOSFET and Si IGBT respectively.

TABLE I
GAN HEMT, SIC MOSFET AND SI IGBT DEVICE PARAMETERS

	Panasonic GaN HEMT PGA26A10DS	ROHM SiC MOSFET SCT2120AF	Infineon Si IGBT IGP20N60H3
V_{ds}	600V	650V	600V
I_{ds} (25^{o}C)	15A	29A	40A
I_{ds} (100^{o}C)	11A	20A	20A
R_{DS-on} (25^{o}C)	65mΩ @8A	120mΩ @10A	N/A
V_{CE-sat} (25^{o}C)	N/A	N/A	1.95V
C_{iss}	300pF @500V	1200pF @500V	1100pF @25V
C_{oss}	90pF @500V	90pF @500V	70pF @25V
C_{rss}	1.5pF @500V	13pF @500V	32pF @25V
Q_g	12nC @3.2V	61nC @18V	120nC @15V
V_{th}	0.8V	1.6V	4.1V
V_{gs}	-10 to 4.5V	-6 to 22V	±20V
T_j	150^{o}C	175^{o}C	175^{o}C
P_{Diss} (25^{o}C)	83W	165W	170W
r_{jc}	1.5^{o}C/W	0.7^{o}C/W	0.88^{o}C/W
Device Package	TO-220D-A1	TO-220AB	TO-220-3

A. Gate Driver Requirements

The devices presented in the previous section require different gate-source voltages for turn-on and turn-off and have different dynamic characteristics; therefore bespoke gate-drivers have to be designed for each device. The schematics and gate waveforms for each device are presented in Fig 2. The gate driver loss P_g for SiC MOSFET and Si IGBT can be calculated as:

$$P_g = V_g Q_g f_s \tag{1}$$

Where V_g is rail-to-rail gate driver voltage, Q_g is cumulative gate charge and f_s is switching frequency. SiC MOSFET and Si IGBT are easy to drive in terms of gate configuration but both devices are generally operated with positive and negative voltage for safety reasons and faster switching. SiC MOSFET requires around +19V to +21V for fast turn-on and minimum conduction loss; and -3V to -5V for better noise immunity during turn-off. On the other hand, Si IGBT is driven with symmetrical voltage such as ±15V or ±18V for similar reasons with SiC MOSFET. For these two devices, two isolated power supplies or isolated power supply with two outputs are required. The turn-on and turn-off paths for these devices can be separated with $R_{gate(turn-off)}$, optional external gate-emitter capacitance $C_{gs(ext)}$ can be included as it can be seen in Fig. 2c, in order to achieve optimum switching speed and avoid false turn-on due to reverse transfer capacitance [35].

GaN HEMT requires continuous gate current during conduction therefore the gate driver losses can be calculated as follow:

$$P_g = V_g(Q_{C_s} + Q_{C_g})f_s + R_{gate}{I_g}^2 D \tag{2}$$

Where C_s is series connected capacitor in GaN gate driver, C_g is total gate capacitance including reverse transfer capacitance, R_{gate} is the gate resistor that provides continuous gate current I_g and D is duty cycle in a switching period. Series connected capacitance C_s provides inrush current during switching and also negative voltage during turn-off in order to prevent false turn-on due to low threshold voltage of GaN HEMT. The accumulated charge across C_s should be larger than Q_{C_g} in order to reach required voltage level across GaN HEMT during turn-on and the capacitance value of C_s will determine the turn-off negative voltage. R_{gate} resistor is defined by continuous gate current, which is 20mA at 3.2V gate-source voltage, and supply voltage. $R_{gate(turn-on)}$ is determined according to maximum gate driver current, supply voltage and recommended limits (300mA in this case).

In GaN HEMT gate driver, R_{gate} is selected as 470Ω in order to limit continuous gate current to 18.7mA with 12V rail-to-rail gate driver voltage and 3.2V gate-source voltage. For determining $R_{gate(turn-on)}$ and C_s values, at first, $R_{gate(turn-on)}$ is selected as 47Ω in order to provide 300mA gate charging current along with R_{gate}. Then, the series capacitor C_s is selected as 2.82nF according to following equation in order to provide -4.5V ($\triangle V_{(neg)}$) during turn-off for safe operation and speed up turn-on transient:

$$C_s = \frac{Q_g}{V_g - V_{gs} - \triangle V_{(neg)}} \tag{3}$$

By using datasheet values, the gate drive loss for each device at different switching frequencies can be calculated.

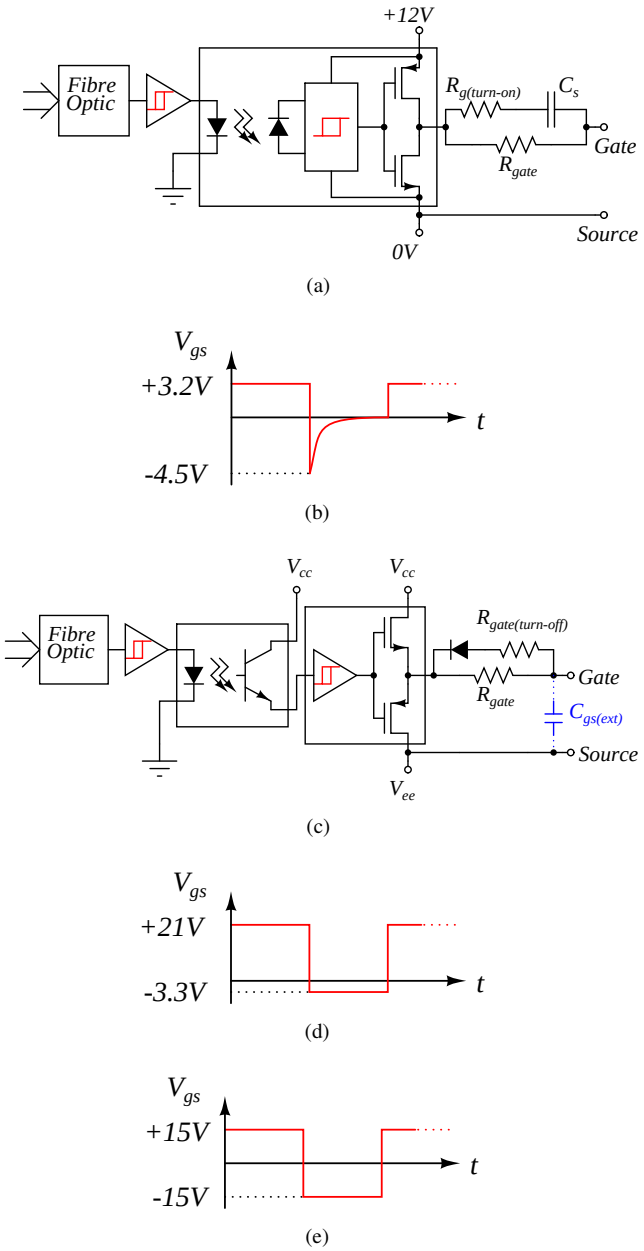


Fig. 2. Gate driver schematics and waveforms: (a) GaN HEMT gate driver, (b) GaN HEMT gate waveform, (c) SiC MOSFET and Si IGBT gate driver, (d) SiC MOSFET gate waveform, (e) Si IGBT gate waveform.

The comparison of gate drive loss with respect to switching frequency is presented in Fig 3. For GaN HEMT, the duty cycle is taken as 0.64 and the gate-source (emitter) voltage, gate charge for all devices are taken as shown in Table I. The comparison in Fig. 3 shows that GaN has minimum gate loss above 100kHz and has clear advantage in high switching frequencies in comparison to both SiC MOSFET and Si IGBT. Results show that the on-state loss of GaN HEMT is clearly dominating switching losses below 100kHz.

The gate current requirement and noise immunity are important factors for selection of gate driver IC and therefore size of the IC package. High speed switching for SiC MOSFET and Si IGBT requires small gate resistance and therefore

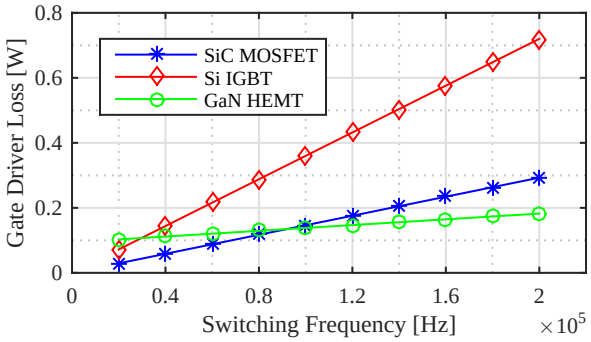


Fig. 3. Gate loss comparison of single Si IGBT, SiC MOSFET and GaN HEMT.

high peak current. Two different gate drive ICs are presented in Fig. 2a and 2c. Gate drive optocoupler (ACPL-P346) in Fig. 2a provides isolation with 70kV/s common-mode noise rejection and totem pole arrangement in the same package but the continuous peak current capability is limited to 3A. The main advantage of this IC is the isolation with single package, minimum external component requirement and small footprint in the printed circuit board. On the other hand, limited current capability means it is not suitable for high speed switching devices with large gate charge. For SiC MOSFET and Si IGBT, in Fig. 2c, a gate drive interface optocoupler with high CMR has to be used for signal isolation and a high current non-isolated gate driver IC is used for driving the power switch. In this configuration, ACPL-4800 interface IC with 30kV/s CMR is used for signal isolation and IXDN609SI with 9A current capability is used for gate drive circuit. Although this configuration provides higher peak current with commercial ICs, the footprint of gate driver circuit increases significantly and component count on the board also increases in comparison to the option in Fig. 2a. Moreover, isolated gate drive supply for both configurations is provided by isolated DC/DC converters with minimum 1kV isolation rating and low isolation capacitance (e.g. IH0512S-H for +12V supply) in order to minimize common-mode current circulation. The complexity of gate driver is an important factor, which significantly impacts both manufacturing and testing, especially in large volume applications, from a cost point of view.

IV. Test Setup

The converter parameters are listed in Table II and a schematic of the test setup is shown in Fig. 1c. Converter parameters are based on single phase grid connected inverters. PPA 5530 precision power analyzer from N4L is used to measure voltage, current and power factor at the input and output of the converter and overall efficiency. The voltage at the output is measured before the filter inductor L_f in order to exclude winding and core losses of output filter inductors from performance analysis. The accuracy of the analyser reduces with respect to signal frequency and is around 2% at 200kHz. Therefore the measurements as carried

out inevitably characterized by some degree of inaccuracy, but as the inaccuracy is the same for all type of devices, it is expected that the error should always be in the same direction and should not affect the comparative analysis.

Two heating resistors are mounted to the heat sink with equal distance to power devices and a cooling fan is placed directly at the cooling fins of heat sin for control of case temperature of devices. The resistors generate additional heat at light load and cooling fan cools down power devices at heavy load conditions. By properly setting the required amount of heat generation including device losses and heat removal, the heat sink temperature can be controlled independently from converter operation point. For each load and switching frequency condition, the heat sink temperature is independently set between 50^{o}C and 80^{o}C in order to evaluate the performance of the devices under different load, frequency and temperature conditions. By this arrangement, temperature of the heat sink can be made independent from load and switching frequency.

Gate driver board and power cell are shown in Fig. 4a and 4b respectively. High frequency film capacitors are placed closed to switches in parallel with electrolytic capacitors in order to provide minimum voltage overshoot across devices and output inductor L_f is formed by two off the shelf 500μH inductors connected in series and mounted on power plane PCB. The gate driver is designed according to requirements in the previous section to provide high switching speed performance for SiC, Si and GaN devices. The board is directly soldered on the device pins in order to minimize the gate loop stray inductance and the gate signals are provided through a fiber optic link by FPGA board that can provide high frequency sinusoidal PWM modulation.

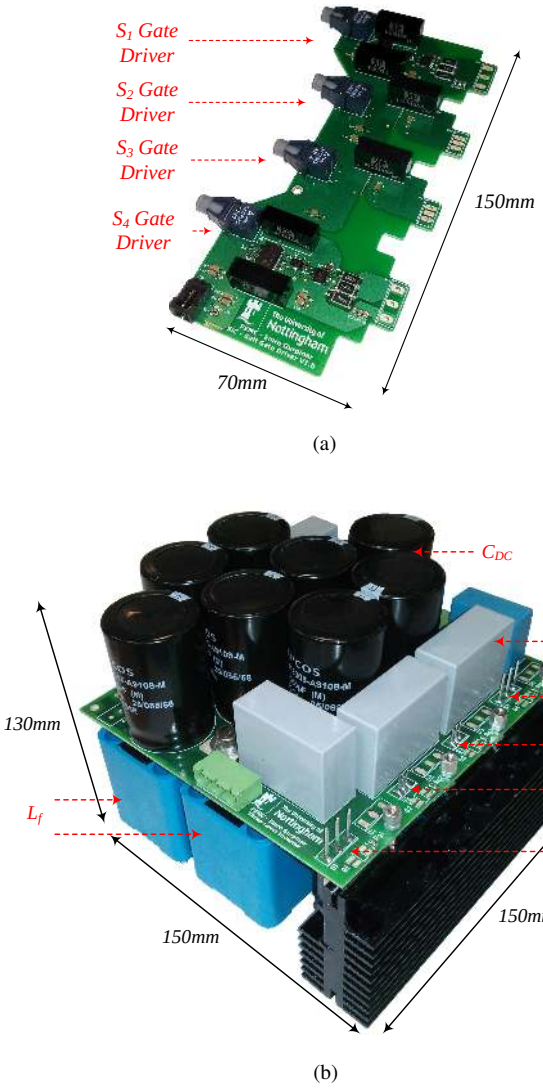


Fig. 4. Single phase T-type inverter: (a) gate driver and (b) power cell.

TABLE II
CONVERTER PARAMETERS AND TEST CONDITIONS

Parameter	Value
P_{MAX}	3.5kW
V_{DC}	700V
V_{OUT}	230V
L_f	1mH
C_{DC}	4mF
f_s	16 to 160kHz
$Dead-time$	400ns
S_1, S_4	CREE CMF2120D
S_2, S_3	Panasonic PGA26A10DS ROHM SCT2120AF Infineon IGP20N60H3
600V SiC Diode	CREE C3D20060
T_h	50 to 80^{o}C

V. EXPERIMENTAL RESULTS

A. Switching Performance

The switching performance of 1200V SiC MOSFET, 650V SiC MOSFET and 600V GaN HEMT is presented in this section. Si IGBT is a well-established technology at 600V and 1200V blocking voltage range and the switching performance already exists in literature [36], [37]. Turn-off and turn-on switching transitions at 3kW output power are presented for 1200V SiC MOSFET, 650V SiC MOSFET and 600V GaN HEMT in Fig. 5 and 6 respectively. Due to commutation scheme of T-type inverter in [22], at unity power factor, S_1 achieves soft turn-off when output voltage changes from +V$_{DC}$/2 to 0 while S_2 switch starts reverse conduction with body diode for SiC MOSFET, antiparallel diode for Si IGBT and freewheeling mode with GaN HEMT. When the output voltage changes from 0 to +V$_{DC}$/2, S_2 achieves hard turn-off. The drain-source currents for all devices are measured at the source pin of the devices; therefore include the gate-source current. In Fig. 5b, one important thing to note is 24A current overshoot in I_{DS} at turn-on due to high dV/dt, which

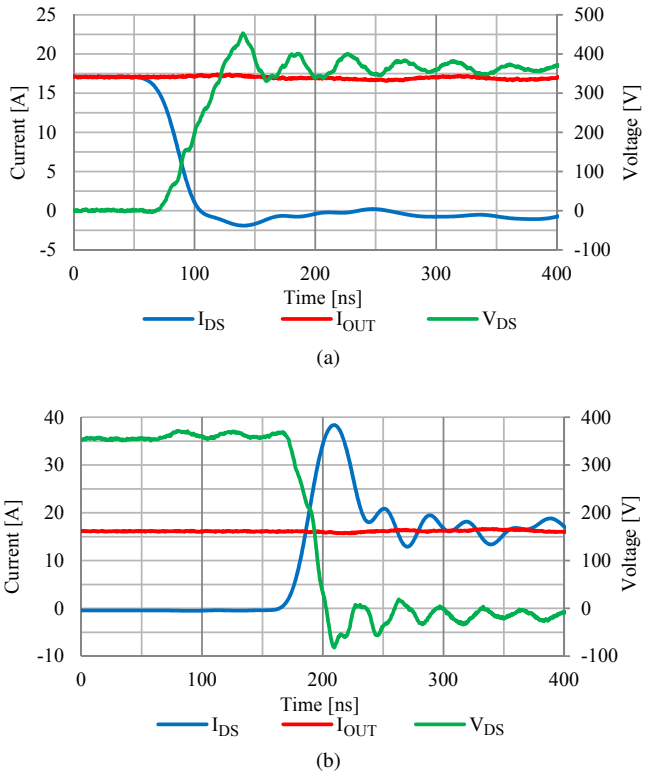


Fig. 5. 1200V SiC MOSFET: (a) turn-off and (b) turn-on performance in T-type inverter.

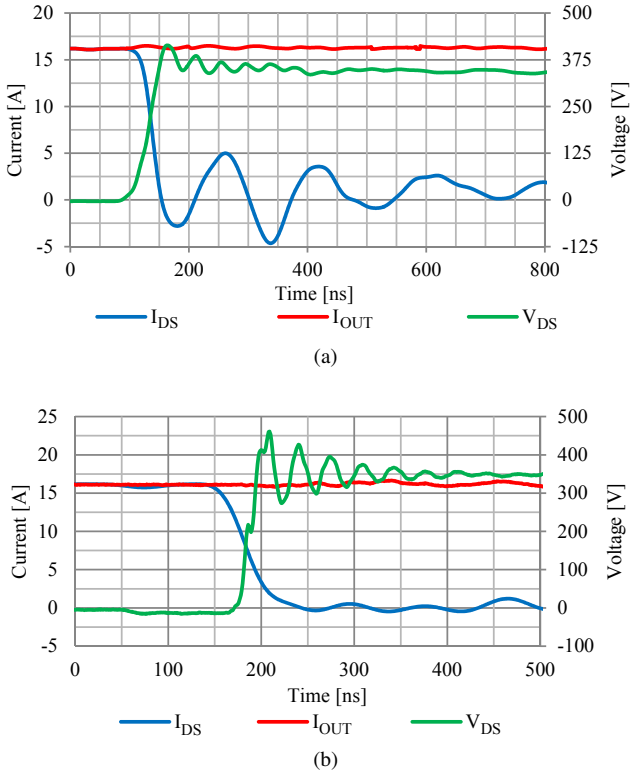


Fig. 6. Turn-off waveforms for: (a) 650V SiC MOSFET, (b) 600V GaN HEMT.

is 12V/ns at device turn-on, and 1.9nF input capacitance. This current overshoot remained constant at different load conditions with same drain-source voltage and one of the reasons is the gate-source current for turn-on of the device and the second reason is the charging current of device output and reverse capacitance. The external and internal gate resistors of SiC MOSFET are 3.3Ω and 4.6Ω respectively and peak gate-source during turn-on is 3A with 24V voltage change at gate-source. The output and reverse capacitance of SiC MOSFET is voltage dependent and increases with decrease drain-source voltage due to decrease of depletion region.

The theoretical conduction loss analysis of T-type inverter has been discussed thoroughly in [38] and equations can be found in the appendix. The theoretical conduction loss can be calculated with respect to experimental conditions (e.g. temperature, modulation index, output power) in order to extract switching losses from experimental efficiency results. Therefore switching and conduction performance of Si, SiC and GaN can be compared at different switching frequency and heat sink temperature cases. The converter total, theoretical conduction and switching loss comparisons at 2.5kW output power, different heat sink temperatures, and 32kHz switching frequency for Si, SiC and GaN based configurations are presented in Fig. 7. Switching losses dominate the total losses for SiC and Si based configurations. On the other hand, GaN based configuration shows significant reduction in total loss due to high switching performance of GaN devices at different heat sink temperature values.

B. Efficiency Performance

The power cell efficiency with three different semiconductor technologies is presented in this section. The efficiency analysis at 16kHz and 32kHz at 50^{o}C heat sink temperature is presented in Fig. 8 for Si IGBT, SiC MOSFET and GaN HEMT. It is clear that by just replacing Si IGBT with GaN HEMT or SiC MOSFET, significant improvements in efficiency can be achieved due to superior switching properties of wide-bandgap devices. The performance difference between silicon and wide-bandgap devices becomes clearer at 32kHz. The converter achieved peak efficiency 99.2% with GaN HEMTs at 16kHz switching frequency and 50^{o}C heat sink temperature. At 16kHz, SiC MOSFET and GaN HEMT brings up to 0.6% and 1.45% efficiency improvement respectively and at 32kHz, these values increase to 0.75% and 1.6% due to poor switching performance of Si IGBT in comparison to wide-bandgap technologies.

The performance of the devices at different switching frequencies and heat sink temperatures are presented in Fig. 9a and 9b. Fig 9a shows the comparison of SiC and GaN solutions up to 64kHz switching frequency and between 60^{o}C and 80^{o}C heatsink temperatures at 2.5kW output power. The results show that GaN solution proves a robust performance under different temperature conditions and complete SiC solution has less than 0.5% efficiency variation at 64kHz switching frequency. Fig. 9b shows a similar efficiency comparison versus heatsink temperature at 16kHz and 32kHz switching frequencies at 2.5kW output power for

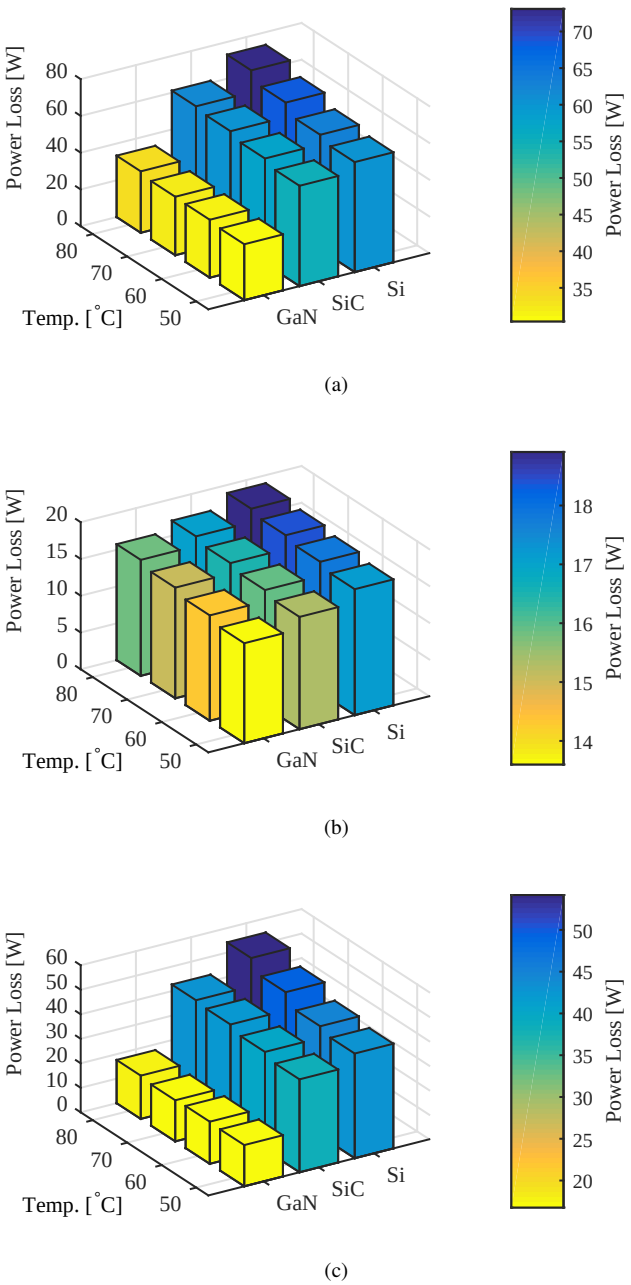


Fig. 7. Loss breakdown for GaN, SiC and Si based converter at 2.5kW output, 32kHz switching frequency: (a) total power device loss, (b) conduction loss, (c) switching loss.

three different device technologies. It is clear that SiC and GaN device show good performance under different ambient temperatures due to wide-bandgap device properties [1].

Finally, due to best performance among all three devices, inverter based on GaN is tested up to 160kHz at various load conditions in order to evaluate switching performance of the inverter. The results are presented in Fig. 10. The efficiency results show that SiC and GaN based T-type inverter can perform with high efficiency up to 3kW output power and up to 160kHz switching frequency. The efficiency remains above 97% above 2.2kW output power.

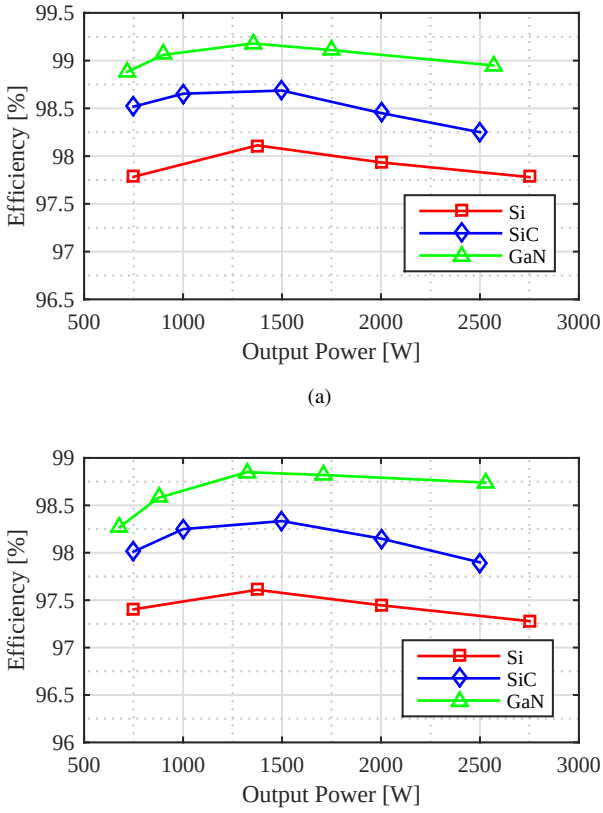


Fig. 8. Efficiency comparison at: (a) 16kHz and (b) 32kHz switching frequencies at 50C heatsink temperature.

VI. Impact on Converter Volume

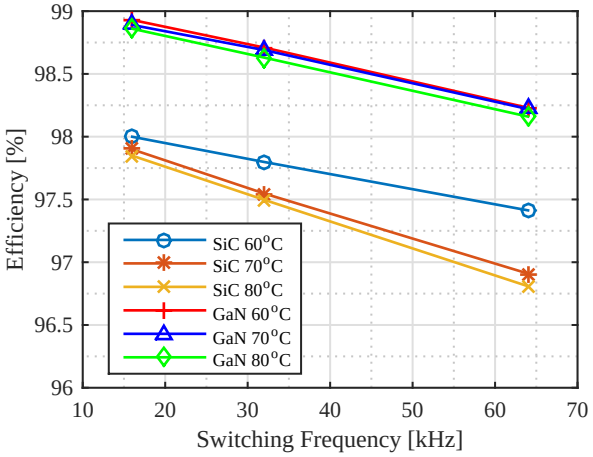
The overall efficiency analysis under various output power, switching frequency and heat sink temperature conditions show that wide-bandgap devices can be used to design inverters at high frequency, high heat sink temperature in order to reduce heat sink volume and output inductor volume without compromising the efficiency. In this section, the impact of high performance of wide-bandgap devices on heat sink volume and output filter volume will be investigated and compared to Si IGBT. The impact analysis is based on following assumptions:

- Cooling system is based on natural air convection.
- Single stage LC output filter is used.
- Converter output power is rated at 2500W.
- Switching frequency of the converter is selected as 32kHz.

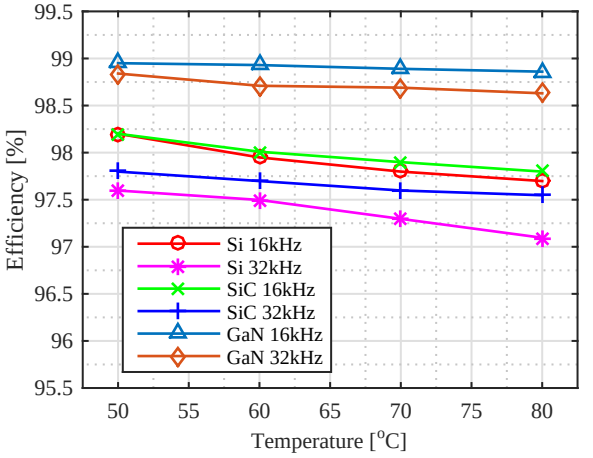
A. Heat Sink Design

The heat sink volume analysis is based on interpolation of power losses of three different device choices at maximum output power and between 60^oC and 100^oC heat sink temperatures. The power losses based on extrapolation of experimental results based on Fig 7 and 8. The power loss curves based on experimental data for each device technology are presented in Fig. 11.

Based on Fig. 11 and 9, the efficiency of power cell as a function of heat sink temperature and switching frequency



(a)



(b)

Fig. 9. Efficiency vs switching frequency comparison at different heatsink temperatures for (a) SiC and GaN , and (b) efficiency vs temperature comparison for SiC, GaN and Si at 16kHz and 32kHz switching frequencies.

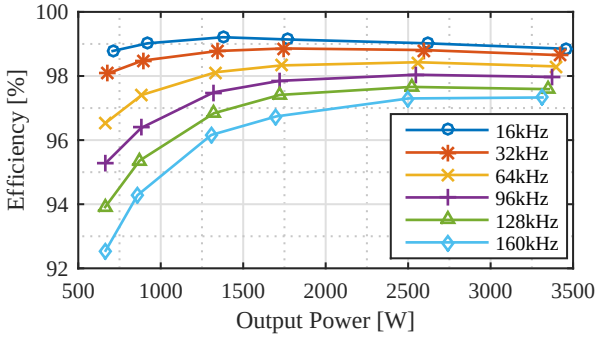


Fig. 10. Efficiency versus output power of SiC + GaN inverter at 50^{o}C heatsink temperature and between 16 and 160kHz switching frequencies.

based on Si IGBT, SiC MOSFET and GaN HEMT can be expressed as follow:

$$\eta_{Si} = k_{t_{Si}}\left(-2.82\times10^{-5}f_s + 98.4\right) \tag{4}$$

$$k_{t_{Si}} = -3\times10^{-4}T_h + 1.0151 \tag{5}$$

$$\eta_{SiC} = k_{t_{SiC}}\left(-1.22\times10^{-5}f_s + 98.192\right) \tag{6}$$

$$k_{t_{SiC}} = -9\times10^{-5}T_h + 1.0043 \tag{7}$$

$$\eta_{GaN} = k_{t_{GaN}}\left(-1.154\times10^{-5}f_s + 99.08\right) \tag{8}$$

$$k_{t_{GaN}} = -4\times10^{-5}T_h + 1.0018 \tag{9}$$

Where η is efficiency, T_h is heat sink temperature and f_s is switching frequency. Equation 4, 6 and 8 are used to calculate device power loss at specific heat sink temperature and switching frequency and the calculated power loss is for calculation of required heat sink thermal resistance r_{h-r}. The thermal network for devices in T-type inverter is presented in Fig. 12. T_j is junction temperature, r_{jc} is junction to case thermal resistance, r_{ch} is case to heat sink thermal resistance, T_c is ambient temperature and T_a is ambient temperature.

The junction temperature for SiC and GaN devices and required heat sink thermal resistance can be calculated as follow:

$$S_{1,4} : T_{j_{SiC}} = P_{SiC}\frac{r_{jc_{SiC}} + r_{ch_{SiC}}}{2} + T_h \tag{10}$$

$$S_{2,3} : T_{j_{S_{2,3}}} = P_{S2,3}\frac{r_{jc_{S_{2,3}}} + r_{ch_{S_{2,3}}}}{2} + T_h \tag{11}$$

$$r_{h-r} = \frac{T_h - T_a}{P_t} \tag{12}$$

Where P_{SiC} is total loss of SiC MOSFET, $P_{S2,3}$ is total loss of S_2 or S_3 switch and Pt is total semiconductor loss. Calculated r_{h-r} then can be used to calculate volume of heat sink based on natural air convection. The volume of various extruded naturally cooled heat sinks against heat sink thermal resistance are presented in Fig. 13 [39]. Based on the results, curve fitting is applied to minimum heat sink volume available at given r_{h-r} value and presented in 13.By using r_{h-r} from 12 in 13, volume of extruded naturally cooled heat sink can be calculated for different device case temperature, ambient temperature and power loss.

$$Vol_{heatsink} = 3263e^{-13.09r_{h-r}} + 1756e^{-1.698r_{h-r}} \tag{13}$$

Heat sink volume calculations based on 10-13 for three different device technologies with respect to heat sink temperature are presented in Fig. 14. The ambient temperature is chosen as room temperature 25^{o}C and case-to-heat sink thermal resistance is 0.57^{o}C/W and taken from a commercial silicon based insulation pad with 4kV insulation breakdown voltage. The results in Fig. 14 show that Si based converter has 2.5 times and SiC based converter has 2.1 times higher heat sink volume in comparison to GaN based converter at 60^{o}C case temperature. In addition to this, the volume of heat sink

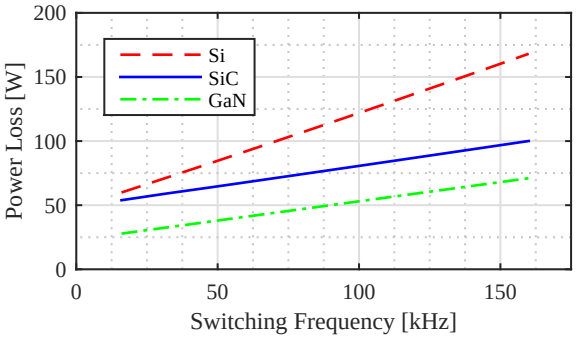


Fig. 11. Power cell loss comparison with different device technologies at 2500W output power at 60^{o}C heatsink temperature.

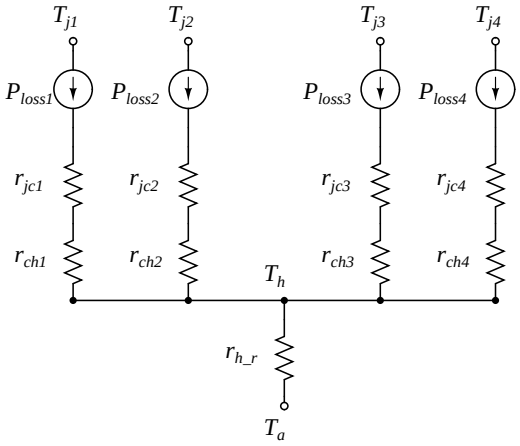


Fig. 12. Thermal network for T-type inverter.

can be reduced by factor of 4.92 and 2.36 for GaN and SiC based converters respectively by increasing case temperature from 60 to 100^{o}C. The penalty for increased case temperature for GaN and SiC solution will be 12% and 16% increase in device losses. On the other hand, heat sink volume of Si based inverter can be reduced by factor of 1.4 with 44% increase in device losses.

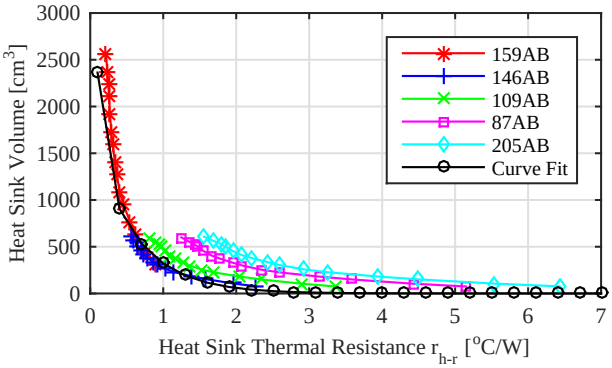


Fig. 13. Commercial naturally cooled heat sink volumes [39].

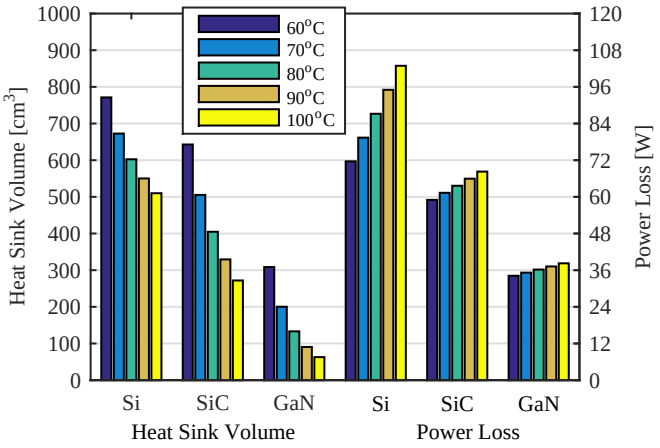


Fig. 14. Heatsink volume versus device power loss for three different technologies.

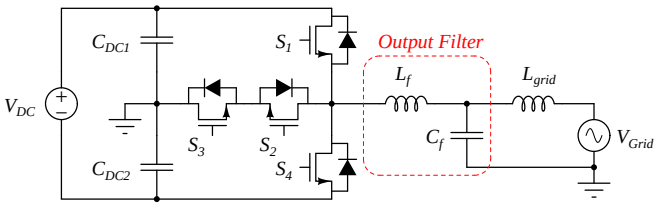


Fig. 15. Grid connected single-phase T-type inverter.

B. Filter Design

Grid connected power inverters must have output filter in order to minimize the injected harmonics to the grid that are caused by high switching frequency. Passive filters are usually chosen in grid connected applications due to its simplicity and high performance. The size of the filter depends on number of stages and order of the filter. One of the most common type of filter is second order single stage LC filter at considered power range and presented in Fig. 15 [40]. L_{grid} in Fig. 15 is the impedance of the grid after point of common coupling and can depend on the length of grid cables, connected loads and sources to the grid.

Passive component and output filter volume is inversely proportional to switching frequency. Therefore, it is interesting to analyse the trade-off between increased power losses due to increased switching frequency and reduction in filter volume. To begin the analysis, expressions that define efficiency with respect to switching frequency at 2500W output power and heat sink temperature are given in 4, 6 and 8. In this study, single stage LC filter, which is the common type differential output filter for power converters at this power range, is considered [40]. The design of LC filter starts with calculation of filter inductance L_f for defined maximum output ripple current by using 14. Calculated Lf is then used in 15 in order to calculate output capacitance:

$$L_f = \frac{V_{DC}}{8\Delta I_{OUT} f_s} \tag{14}$$

$$C_f = \frac{1}{(2\pi f_s)^2 L_f Att_{req}} \tag{15}$$

Where V_{DC} is DC link voltage, ΔI_{OUT} is output current ripple, f_s is switching frequency and Att_{req} is required attenuation of the filter [40], [41]. The required attenuation is chosen as 0.01 in order to provide adequate damping at switching frequency and keep the resonance frequency far away from inverter switching frequency. Output ripple current is chosen 20% of peak output current for limiting maximum power device switching current and keeping inverter output current ripple in reasonable level. By using inductance and capacitance values, volume of the LC filter can be calculated by using area-product approach for inductor and capacitor volume constant for capacitor. After [42], the area-product A_p and volume of a power inductor and volume can be calculated as:

$$A_p = \left[\frac{\sqrt{1+\gamma} K_i L_f \widehat{I}^2}{B_{max} K_t \sqrt{k_u \Delta T}}\right]^{\frac{8}{7}} \tag{16}$$

$$Vol_L = k_L {A_p}^{\frac{3}{4}} \tag{17}$$

Where γ is ratio of iron loss to copper loss (is taken to be 0.03 or less for AC inductors with small high frequency flux ripple), B_{max} is maximum flux density of inductor core, K_i is current waveform factor ($I_{rms}/\widehat{I}$), K_t is 48.2×103, $\widehat{I}$ is peak inductor current, k_u window utilization factor (based on window fill factor, proximity and skin effects) and k_L is inductor volume constant. Maximum flux density is based on performance factor of ferrite material ($f \times B_{max}$) N87 in [43]. Maximum temperature rise ΔT is chosen as 60^oC in order to keep current density in the windings high enough while keeping maximum core temperature within recommended operating temperature limits. Inductor volume constant vary for different types of cores, therefore it has been calculated and presented in Fig. 16a with respect to designed inductors' area-product and total volume. The constant increases slightly with respect to switching frequency and this affect can be represented with a first order polynomial shown in 18 and represented with blue curve in Fig. 16a.

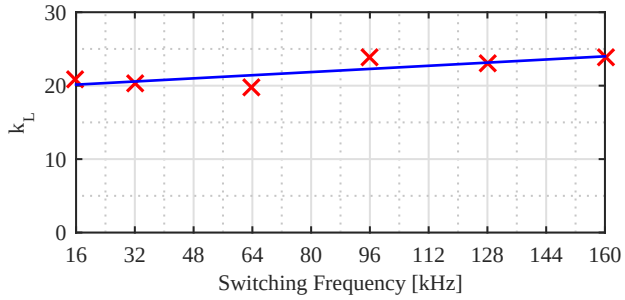
$$k_L = 2.676 \times 10^{-5} f_s + 19.71 \tag{18}$$

The inductor volume at different switching frequencies based on analytical calculation and actual design are presented in Fig. 16b. It is clear that analytical calculation is well matched with design results and can be used further in calculation of total volume of output filter for Si, SiC and GaN solutions at different switching frequencies.

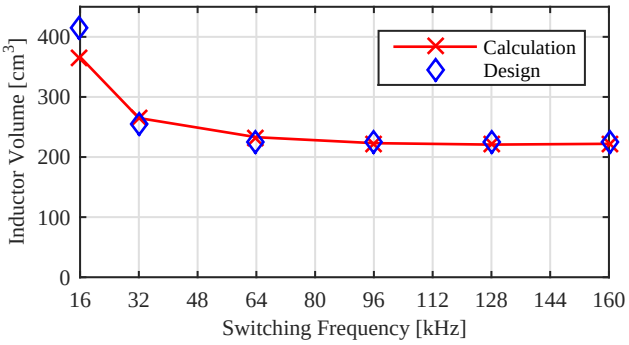
The next step in volume analysis of LC filter is filter capacitor. The volume of filter capacitor can be calculated by the following equation:

$$Vol_C = k_c C_f {V_{nom}}^2 \tag{19}$$

Where V_{nom} is nominal voltage of capacitor and kc is capacitor volume constant in $cm^3/\left(V^2F\right)$. The minimum capacitor volume constant is calculated as 72 for X2 type



(a)



(b)

Fig. 16. (a) Inductor volume constant and (b) inductor volume.

capacitors according to datasheets of different capacitance values in [44]. Based on calculation of inductor and capacitor volumes in 16 to 19, the volume analysis of LC filter with respect to power loss for three different semiconductor technologies is presented in Fig. 17. It should be noted that Si IGBTs are not feasible above 64kHz due to high losses and switching times, but they are included in this study in order to compare the WBG technology with Silicon over a wide switching frequency range. The volume of output inductor and capacitor are calculated for switching frequencies between 16 and 160kHz. The inductor volume dominates the output filter volume with 20% ripple current and 0.01 required attenuation. The reduction in filter volume becomes less pronounced below 240cm^3 for all device technologies and increase in switching frequency does not bring significant reduction in filter volume. The main reasons are decrease in B_{max} and window utilization factor k_u with increase of switching frequency that increase core volume and winding volume respectively. On the other hand, filter volume can be reduced by 43% with 24W, 26W and 61W increase in device power loss for GaN, SiC and Si based converters respectively. It should be noted that the inductor size is calculated for specific current density and core loss density, therefore reduction in inductor volume will reduce filter losses and make the efficiency penalty for increasing f_s less important.

C. Dead-time Effect on Harmonics

Small time interval between commutating switches S_1 and S_2, and S_3 and S_4, where both switches are turn-off, is introduced in order to avoid shoot through. During dead-time, the control of output voltage is lost and the output voltage

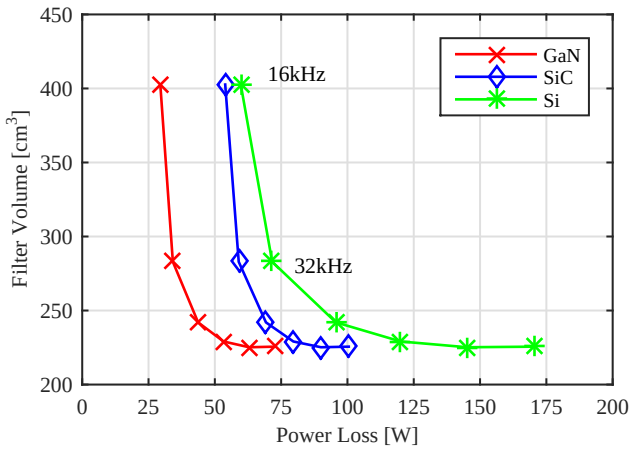


Fig. 17. Output LC filter volume vs. device power loss for three different device technologies.

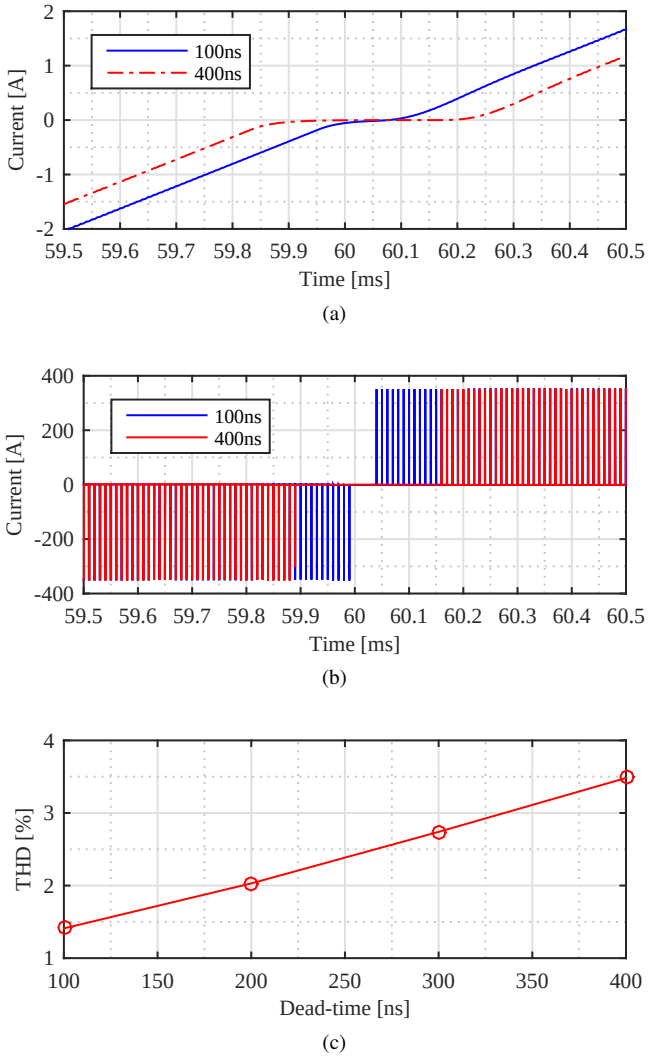


Fig. 18. Effect of different dead-time values to: (a) output current zero crossing, (b) output voltage, (c) output current total harmonic distortion.

can be clamped to +V_{DC}/2, -V_{DC}/2 or 0 depending on the direction of current. The effect of dead-time becomes severe when at higher switching frequencies and lower modulation index values. The harmonic analysis and compensation of dead-time effect for voltage source converters have been studied in [45], [46]. In this study, it is defined as 400ns in this study in order to make the comparison between Si IGBT and wide-bandgap devices but the switching results of SiC and GaN in the previous sections show that the dead-time for wide-bandgap devices can be as small as 100ns due to high switching speeds. In order to evaluate the effect of dead-time in T-type inverter with wide-bandgap technology, simulations are conducted with 100ns and 400ns dead-time values. The switching frequency is set as 100kHz and results are presented in Fig. 18. The effect of two different dead-time values to output current at zero crossing is shown in Fig. 18a. The reason for this distortion is due to elimination of output voltage pulses in Fig. 18b with duty ratio of less than 0.04 and 0.01 for 400ns and 100ns dead-times respectively. The blanking in the output current increases the total harmonic distortion (THD) and therefore output filter requirements. The variation of output current THD with respect to dead-time is presented in Fig. 18c. It is clear that minimum dead-time value has to be used with SiC and GaN devices regardless efficiency concerns in order to utilize high switching performance that allows reduction in filter volume.

VII. Conclusion

In this paper, the performance benchmark of T-type inverter with Si IGBT, SiC MOSFET and GaN HEMT at 600V blocking voltage range is presented. The benchmark covered gate driver requirements, switching performance, inverter efficiency performance, heat sink volume, output filter volume, and dead-time effect for each technology. Gate driver study shows that GaN HEMT has the lowest gate driver losses above 100kHz due to lowest input capacitance and below 100kHz, SiC MOSFET has lowest gate losses due to continuous current requirement of GaN HEMT during turn-on. In terms of switching performance, GaN HEMT has the best performance among three technologies at 350V, 16A and allows high efficiency at high frequency applications. GaN based inverter operated up to 160kHz switching frequency with 97.3% efficiency at 2.5kW output power, 160kHz and reached 99.2% efficiency at 1.4kW output power, 16kHz switching frequency. Performance evaluation of three device technologies at different temperature, switching frequency and load conditions shows WBG device provide robust performance under wide temperature and switching frequency conditions. Therefore, the heat sink volume of the converter can be reduced by 2.5 times by switching from Si to GaN solution at 60^{o}C case temperature at 32kHz, and for SiC and GaN based inverters, heat sink volume can be reduced by 2.36 and 4.92 times respectively by increasing heat sink temperature to 100^{o}C with increase of 16% and 12% in device losses respectively. Output LC filter volume can be reduced by 43% with 24W, 26W and 61W increase in device power loss for GaN, SiC and Si based converters respectively. Fast switching of WBG devices allows

reduction of dead-time from 400ns to 100ns and therefore total harmonic distortion at output current from 3.5% to 1.5% at 100kHz.

ACKNOWLEDGEMENT

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APPENDIX

Theoretical conduction loss analysis of the T-type converter is as follow [38]:

$$P_{c-S_{1,4}} = \frac{v_{o,S}M\widehat{I}_{OUT}}{4\pi}\left[sin\left(\phi\right)+\left(\pi-\phi\right)cos\left(\phi\right)\right] + \frac{r_{o,S}M\widehat{I^2}_{OUT}}{4\pi}\left[\frac{8}{3}cos^4\left(\frac{\phi}{2}\right)\right]$$

$$P_{c-D_{1,4}} = \frac{v_{o,D}M\widehat{I}_{OUT}}{4\pi}\left[sin\left(\phi\right)+\phi cos\left(\phi\right)\right] - \frac{r_{o,D}M\widehat{I^2}_{OUT}}{2}\left[\frac{4}{3\pi}sin^4\left(\frac{\phi}{2}\right)\right]$$

$$P_{c-S_{2,3}} = \frac{v_{o,S}\widehat{I}_{OUT}}{pi}\left[1-\frac{M}{4}\left(2sin\left(\phi\right)-\left(2\phi-\pi\right)cos\left(\phi\right)\right)\right] + \frac{r_{o,S}\widehat{I^2}_{OUT}}{4}\left[1-\frac{4M}{3\pi}\left(1+cos^2\left(\phi\right)\right)\right]$$

$$P_{c-D_{2,3}} = \frac{v_{o,D}\widehat{I}_{OUT}}{pi}\left[1-\frac{M}{4}\left(2sin\left(\phi\right)-\left(2\phi-\pi\right)cos\left(\phi\right)\right)\right] + \frac{r_{o,D}\widehat{I^2}_{OUT}}{4}\left[1-\frac{4M}{3\pi}\left(1+cos^2\left(\phi\right)\right)\right]$$

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Emre Gurpinar (S'11) received the Bachelor of Science degree in electrical engineering from Istanbul Technical University, Istanbul, Turkey, in 2009 and the Master of Science degree in power electronics, machines and drives from the University of Manchester, Manchester, U.K. in 2010. After working as R&D Power Electronics Engineer with General Electric, U.K., he joined the University of Nottingham, U.K. as a Ph.D. candidate in 2013. He is currently working on his PhD thesis based on wide-bandgap semiconductor based renewable power converters. He was a visiting PhD student at Department of Energy Technology, Aalborg University, Denmark between August 2015 and October 2015. His research interests include wide-band-gap power devices, high-frequency converters, renewable power systems and hybrid multi-level inverters.

Alberto Castellazzi received the Laurea degree in physics from the University of Milan, Milan, Italy, in 1998 and the Ph.D. degree in electrical engineering from the Munich University of Technology, Munich, Germany, in 2004. He is an Associate Professor of power electronics with The University of Nottingham, Nottingham, U.K. He has been active in power electronics research and development for over 15 years and has had extensive collaborations with major European and international industrial research laboratories and groups on publicly and privately funded research projects. He has authored or coauthored over 130 papers published in peer reviewed specialist journals and conference proceedings, for which he also regularly acts as a reviewer. His research interests include characterization, modelling, application, packaging and cooling of power devices. He is a member of the Technical Programme Committee of the ISPSD, ESTC and ECCE-Asia.