Single-Stage Push–Pull Boost Converter With Integrated Magnetics and Input Current Shaping Technique

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***Abstract*—This paper presents a novel single-stage push–pull boost converter with improved integrated magnetics and a better low-ripple input current. Most of the reported single-stage power factor corrected (PFC) rectifiers cascade a boost-type converter with a dc–dc converter. It is found that the push–pull converter, when the duty cycles are greater than 50%, can simplify the front end of the boost-type converter to a novel single-stage converter. Coupled inductor techniques provide a method to reduce the converter size and weight and to achieve a ripple-free current. All the magnetic components including the input filter inductor and the step-down transformer are integrated into a single EI core. The proposed integrated magnetic structure has a simple core structure, a small leakage inductance, and low core losses. The prototype is built to demonstrate the theoretical prediction.**

***Index Terms*—Integrated magnetics, push–pull boost converter, ripple-free, single-stage.**

I. Introduction

In RECENT years, a number of single-stage input current shaping converters have been introduced in [1]–[5]. It is found that many of these topologies can be implemented by combining a two-terminal or three-terminal boost input current shaper cell with dc–dc converter along with an energy storage capacitor in between [6], [7]. This capacitor must be realized by a conventional power component with high current stress. The major disadvantages of the conventional two-stage conversion approach are the added cost, the high current stress, and the complexity of the two-control loop two-power-stage nature. The single-stage power factor corrected (PFC) ac/dc converters integrated the two power stages into one, thus reducing significantly the component count and cost and gaining much attention in many low-power applications during the past ten years.

Fig. 1(a) shows the preregulated dc–dc boost converter with a parallel dc transformer. The switching power circuit (SPC) uses three main switch elements. The two converters are controlled independently to achieve output voltage regulation. The duty cycles of the switches $S1$, $S2$, and $S3$ are 50%, 50%, and D, respectively. The duty ratio D may be larger or less than 50%. Fig. 1(b) shows the switching sequence of the three main-switches. In a general sense, the two main switches of the traditional push–pull converter operate alternately, with conduction duty cycles of 50% during one complete switching cycle. These switching actions generate a symmetrical and alternating voltage across the primary of transformer. It is found that the push–pull converter, when the duty cycles greater than 50%, leads to conduct overlap intervals. Conduction overlap of primary switches causes high current spikes during such intervals. If the transformer is supplied from a voltage source and both switches are ON simultaneously, there is very little impedance to limit the switch current amplitudes and the switches could very well be damaged or destroyed as a result. A boost converter is added to the front end of the conventional push–pull converter for PFC as shown in Fig. 1(a). Thus, the possibility of damage is removed. The energy stored in the input inductor follows any overlap interval of two switches. At the next interval, the energy is delivered to the output network. One of the advantages of the overlapping primary switch conduction is the equal division of the inductor current in two switches, thus reducing their average and rms current levels as well as the primary winding rms current magnitude. When MOSFET devices are used as the switch elements, a significant improvement in conversion efficiency can be achieved.

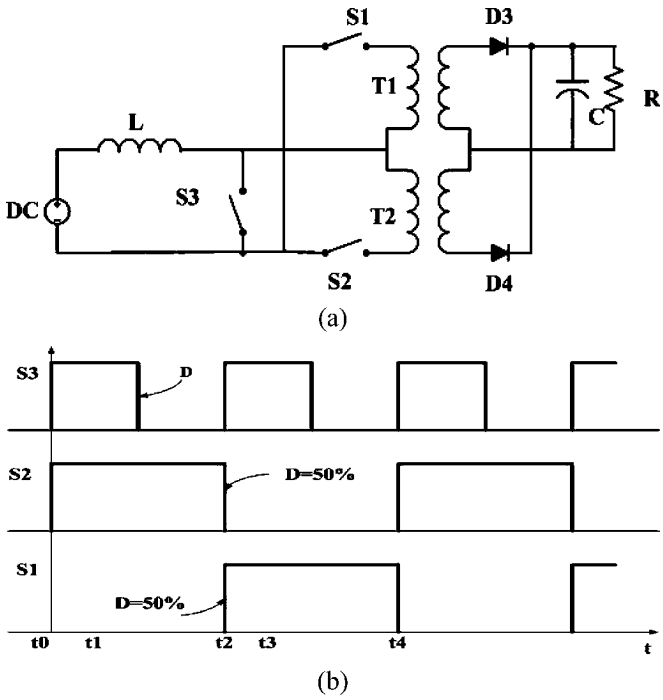

Fig. 1. Preregulated dc–dc boost converter. (a) Power circuit. (b) Switching sequences with $S1$ and $S2$ duty ratio equal to 50%.

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An application of the zero-ripple technique to converter structure is described in [8]. In this paper, the zero-ripple technique is applied to the proposed push–pull converter. For basic consideration, it seems to be perfect that only by extending a basic converter structure by a defined magnetic coupling of the input and filter inductors can a complete elimination of the input current ripple be obtained. It is shown that the ripple suppression can be achieved only on the input side or on the output side. A circuit consisting of passive elements cannot have an infinite high effective input inductance for all frequencies. The impossibility of a complete suppression of the input current ripple of the converter becomes clearly understandable. Therefore, the system should be labeled better low-ripple boost converter and not zero-ripple boost converter. In addition, coupled inductor techniques supply a method to reduce the converter size and weight and to achieve ripple-free current. In order to improve efficiency and reduce size, this paper proposes an improved push–pull boost converter with integrated magnetics. In this structure, all the magnetic components including input inductor, input filter inductor, and step-down transformer are integrated into a single EI core. The proposed integrated magnetic structure has a simple core structure, a small leakage inductance and low core losses. The prototype is built to demonstrate the theoretical prediction.

This paper is organized as follows. Section I introduces the research background and the motivation of this work. Section II briefly reviews basics considerations. Section III proposes an improved push–pull boost converter with integrated magnetics. Section IV provides experimental results.

II. Preliminary Consideration

In order to clearly explain the proposed converter, we want to consider the primary concepts in the following.

A. Single-Stage

There are several interesting state-of-the-art single-stage solutions [1]–[5]. Single-stage solutions supply the load with a constant and fast-regulated dc voltage, while in most cases the line current is not sinusoidal. The pulsed current deteriorates the line voltage, produces radiated and conducted electromagnetic interference, and leads to poor utilization of the capacity of the power sources. For single-phase electronics applications, passive power filters, active one and two-stage PFC rectifiers are typical approaches used to achieve high power factor and low total-harmonic distortion (THD). Compared with the two-stage approach, many strategies have been developed to reduce the size and the cost and to improve the efficiency.

In this paper, an improved boost-derived push–pull converter is proposed as shown in Fig. 2(a). It is found that the push–pull converter, when the duty cycles are greater than 50%, can operate in an interesting condition. Therefore, it acts as a combination of the front end of the boost-type converter and a novel single-stage converter.

If the duty cycles of $S1$ and $S2$ are made variable and always greater than 50%, and it can be eliminated, as shown in Fig. 2(a); i.e., if $S1$ and $S2$ have overlapping conduction interval, then $S3$ is no longer needed. Fig. 2(b) shows the switching sequences of the two main switches and a pseudo switch $S3'$. As a result, the proposed single-stage push–pull boost converter as shown in Fig. 3(a) integrates a ripple-free input current shaper and an isolated push–pull converter with two shared switches and controllers. One of the advantages of the overlapping primary switch conduction is the equal division of inductor current between $S1$ and $S2$, thus reducing the switch stress and improving conversion efficiency. The proposed push–pull boost converter in Fig. 3(a) with the duty cycles greater than 50% is a suitable approach for ripple-free input current. Fig. 3(b) shows the main typical waveforms of the converter in a switching cycle. This will be verified in the following sections.

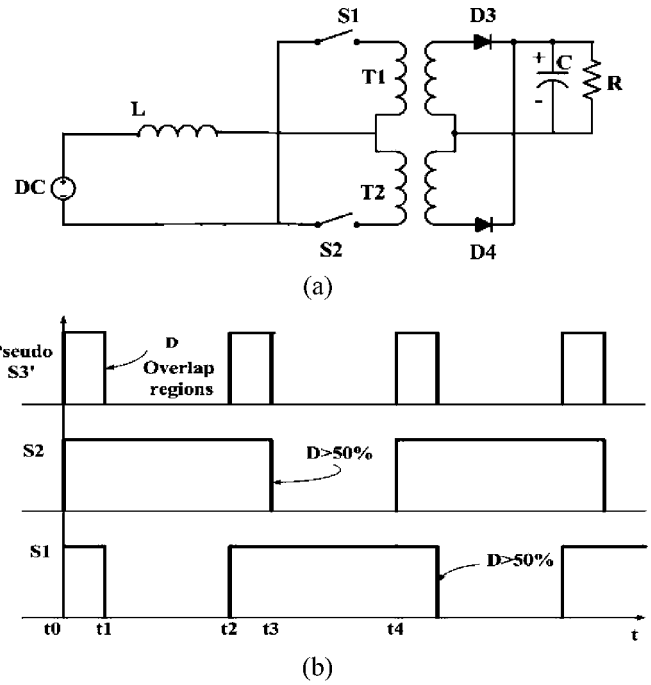

Fig. 2. Improved boost-derived push–pull converter. (a) Power circuit. (b) Switching sequences with $S1$ and $S2$ duty ratio greater than 50%.

B. Ripple-Free Input Current

In order to explain the effect called zero-ripple phenomenon in Fig. 3(a) [8], we want to consider briefly the relationships given for magnetic coupling of the two ports networks shown in Fig. 4(a). The two ports network is part of Fig. 3(a), and the nodes are indicated by ①, ②, and ③. Fig. 4(b) is the equivalent circuit of Fig. 4(a) which is represented by an ideal transformer ($N1 : N2$) and a mutual inductance $L_{\rm M}$, where $L_M = \sqrt{L_1 L_2}$ under ideal conditions. The elimination of the ideal transformer from Fig. 4(b) results in the simple model of Fig. 4(c) by transformation from the primary to the secondary side. The secondary equivalent inductance is $(N_2/N_1)^2 L_M$. The following mathematical deriving from Fig. 4(c) is used to analyze the ripple cancellation [9], [11], [12].

Let us now make the assumption that it is possible to reduce the value of i_1 to zero in our model as shown in Fig. 4(c); and let us examine the circuit currents and voltages that result from our assumption. If i_1 is zero, then the ac voltage drop across $L1$ must also be zero, as illustrated in Fig. 4(a). The voltage appearing across $L_{\rm M}$ must therefore be equal to that of the secondary voltage source, $(N2/N1)Vs$, reflected through the ideal transformer in the model. Also, the current through $L2$ and $L_{\rm M}$ must be equal to that produced by the secondary voltage,

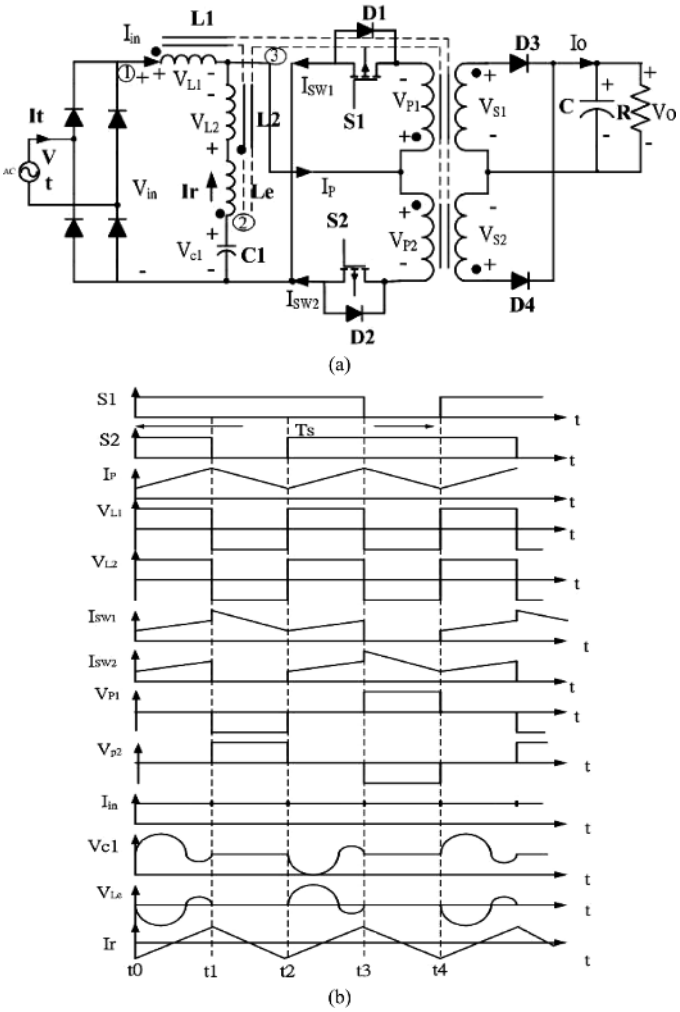

Fig. 3. Proposed push–pull boost converter. (a) Power circuits. (b) Main typical waveforms.

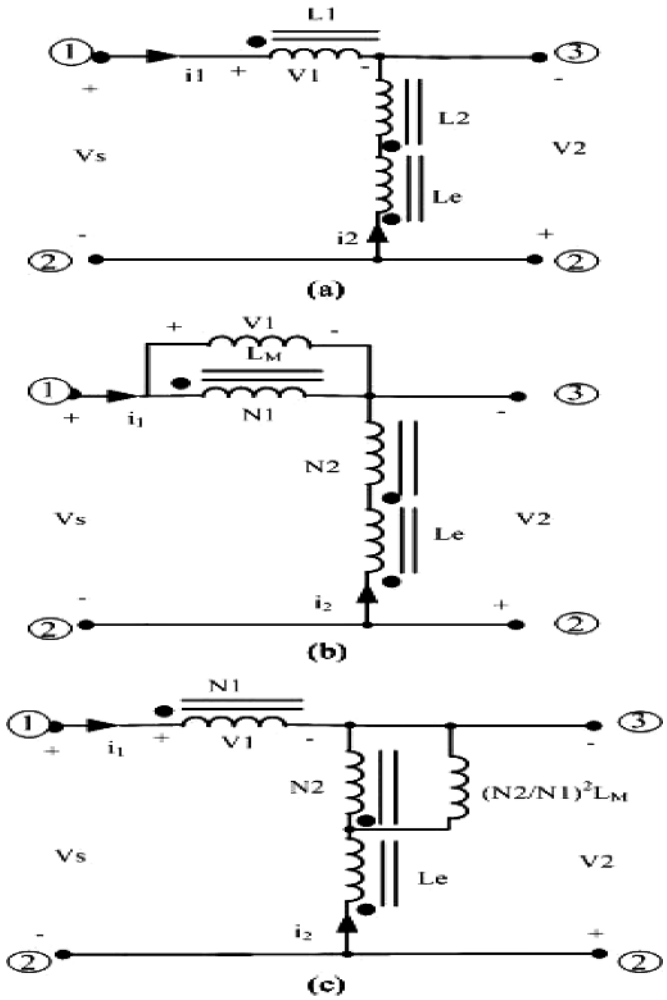

Fig. 4. Two-port network of the magnetic coupling. (a) Proposed coupling inductor. (b) Equivalent circuit of (a). (c) Equivalent circuit of (b).

$V2$. These conditions lead to the simplified circuit model of Fig. 3(c), where

$$\frac{N2}{N1}V1 = \left(\frac{N2}{N1}\right)^2 L_M \frac{di_2}{dt} \tag{1}$$

$$V2 = Le\frac{di_2}{dt} + \left(\frac{N2}{N1}\right)^2 L_M \frac{di_2}{dt} \tag{2}$$

$$Le = \left(\frac{N2}{N1}\right) L_M \left(\frac{V2}{V1} - \frac{N2}{N1}\right). \tag{3}$$

The relationship between secondary leakage inductance and that of the core material set by (3) is important and worth dwelling on for a moment. First of all, recall that this equation was derived based on the premise that no input ripple current existed in our model and, if satisfied, must produce this condition. It is known that there are several advantages to having $L1$ and $L2$ wound on the same core. One viable method is to tightly wind primary and secondary turns together to reduce the leakage inductance of $L1$ and $L2$ to essentially zero, and then insert a small external trimming inductor in series with the secondary sides to emulate the desired value of Le.

The initially analyzed basic principle of ripple elimination can now be applied to the proposed push pull converter. A coupling capacitor $C1$ has to be provided in order to suppress the occurrence of a dc voltage component across $L2$. If the capacitance $C1$ is selected sufficiently large, identical voltages across $L1$ and $L2$ will result. The zero-ripple phenomenon will be obtained only for the theoretical limiting $C1 \to \infty$. Therefore, the assumptions mentioned in Fig. 4 are present for suppressing the ripple of the input current i_1 by proper choice of the Le. For a practical system realization a capacity value $C1$ as small as possible is desired in order to minimize size and weight of the converter. The average value $Vc1$ of the coupling capacitor is equal to the input voltages in the stationary case. That is, $Vc1 = V\text{in}$. Then, that follows for a small finite ripple of the input current $\Delta i_1 \approx (\Delta v_{c1} \cdot T_s)/2\pi(L_1 - L_M)$ results. It acts like a low-pass filter lying at the converter input.

One has to point out that the low-pass filter is already an integral part of the basic converter structure. Thus, it does not have to be realized by additional power components; however, $C1$ for the conventional boost converter acts as an essential element of the energy transfer between the input and output sides. Therefore, the current stress on $C1$ is basically different from that of a

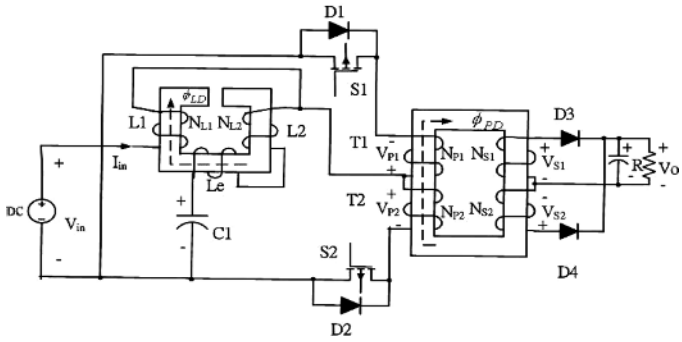

Fig. 5. Discrete magnetics of the proposed push–pull converter

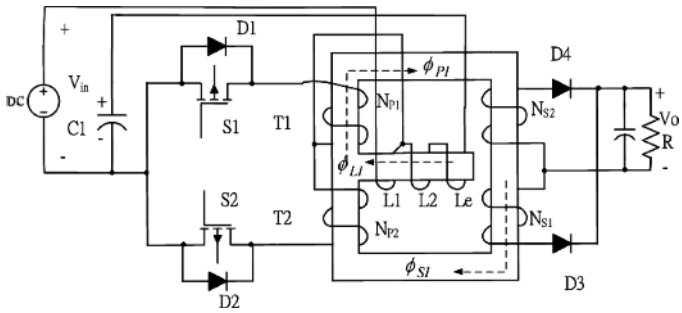

Fig. 6. Integrated magnetics of the proposed push–pull converter.

conventional filter capacitor. A circuit consisting of passive elements $L1$, $L2$, and $C1$ cannot have an infinitely high effective input inductance for all frequencies. Thus, a complete suppression of the input current ripple is impossible. The system shown in Fig. 3(a) should be labeled a better low-ripple converter and not a zero-ripple converter.

C. Integrate Magnetics

From Fig. 3(a), the magnetic core requires inductive elements like $L1$, $L2$, and transformer $T1$, $T2$. The SPC circuits of Fig. 5 are discreted magnetic versions of boost and push–pull topologies with transformer isolation. Let us now see if we can formulate an easy way to synthesize an integrated magnetic version of Fig. 6, given the discrete-magnetic circuit arrangements as starting points. To begin, we must first reconstruct the circuit schematics of Fig. 5 so as to detail the magnetic aspects of the transformer and inductor components. The schematics along with the result from this reconstruction process are illustrated in Fig. 6. Note that a flux direction within each magnetic component has also been assigned, based on winding polarities produced by converter operation. Next, for each of the switching intervals of the converters, a set of equations defining the rate of change of flux in each magnetic component is established [12]. For this exercise, we can assume all semiconductors of the SPCs are ideal in order to simplify our work. Also, we will ignore potential leakage inductance effects between transformer windings for the same reason, and assume that fluxes are completely contained within its core structure.

Thus, for the converter of Fig. 5 during interval I ($S1, S2ON$)

$$\dot{\phi_{LD}} = \frac{d\phi_{LD}}{dt} = \frac{V\text{in}}{N_{L1}}. \tag{4}$$

For the converter of Fig. 5 during interval II ($S1ON, S2$ OFF)

$$\dot{\phi_{LD}} = \frac{d\phi_{LD}}{dt} = \frac{V_{P1}}{N_{L1}} - \frac{V\text{in}}{N_{L1}} \tag{5}$$

$$\dot{\phi_{PD}} = \frac{d\phi_{PD}}{dt} = \frac{Vo}{N_{S1}} = \frac{V_{P1}}{N_{P1}}. \tag{6}$$

From (5) and (6), we can combine them to eliminate the dependent variable, V_{P1}. Performing this combination gives

$$\dot{\phi_{PD}} = \dot{\phi_{LD}}\left(\frac{N_{L1}}{N_{P1}}\right) + \frac{V\text{in}}{N_{P1}}. \tag{7}$$

Note that the last term of (7) is of a form that could be considered as defining a flux change in a magnetic medium that is dependent on the input voltage, $V\text{in}$, of the converter and the number of primary turns on the converter's transformer, N_{P1}. Since our goal is to make the inductor a part of the same magnetic assembly that contains the transformer component, it is logical to assume that N_{L1} should be made equal to N_{P1}, so that all of the flux change is contained within one magnetic path or leg of this assembly. Therefore, we arrive at an expression for $\dot{\phi}_{PD}$ as

$$\dot{\phi_{PD}} = \dot{\phi_{LI}} + \dot{\phi_{SI}} \equiv \dot{\phi_{PI}}. \tag{8}$$

We can interpret (8) as defining a magnetic assembly in which there are three major flux paths. It also tells us that the flux change in an input source-related path (ϕ_{PI}) contributes to the change in another path associated with the inductor portion of the magnetic assembly (ϕ_{LI}), as well as to flux change in a third path (ϕ_{SI}). These general observations permit us to sketch out a magnetic path arrangement that satisfies the needs of (8). This is done in Fig. 6. It shows the flux distribution in the core. The transformer and the filter inductors in the push–pull boost converter can be integrated into a single magnetic core. Note that we have added a gap in the inductor path area because we expect this leg will have significant dc bias, just as a discrete inductor in a boost converter would experience.

In order to improve the core structure and to reduce the leakage inductance of the existing integrated magnetics, a novel magnetic integration approach is proposed in [10]. First, since the transformer's primary winding is split between two outer legs, as shown in Fig. 6, interleaved windings can be used to minimize the leakage inductance of the integrated transformer. Second, the polarity of one set of windings is changed through different winding connections. Correspondingly, the direction of flux is changed as well. The air gap on the center leg prevents saturation of the core. The air gap will be the major factor in determining their winding inductance values, and increasing the air gap length will decrease the inductance of a magnetic material. Third, as shown in Fig. 6, auxiliary windings can be added to the center legs of the integrated magnetic converters to reduce input ripple current magnitudes. We can utilize the transformer equations of (3) to select the number of turns of this third winding so as to adjust the SPC's input current ripple to essentially zero. The gap inductance (Lg) is much smaller than that of the ungapped outer legs of the magnetic structure. Both center leg winding are wound tightly together to maximize magnetic coupling between them and to minimize

parasitic leakage inductances. The addition of this second winding does not compromise the input-to-output voltage gain of the converter, and it is defined in the following.

III. Proposed Push–Pull Boost Converter

The proposed push–pull converter with integrated magnetics is studied in this section. It can achieve continuous or better low-ripple input current with duty cycle greater than 50%. This section mainly discusses the steady-state and integrated magnetic properties of the proposed converter. It shows that the proposed boost converter has the same steady-state properties as the conventional boost converter. The prototype is built to demonstrate the theoretical prediction.

A. Principle of Operation

In boost-derived push–pull converters as shown in Fig. 3(a), switch duty cycle (D) is greater than 50% and a separate drive circuit will be necessary for each dc isolated switch element. The two switch elements have conduction duty cycles greater than 50%. Twice during each switching cycle, the two main switches are ON simultaneously. At the beginning of a switching cycle, $S1$ and $S2$ are ON. Inductor current therefore flows through $S1$ and $S2$. Energy to sustain the output voltage load comes from the filter capacitor C. When $S2$ turns OFF and switch $S1$ closes, it now allows the inductor current to flow through the primary of $T1$ and to deliver its stored energy to the output of the converter. One conversion stage consists of switches $S1$, transformer $T1$, diode $D1$, and rectifier diode $D3$. The other one consists of switches $S2$, transformer $T2$, diode $D2$, and rectifier diode $D4$. In addition, a two-port magnetic coupling cell is used for the input filter. Le is the small leakage inductance of the coupled inductor. In order to prevent parasitic ringing and negative undershoots across $S1$ and $S2$, caused by parasitic capacitance of $S1$ and $S2$, low current stress diodes $D1$ and $D2$ are used.

The switching sequences and theoretical waveforms of the proposed converter are illustrated in Fig. 3(b). As shown in Fig. 3(b), the switching sequence differs from that of universal push–pull converters. $S1$ and $S2$ are driven complementary with an overlap interval (mode 1). The output voltage can be regulated by varying this controllable interval as pulsewidth modulation (PWM) with a constant switching frequency. The principle of operation in a steady-state condition is described with the following assumptions.

- All the switches and components are ideal.
- Transformers $T1$ and $T2$ are identical.
- Inductance $L1$ and $L2$ are tightly coupled with each other.
- The output voltage Vo is assumed to be constant.

1) Mode 1 ($t_0 \le t < t_1$, $t_2 \le t < t_3$): With switches $S1$ and $S2$ ON as shown in Fig. 7(a), the inductor $L1$ is grounded. The input current, $I\mathrm{in}$ is increased, resulting in energy stored in $L1$. The current through $L2$, Ir is increasing and then changes its direction. Diodes $D1$ and $D2$ are not conducting during this period. The voltage across inductor $L1$ is the input voltage, $V\mathrm{in}$, and the voltage across inductor $L2$ is $V_{\mathrm{c1}} = V\mathrm{in}$.

2) Mode 2 ($t_1 \le t < t_2$): With switch $S1$ ON and $S2$ OFF as shown in Fig. 7(b), Ir releases the energy stored in $L1$ to the transformer $T1$. Ir is still keeping its positive direction; however, it is decreasing. The capacitor $C1$ is charged by Ir. The voltage across inductor $L1$ is ($V\mathrm{in}$–Vp). The voltage across inductor $L2$ should be $V_{\mathrm{c1}} - Vp = V\mathrm{in} - Vp$.

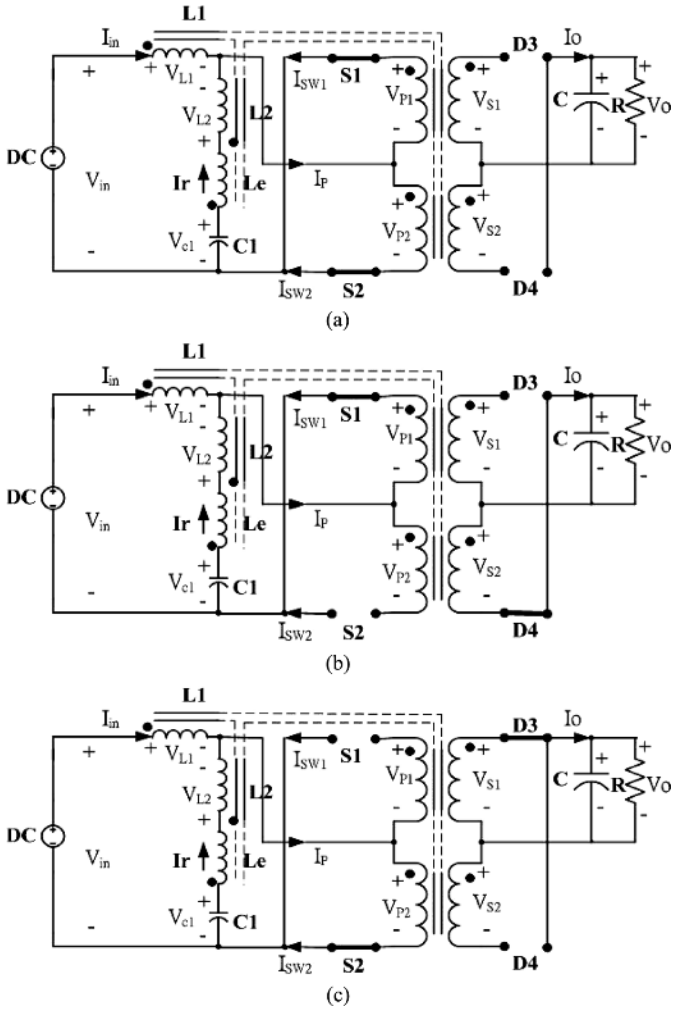

Fig. 7. Principle of operation circuits: (a) Mode 1, (b) Mode 2, and (c) Mode 3.

3) Mode 3 ($t_3 \le t < t_4$): With switch $S1$ OFF and $S2$ ON as shown in Fig. 7(c), Ir releases the energy stored in $L1$ to the transformer $T2$. The converter action operates the same as mode 2.

As a result, the inductances $L1$ and $L2$ have the same voltage waveforms during the whole cycle. It is possible to couple them and to achieve a reduced component count, reducing the amount of material, increasing the energy density, and achieving ripple-free input current [8]. The voltage relationships of Fig. 6, along with the right choice of leakage inductances (Le) associated with the inductor windings, are the key factors in achieving zero-ripple current at the input of the proposed push–pull converter.

The meanings of variables in this paper are listed in Table I.

B. Steady State Analysis

1) Voltage Gain: According to the voltage-second balance

$$V\mathrm{in}(D - 1/2)Ts = (Vp - V\mathrm{in})(1 - D)Ts \qquad (9)$$

where

$$\frac{Vo}{Vp} = \frac{Ns1}{Np1} = \frac{Ns2}{Np2} = \frac{1}{n}. \tag{10}$$

Thus, the following voltage gain can be derived

$$Mv = \frac{Vo}{V\text{in}} = \frac{1}{2(1-D)n}. \tag{11}$$

Considering the power balance $Pin = Po$, that is

$$V_{\text{in}} i_{\text{in}} = VoIo. \tag{12}$$

The current gain is

$$M_I = \frac{Io}{I\text{in}} = 2(1-D)n. \tag{13}$$

2) DC Characteristics: From Fig. 6, the average current of i_{L1} and i_{L2} can be derived as follows:

$$I_{avL1} = \frac{1}{4}(2D-1)\frac{V\text{in}}{L1}Ts + I \tag{14}$$

$$I_{avL2} = \frac{1}{4}(2D-1)\frac{V\text{in}}{L2}Ts - I. \tag{15}$$

It can be seen that the presence of the capacitor implies that $i_{\text{avL2}} = 0$ in steady state. Leq and K are defined as follows:

$$\frac{1}{Leq} = \frac{1}{L1} + \frac{1}{L2} \tag{16}$$

$$K = \frac{Leq}{R \cdot Ts}. \tag{17}$$

The output average current flows in mode2 and mode3, i.e., when the diode is conducting. Therefore

$$Io = \frac{nV\text{in}}{2Leq}(1-D)(2D-1)Ts. \tag{18}$$

Using the assumption of 100% efficiency, the average input current can be derived

$$I\text{in} = \frac{IoVo}{V\text{in}} = \frac{nVo}{2Leq}(1-D)(2D-1)Ts. \tag{19}$$

Summing i_{avL1} and i_{avL2}

$$\begin{aligned} I_{avL1} + I_{avL2} &= \frac{V\text{in}}{4Leq}(2D-1)Ts \\ &= \frac{nVo}{2Leq}(1-D)(2D-1). \end{aligned} \tag{20}$$

An interesting equation can be derived

$$I\text{in} = I_{avL1} + I_{avL2}. \tag{21}$$

This means that the averaged input current is equal to the sum of the currents through the two inductors.

Qualitatively, this must be true since $i_{\text{avL2}} = 0$.

3) Boundary Condition: Considering the power balance again, where

$$Po = Io^2 R \tag{22}$$

$$P\text{in} = I\text{in} \cdot V\text{in}. \tag{23}$$

Thus

$$n^2(1-\text{D})^2(2\text{D}-1)\text{TsR} = Leq \tag{24}$$

then substituting (17) into (24), that is

$$n^2(1-\text{D})^2(2\text{D}-1) = \text{K}. \tag{25}$$

It can be seen that continuous current mode can be achieved in the proposed topology. The boundary conditions are

$$\frac{1}{2} < D < 1 \tag{26}$$

$$M > \frac{1}{n} \tag{27}$$

$$K > 0. \tag{28}$$

4) Semiconductor Devices Stress: The switch average current is

$$Iavs1 = Iavs2 = \frac{V\text{in}Ts}{2Leq}\left(D - \frac{1}{2}\right)\left(\frac{3}{2} - D\right). \tag{29}$$

The diode average current is

$$I_{avD3} = I_{avD4} = \frac{nV\text{in}Ts}{2Leq}(1-D)(2D-1). \tag{30}$$

The switch peak current is

$$i_{pkS1} = I_{pkS2} = \frac{V\text{in}Ts}{2Leq}(2D-1). \tag{31}$$

According the previous analysis, Fig. 8 shows some characteristics curves for the proposed converter. It is operated in duty ratio greater than 50% and satisfies the typical boost converter characteristics.

C. Derivation of the Integrated Magnetics

A novel magnetic integration approach is proposed for the push–pull boost converter as follows. The flux directions are determined by using the right-hand rule as shown in Fig. 6. The current directions are defined as in the equivalent electrical circuit shown in Fig. 9. In the proposed structure, the polarity of one set of windings is changed and consequently, the direction of ac flux in one of the two outer legs is also changed. Therefore, the ac fluxes are canceled in the center leg. With the reduction of the magnitude of ac flux in the center leg, the proposed structure has a lower core loss in the center leg. Fig. 10 shows the ac flux distribution in the core for the proposed structure by using

TABLE I
PRINCIPLE SYMBOLS USED

D	**Switch-on duty ratio**	**Ir**	**Current through L2**	**M_V**	**Converter voltage gain**
Ts	**Period of one switching cycle**	**Ip**	**The sum of the current through L1 and L2**	**M_I**	**Converter current gain**
Vin	**Input voltage**	**Io**	**Output average current**	**Np1**	**The number of turns of the primary of transformer T1**
Vo	**Output voltage**	**I_{SW1}**	**Current through switch S1**	**Np2**	**The number of turns of the primary of transformer T2**
Vc1	**Voltage across C1**	**I_{SW2}**	**Current through switch S2**	**Ns1**	**The number of turns of the secondary of transformer T1**
V_{L1}	**Voltage across L1**	**I_{pkS1}**	**Peak current through switch S1**	**Ns2**	**The number of turns of the secondary of transformer T2**
V_{L2}	**Voltage across L2**	**I_{pkS2}**	**Peak current through switch S2**	**K**	**Coefficient: $K = Leq / R \cdot Ts$ Leq=L1//L2**
Vp1	**Voltage across primary of transformer T1 (Vp1=Vp)**	**I_{avL1}**	**Average current through L1**	**ψ_{PD}**	**Flux through transformer for discrete magnetics**
Vp2	**Voltage across primary of transformer T2 (Vp2=Vp)**	**I_{avL2}**	**Average current through L2**	**ψ_{LD}**	**Flux through inductor for discrete magnetics**
Vs1	**Voltage across secondary of transformer T1**	**I_{avS1}**	**Average current through switch S1**	**ψ_{PI}**	**Flux through primary of transformer for integrated magnetics**
Vs2	**Voltage across secondary of transformer T2**	**I_{avS2}**	**Average current through switch S2**	**ψ_{LI}**	**Flux through inductor for integrated magnetics**
Iin	**Average input current**	**I_{avD3}**	**Average current through diode D3**	**ψ_{SI}**	**Flux through secondary of transformer for integrated magnetics**

Ansoft simulations. The outer legs are averaging distributed in the core and larger than the center leg. It satisfies the former description.

From Fig. 6 we assume that the double transformer number of turns of the primary and secondary are the same. That is, $N_{\rm p1} = N_{\rm p2} \equiv Np$, and $N_{\rm S1} = N_{\rm S2} \equiv Ns$. And the current may be the same in an ideal situation. That is, $ip1 = ip2 \equiv ip$; $is1 = is2 \equiv is$. Fig. 9(a) shows the reluctance model for the proposed magnetic circuit. The electrical circuit model can be derived from the reluctance model by using the principle of duality, as shown in Fig. 9(b). The circuit of Fig. 9(c) results from scaling step with Np designated as the reference winding. The scaled permeances are then replaced by inductances. From the reluctance circuit shown in Fig. 9(a), the fluxes in the cores can be derived in the form of reluctances and MMF sources, as follows:

$$\phi_{PI} = \frac{\Re c + \Re g}{\Re c(\Re c + 2\Re g)} Np \cdot ip - \frac{\Re g}{\Re c(\Re c + 2\Re g)} Ns \cdot is \quad (32)$$

$$\phi_{SI} = \frac{-\Re g}{\Re c(\Re c + 2\Re g)} Np \cdot ip + \frac{\Re c + \Re g}{\Re c(\Re c + 2\Re g)} Ns \cdot is \quad (33)$$

where $\Re c$ and $\Re g$ represent the reluctances of the outer and center legs, and ip and is are the total winding currents reflected to the primary and secondary of the transformer, respectively. According to Farady's Law, and that the mutual inductance between Lp and Ls is M, and the coupling coefficient is k; the re-

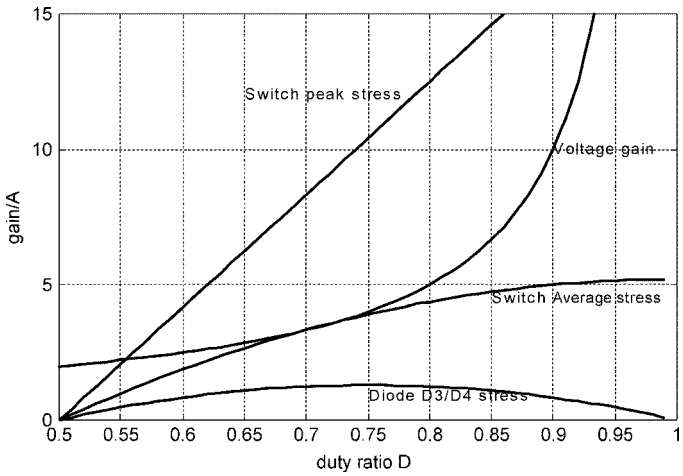

Fig. 8. Characteristic curves for the proposed converter.

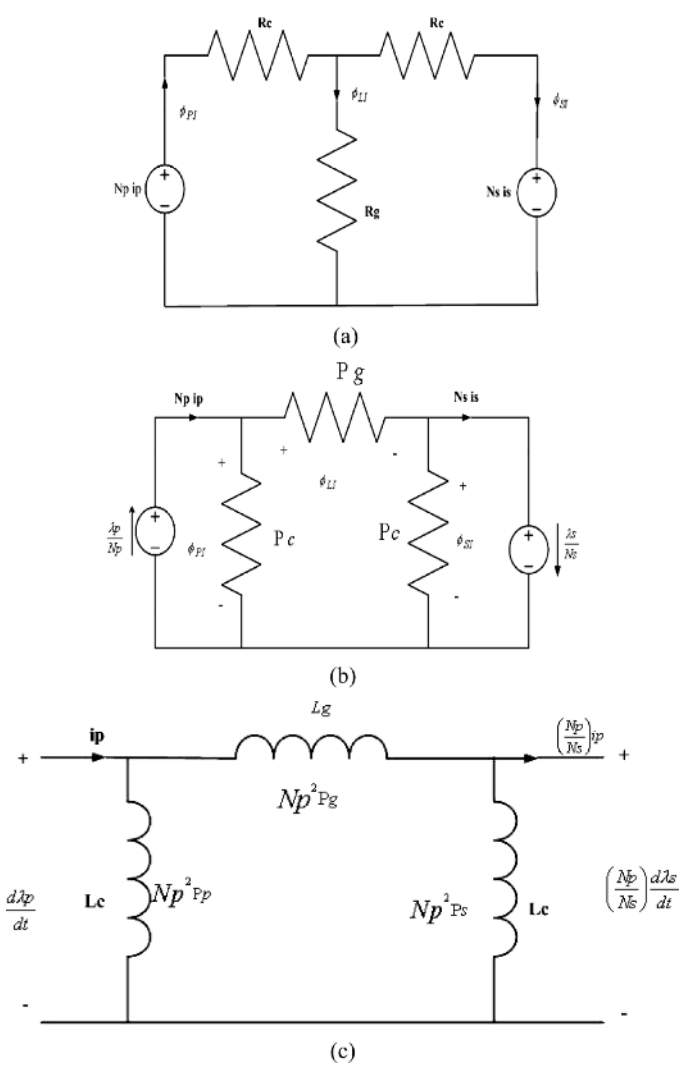

Fig. 9. (a) Reluctance model of proposed magnetic circuit. (b) Model (a) by using the principle of duality. (c) Model (b) of scaling step with Np designated as the reference winding.

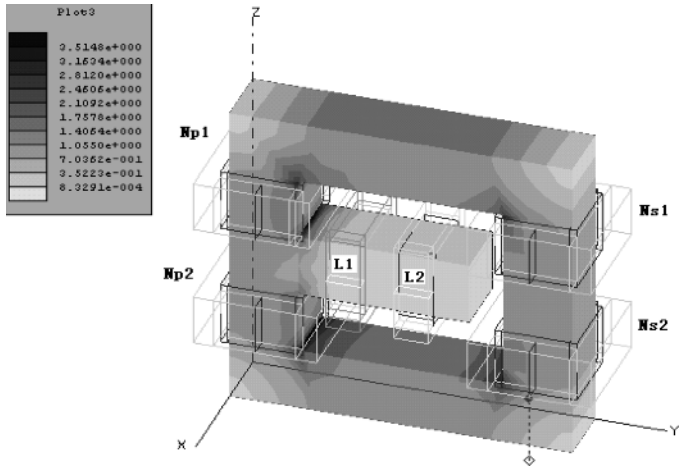

Fig. 10. Flux distribution of the proposed structure by Ansoft simulation.

lationship between inductances and reluctances can be derived as follows:

$$Lp = \frac{(\Re c + \Re g)Np^2}{\Re c(\Re c + 2\Re g)} \tag{34}$$

$$Ls = \frac{(\Re c + \Re g)Ns^2}{\Re c(\Re c + 2\Re g)} \tag{35}$$

$$M = \frac{\Re g NpNs}{\Re c(\Re c + 2\Re g)} \tag{36}$$

$$k = \frac{\Re g}{\Re c + \Re g}. \tag{37}$$

Similarly, from the reluctance circuit shown in Fig. 9(c)

$$Lp = Ls = \frac{LgLc + Lc^2}{Lg + 2Lc} \tag{38}$$

$$M = \frac{Lc^2}{Lg + 2Lc}. \tag{39}$$

Since the reluctances from the magnetic material are much smaller than that of the air gap, the reluctance in the center leg is much larger than those of the outer legs ($\Re g \gg \Re c$), (34)–(37) can be simplified as follows:

$$Lp \approx \frac{Np^2}{2\Re c} \tag{40}$$

$$Ls \approx \frac{Ns^2}{2\Re c} \tag{41}$$

$$M \approx \frac{NpNs}{2\Re c} \tag{42}$$

$$k \approx 1. \tag{43}$$

Similarly, $Lc \gg Lg$, (38)–(39) can be simplified as follows:

$$Lp = Ls = M \approx \frac{Lc}{2}. \tag{44}$$

As can be seen from (35) to (37), in the proposed integrated magnetic structure, the coupling coefficient for the transformer is close to one. Two coupled windings still have a certain amount of leakage inductance. In practice, the reluctances from the magnetic material influence the value of $\Re c$ and $\Re g$. We now have an

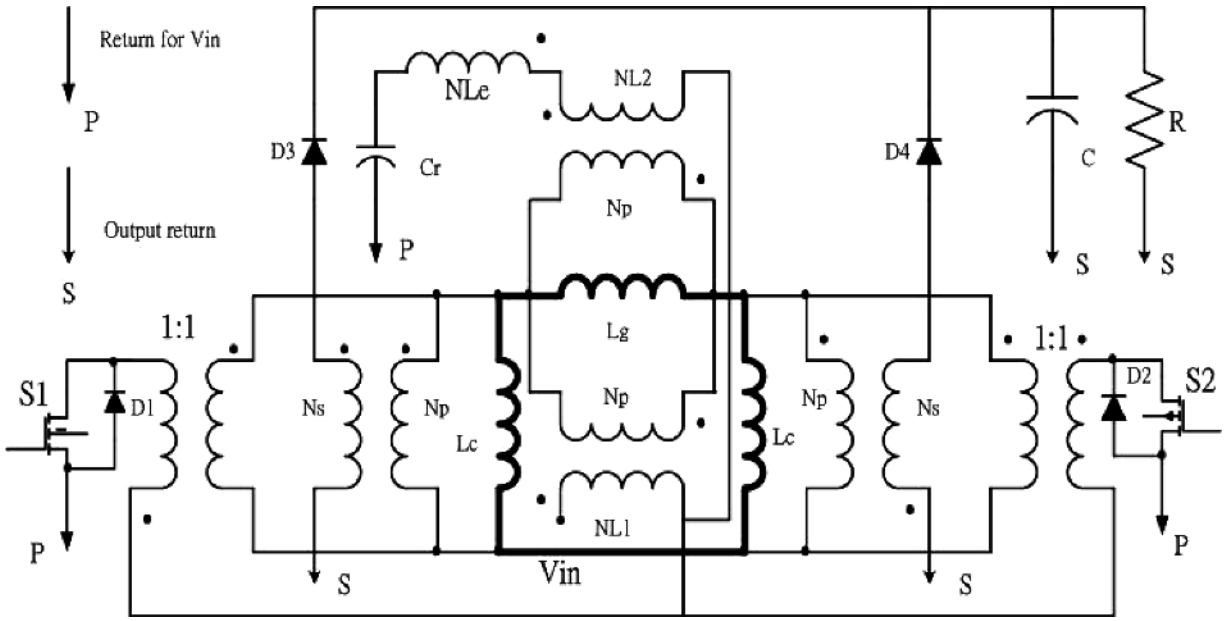

Fig. 11. Equivalent electrical circuit for the proposed integrated magnetic circuits.

electrical model for the magnetic circuit as shown in Fig. 9(c). Substituting this model into the proposed converter of Fig. 6, results in the equivalent SPC circuit shown in Fig. 11. Note that, in making this substitution, we have moved the inductance to the secondary side of the ideal transformer of turns ratio, $Np{:}Ns$ (N_{L1}, or N_{L2}). The two unit ideal transformers 1:1 are used for connecting the switch to the magnetic circuits for equivalent action.

D. Comparison of the Realization Variants

This section attempts to answer the question of how the application of a "zero" (or low)-ripple current technique for the proposed push–pull boost converter can be judged in comparison to a conventional passive filtering of the converter input current. Advantages of the converter structure according to Fig. 3(a) are as follows: i) only one magnetic core is required for the realization of the filter inductor and of the input inductor of the converter and ii) only a current ripple flows through inductor $L2$ and not, as for conventional filtering, the full load current. This results in a relatively small rated power of the magnetic core and in low ohmic losses in the winding. Overall, a relatively small realization effort and a relatively high power density $(\mathrm{W/in}^3)$ are given.

On the other hand, the following disadvantages have to be mentioned: i) a defined, reproducible value of the coupling between $L1$ and $L2$ can be guaranteed regarding manufacturing possibly only by an external balancing inductor lying in series to $L2$. The balancing of the winding turns ratios is connected with a relatively high manufacturing effort. ii) the magnetic integration of $L1$ and $L2$ leads possibly to a higher parasitic coupling capacitance of the windings and to a less efficient suppression of high-frequency electromagnetic influences. The arrangement of $L1$ and $L2$ has to be realized.

In summary, the decision between different realization variants of a "zero"-ripple boost converter has to be made, especially on the basis of manufacturing points of view. This paper presents a novel single-stage push–pull boost converter with an improved integrated magnetics and better low-ripple input current.

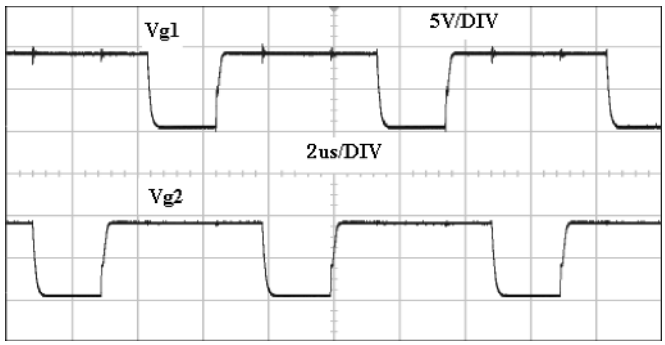

Fig. 12. Measured MOSFET gate voltage ($Vg1, Vg2$) waveforms.

IV. Experiment Result

The new push–pull boost converter was implemented, with the following specifications: nominal output power $Po = 150$ W; output voltage $Vo = 48$ V; input voltage $\mathrm{Vin} = 110$–120 V; switching frequency $fs = 150$ KHz. The power stage consists of the following parameter: Switches $S1$ and $S2$: power MOSFET's IRF 740; Diodes $D1$ and $D2$: HFA08TB60; Diodes $D3$ and $D4$: HFA15TB40; Capacitor $C1$: 10 μF; Couple inductor $L1 = L2 = 6.3$ μH; Extra inductor $Le = 1.3$ μH; Core: TDK EI 35; $Np1 = Np2 = 96$ turns; $Ns1 = Ns2 = 48$ turns; $N_{\mathrm{L1}} = N_{\mathrm{L2}} = 36$ turns; $Ne = 10$ turns; Load R: 10 Ω; and Output capacitor C: 1000 μF.

The switch conduction sequences of the proposed converter are shown in Fig. 12. It shows that the duty cycles greater than 50%. Thus, the proposed push–pull converter work in symmetrical continuous conduction boost mode. Fig. 13 shows the input voltage waves and input current waveforms with and without

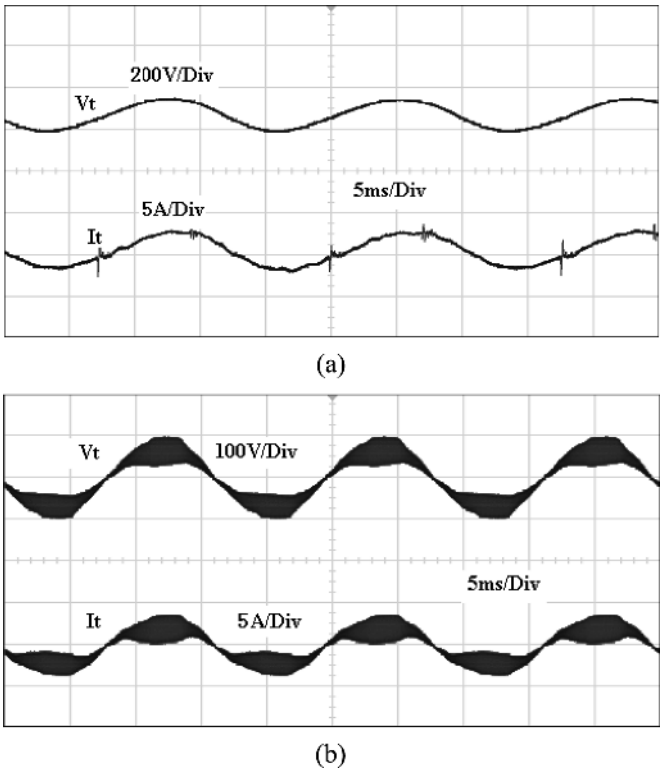

Fig. 13. Measured the input voltage (Vt) and line current (It) waveform: (a) with input current shaper and (b) without input current shaper.

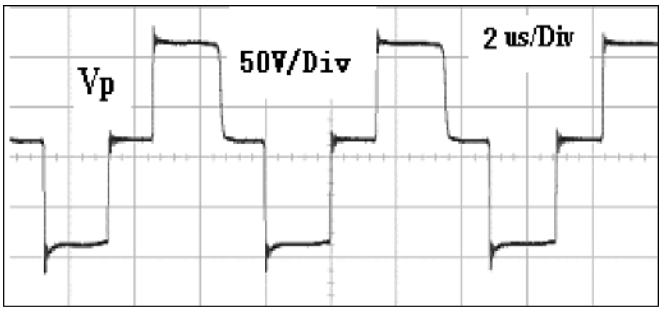

Fig. 14. Experiment results: the voltage across primary transformer (Vp).

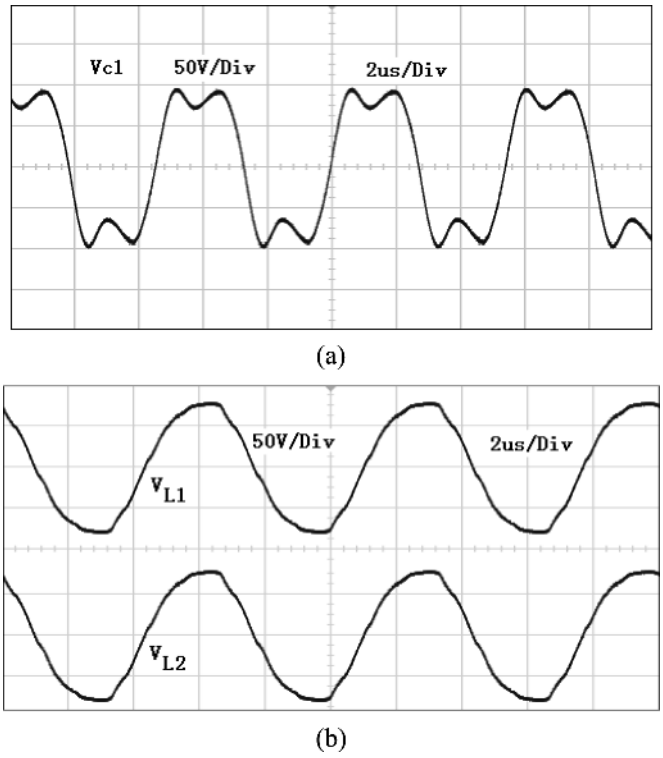

Fig. 15. Experiment results: (a) voltage across capacitor $C1$ and (b) the voltage across inductor $L1$, $L2$.

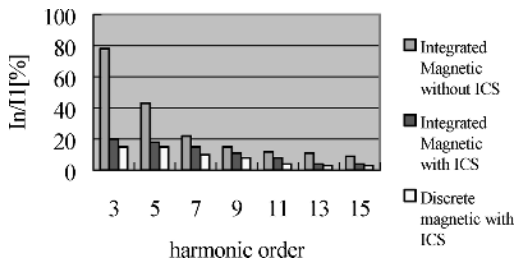

Fig. 16. Comparison of the corresponding line-current harmonics.

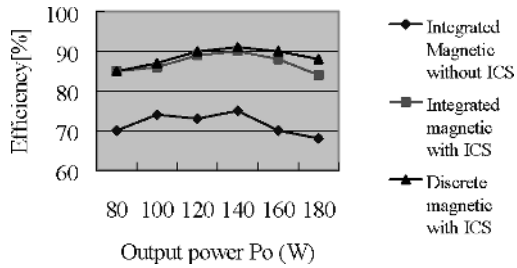

Fig. 17. Comparison of the efficiency.

input current shaper (ICS). The line current (It) and line voltage (Vt) of the proposed converter are shown in Fig. 13(a). It can be seen that the power factor is almost one. The ICS achieves a PFC and low ripple in this situation. And Fig. 13(b) shows the distortion input voltage waves for without ICS, where the ripple variation is very large. The voltage across primary transformer is shown in Fig. 14. The results are consistent with the typical waveforms in Fig. 3(b). Fig. 15(a) shows the voltage across capacitor $C1$ in the proposed topology. It can be seen that the voltage is the variation of $V\mathrm{in}$. And the voltages across inductor $L1$, $L2$ are shown in Fig. 15(b). It has the same wave and satisfied the theoretical prediction. In order to demonstrate the theoretical prediction, the proposed integrated magnetic converters with and without ICS and another discrete magnetic converter with ICS are implemented. The corresponding line-current harmonics are shown in Fig. 16 for three different cases. The odd order harmonics of input currents i_{h} are expressed as a ratio of the fundamental current i_1. The harmonic of the converter without ICS is the worst case. However, the harmonics of the proposed converter with integrated and discrete magnetic are approximately the same. It satisfies the better low-ripple condition. Finally, the efficiency of the power stage of the three different converters is shown in Fig. 17. The maximum value at full load is about 90%, and the converter without ICS filter is the worst case.

V. Conclusion

A novel simple single-stage push–pull ac–dc converter has been introduced. This converter can achieve small converter size and near zero-input current using coupled inductor techniques. The proposed circuit consists of a simple topology and control strategy. It has several advantages such as lower switch and diode stress and lower stresses on capacitor $C1$. This makes the conduction and switching losses low and may result in a high efficiency. In this paper, a small capacitor is normally used as the input filter in the proposed topology, while a significant low-pass filter is used in the conventional boost converter. It has been proven that the proposed boost converter has the same steady-state properties as the conventional boost converter. Blending of the inductors and transformers of SPCs into single magnetic systems can be very advantageous, often resulting in converter designs of lower cost, weight, and size than their discrete magnetic counterparts. Finally, conversion performance can also be improved and component stresses reduced, provided the integration process is well thought out and executed properly.

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