Single-Stage Single-Switch Input-Current-Shaping Technique with Fast-Output-Voltage Regulation

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***Abstract*— A new single-stage single-switch input-current-shaping (S^4ICS) technique, which combines the boost-like input-current shaper with a continuous-conduction-mode (CCM) dc/dc output stage, is described. In this technique, the boost inductor can operate in both the discontinuous conduction mode (DCM) and CCM. Due to the ability to keep a relatively low voltage (<450 V_{dc}) on the energy-storage capacitor, this technique is suitable for the universal line-voltage applications. The voltage on the energy-storage capacitor is kept within the desirable range by the addition of two transformer windings. The principle of operation of the S^4ICS circuit with a forward dc/dc converter is presented. Experimental results obtained on a 100-W (5-V/20-A) prototype circuit are also given.**

***Index Terms*— Fast-output-voltage regulation, line-current shaper, power factor correction, single-stage ac–dc converter.**

I. Introduction

THE HARMONIC content of the line current drawn from the ac mains by a piece of electronic equipment is regulated by a number of standards whose requirements depend on the type of the equipment and its power level [1]. To comply with these standards, input-current shaping (ICS) of off-line power supplies is necessary. So far, a variety of passive and active ICS techniques have been proposed. While the passive techniques can be the best choice in many cost-sensitive applications, the active ICS techniques are used in the majority of applications due to their superior performance.

The most commonly used active approach that meets high-power quality requirements is a two-stage approach [2]. In this approach, a nonisolated boost-like converter is used as the input stage that creates an intermediate dc bus with a relatively large second-harmonic ripple. This ICS stage is then followed by a dc/dc converter, which provides isolation and high-bandwidth voltage regulation. For high-power levels, the ICS stage is operated in the continuous conduction mode (CCM), while the discontinuous conduction mode (DCM) of operation is commonly used at lower power levels due to a simpler control.

Although relatively simple, mature, and viable in wide power-range applications, the two-stage approach suffers from several drawbacks. First, due to two-stage power processing, conversion efficiency is reduced. Second, a separate ICS stage adds components and complexity and, consequently, increases the cost. The cost increase is especially undesirable for low-power supplies used in consumer electronic products such as, for example, personal computers, low-end printers, home appliances, etc.

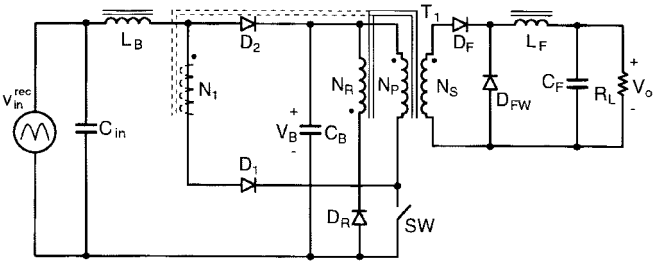

Fig. 1. S^4ICS forward converter introduced in [3]. Winding N_1, shown dashed, is added for improved performance as described in [8].

In an effort to reduce the component count and also improve the performance, a number of single-stage ICS techniques have been introduced recently [3]–[8]. In a single-stage approach, input-current shaping, isolation, and high-bandwidth control are performed in a single step, i.e., without creating an intermediate dc bus. Generally, these converters use an internal energy-storage capacitor to handle the differences between the varying instantaneous input power and a constant output power.

Among the single-stage circuits, a number of circuits described in [3], [5], [7], and [8] seem particularly attractive because they can be implemented with only one semiconductor switch and a simple control. Except for the circuit in [7], all other S^4ICS circuits employ the DCM operation in the ICS stage, mostly with boost topology. In fact, in these circuits, low-input-current harmonic distortions are achieved through the inherent property of the DCM boost converter to draw a near sinusoidal current if its duty cycle during a line period is held relatively constant. As an example, Fig. 1 shows the forward-converter implementation of the S^4ICS concept described in [3].

While boost inductor L_B in the ICS stage of the converter in Fig. 1 must operate in DCM, output filter inductor L_F can be designed to operate either in DCM or CCM. According to the analysis in [6], if L_F operates in CCM, the energy-storage capacitor voltage V_B shows a strong dependence on the line voltage and output current. In fact, V_B increases as the rms of the line voltage increases and/or output current decreases. For a converter in Fig. 1 designed for universal

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line-voltage range from 90 to 270 V_{ac}, V_B can exceed 1000 V_{dc} at high line and light load if L_F operates in CCM. The voltage V_B can be substantially reduced by employing the variable-switching-frequency (VSF) control as described in [9]. However, even with a wide range of switching frequency, V_B cannot be kept below the desirable 450 V_{dc} (typically used in conventional ICS's). Voltage V_B can be kept below 450 V_{dc} only if L_F is designed to operate in DCM. As explained in [6], in that case, V_B is independent of the load current, but depends only on the L_B/L_F ratio. However, for low-voltage high-current applications, the DCM operation of L_F is not desirable because it results in much higher stresses in semiconductor components compared to the CCM operation. As a result, the approach proposed in [3] is not practical for applications with the universal line-voltage range.

Voltage V_B can be further reduced by the addition of a second primary winding N_1 in series with diode D_1 as shown with the dashed line in Fig. 1 [8]. With winding N_1, when switch SW is closed, the induced voltage across N_1 is in opposition to rectified input voltage $v_{\text{in}}^{\text{rec}}$. As a result, to keep the same volt-second product across L_B, a larger duty cycle is necessary. With a larger duty cycle and L_F operating in CCM, voltage V_B will be reduced. In addition, through the magnetic coupling of windings N_1 and N_S, part of the input energy is directly transferred to the output.

In this paper, a new S^4ICS technique, which combines the boost-like ICS with a CCM dc/dc output stage, is described. The boost inductor can operate in both DCM and CCM. Due to the ability to keep a relatively low voltage on the energy-storage capacitor ($V_B < 450$ V_{dc}), this technique is suitable for the universal line-voltage applications. The voltage V_B is kept within the desirable range by the addition of two transformer windings, as shown in Fig. 2. By connecting the windings so that the voltages across them are in opposition to the input voltage when they conduct the boost-inductor current, the volt-second balance of the boost-inductor core is achieved at a substantially lower voltage V_B compared to the other known approaches. In addition, for the forward and flyback converter-type S^4ICS's, a direct transfer of a part of the input energy is achieved by the winding, which appears in series with the boost inductor during the on and off time, respectively.

Although in the next section the new ICS technique is described for the forward-converter implementation, this technique can be applied to any other single-ended, single-switch, isolated, and single- or multiple-output topology, such as the flyback, Ćuk, sepic, zeta, and other converters. Furthermore, the concept described in this paper can be extended to hard- and soft-switched multiswitch converters, such as two-switch forward and flyback converters, as well as the bridge-type topologies.

II. Principle of Operation

To simplify the analysis, it is assumed that all semiconductor components are ideal. According to this assumption, the primary switch and the rectifiers do not have parasitic capacitances and represent ideal short and open circuits in their on and off states, respectively. Also, it is further assumed that the power transformer does not have the leakage inductances because of the ideal coupling, but possesses a finite magnetizing inductance. Finally, in the following analysis, the input voltage of the converter is considered constant during a switching cycle because the switching frequency is much higher than the line frequency.

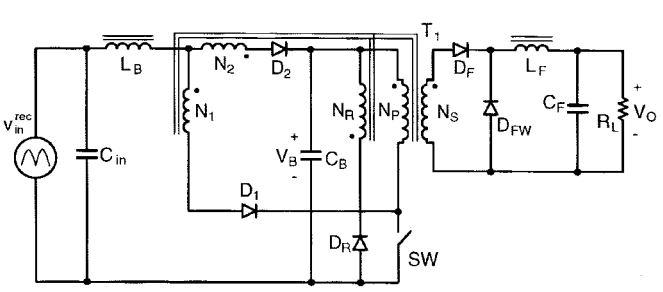


Fig. 2. Proposed S^4ICS forward converter.

A. DCM Operation of Boost Inductor

To further simplify the explanation of the circuit operation, it is assumed that the inductance of ICS inductor L_B in Fig. 2 is small so that L_B operates in DCM and that the inductance of the output-filter inductor L_F is large enough so that L_F operates in CCM. To facilitate the analysis of operation, Figs. 3 and 4 show the topological stages of the converter during a switching cycle and its key waveforms, respectively.

During the on time $[T_0 - T_1]$, switch current i_{SW} is given by the sum of ICS inductor current i_{LB}, primary-winding current i_P, and magnetizing current i_M. To help visualize the components of switch current i_{SW}, Fig. 4 uses different hatching patterns for each component. From Fig. 3(a) and Ampere's law, the currents flowing in the transformer are related as

$$N_P i_P + N_1 i_{LB} - N_S i_S = 0. \tag{1}$$

Therefore, secondary current i_S during on-time can be expressed as

$$i_S = \frac{N_P}{N_S}\, i_P + \frac{N_1}{N_S}\, i_{LB}. \tag{2}$$

It can be seen that the secondary current, which during on time supplies output energy, is composed of two components which obtain energy from different sources. The energy transferred to the secondary, which is associated with primary current i_P, is obtained from the discharging energy-storage capacitor C_B, while the energy associated with ICS inductor current i_{LB} is drawn directly from the input line. The hatched areas in the i_{LF} waveform in Fig. 4 indicate the two current components.

When primary switch SW is turned off at $t = T_1$, current i_{LB}, which was flowing through switch SW, is diverted to energy-storage capacitor C_B, as indicated in Fig. 3(b). The

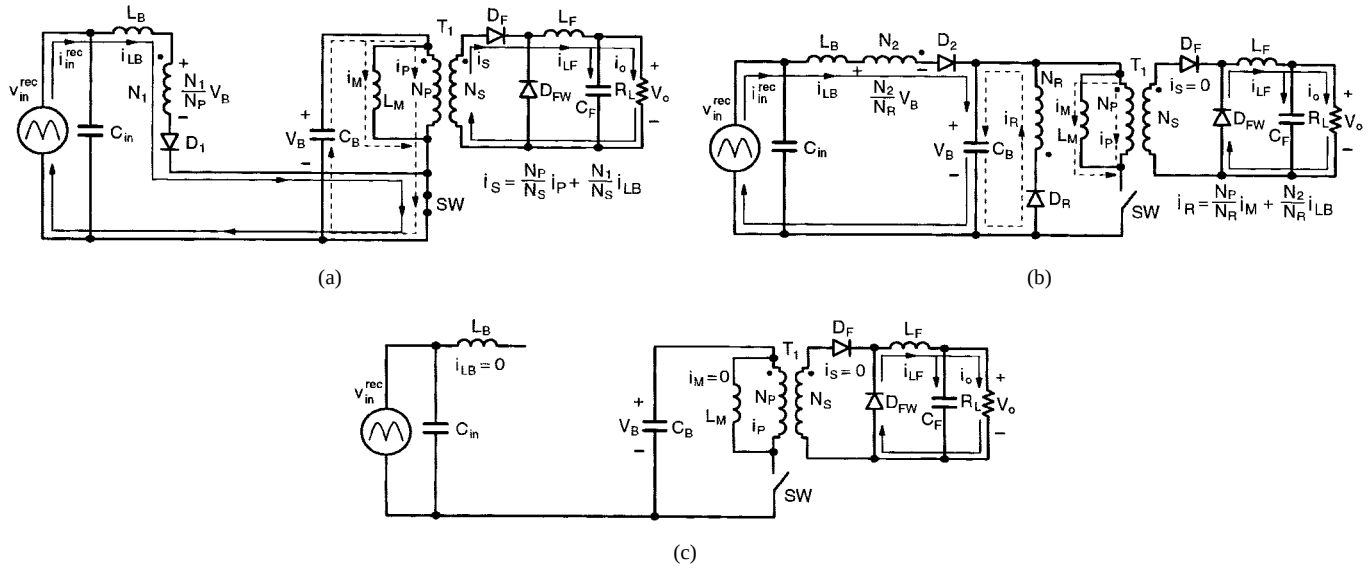


Fig. 3. Topological stages of S^{4}ICS forward converter with L_B in DCM.

downslope of i_{LB} is given by

$$\frac{di_{LB}}{dt} = \frac{v_{\text{in}}^{\text{rec}} - \left(1 + \dfrac{N_2}{N_R}\right) \cdot V_B}{L_B}. \tag{3}$$

Since during off time i_{LB} needs to decrease to zero to completely reset the L_B core, the voltage applied across L_B must be negative, i.e.,

$$\left(1 + \frac{N_2}{N_R}\right) \cdot V_B > v_{\text{in}}^{\text{rec}}. \tag{4}$$

It can be seen that with winding N_2, the required reset voltage for L_B can be obtained with a smaller V_B because of induced voltage $(N_2/N_R)\, V_B$ across winding N_2.

The reset of the transformer core is done by reset winding N_R. The reset winding carries also reflected input current i_{LB} because of the magnetic coupling between windings N_2 and N_R. According to Ampere's law, reset winding current is given by

$$i_R = \frac{N_P}{N_R}\, i_M + \frac{N_2}{N_R}\, i_{LB}. \tag{5}$$

As can be seen from Fig. 3(b), during the off time, energy stored in L_B is discharged to C_B through two paths. One path is the direct path through rectifier D_2, whereas the other path is the indirect path through the reset winding. The ratio of the indirectly and directly discharged energy is determined by turns ratio N_2/N_R. In Fig. 4, the energy stored in L_B completely discharges at $t = T_2$.

At $t = T_3$, the flux in the core of the transformer is also reset, therefore, the voltage across the transformer collapses to zero, as indicated in Fig. 3(c). The topological stage in Fig. 3(c) lasts until the initiation of the next switching cycle.

To ensure a proper operation of the circuit, the number of turns of windings N_1 and N_2 must be selected so that rectifier D_2 is off during the time switch SW is closed. From Fig. 3, this condition requires that

$$\frac{N_1}{N_P}\, V_B + \frac{N_2}{N_P}\, V_B < V_B, \qquad \text{or} \quad \frac{N_1}{N_P} + \frac{N_2}{N_P} < 1. \tag{6}$$

To maximize the direct energy transfer, it is desirable to select ratio N_1/N_P as large as possible. However, a larger ratio causes larger input-current harmonic distortions, as illustrated in Fig. 5. Namely, i_{LB} current and therefore the input current cannot flow until the line voltage exceeds the N_1-winding voltage $(N_1/N_P)V_B$. Therefore, by increasing N_1/N_P, the zero-crossing distortions are increased due to a larger dead angle. The dead angle θ can be calculated from

$$\theta = a\sin\left(\frac{N_1}{N_P} \cdot \frac{V_B}{\sqrt{2}V_{\text{in}}}\right) \tag{7}$$

where V_{in} is the rms input voltage. The relationship between θ and total harmonic distortion (THD) is discussed in [10]. In addition to these crossover harmonic distortions, the input current contains harmonic distortions caused by the finite downslope of i_{LB}, as explained and quantified in [11]. Generally, these distortions decrease as the i_{LB} downslope increases.

The duty cycle of the switch is determined by the fast (wide-bandwidth) output-voltage control loop. If the voltage ripple on C_B is small, the duty cycle is essentially constant during a half of a line cycle

$$D = \frac{N_P}{N_S} \cdot \frac{V_o}{V_B}. \tag{8}$$

To use the above equations, energy-storage-capacitor voltage V_B needs to be known. By applying the input–output power balance principle to the circuit in Fig. 2, this voltage

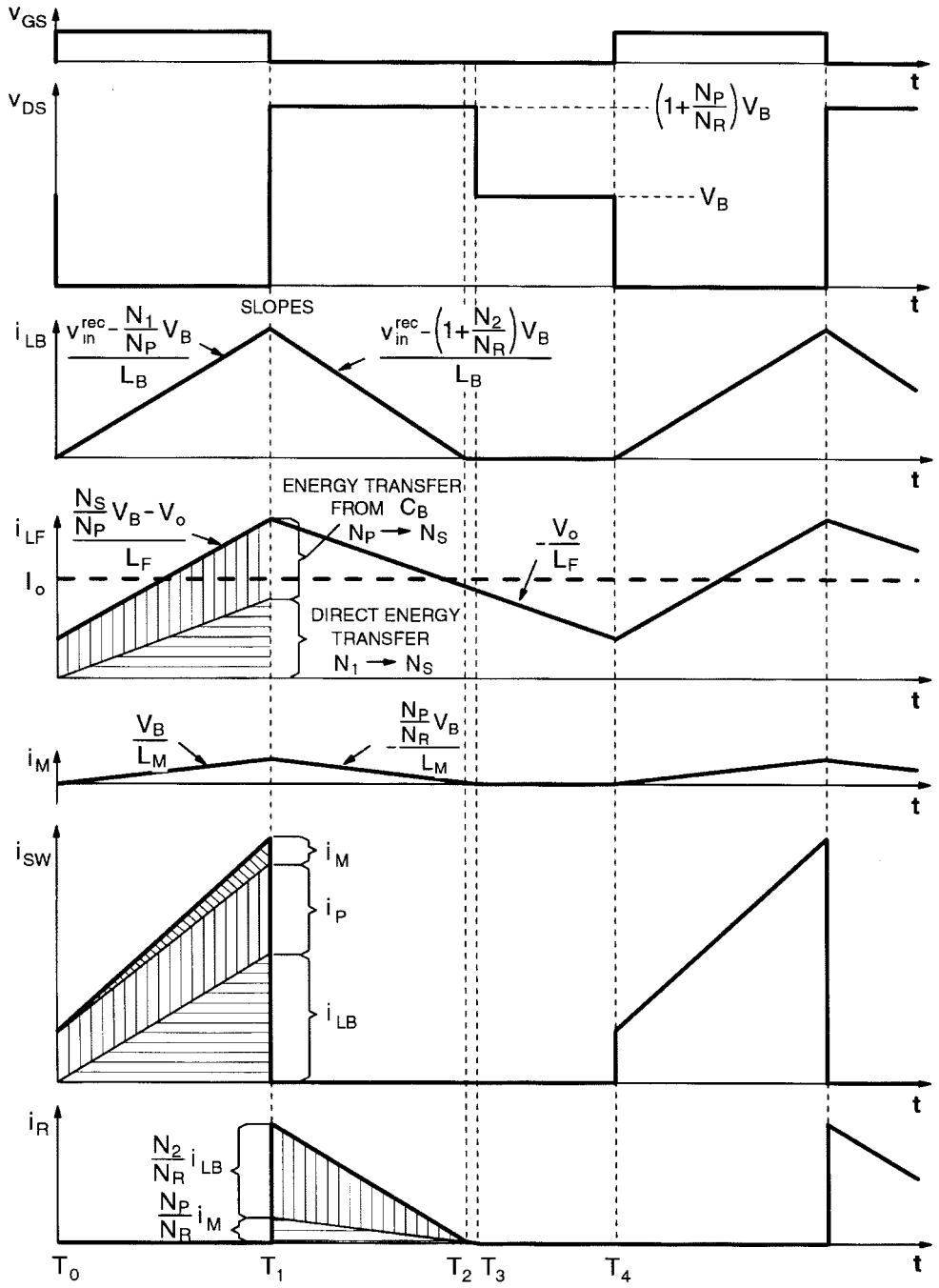


Fig. 4. Key waveforms of S^{4}ICS forward converter with L_B in DCM.

can be expressed in an implicit form as

$$\frac{\eta}{\pi}\cdot\left(\frac{\frac{N_P}{N_S}\sqrt{2}V_{\text{in}}V_o}{V_B}\right)^2\cdot\frac{1+\frac{N_2}{N_R}-\frac{N_1}{N_P}}{V_o\cdot I_o}\cdot\frac{1}{L_B f_S}\cdot\int_\theta^{\pi/2}\frac{\sin^2(x)-\frac{N_1}{N_P}\cdot\frac{V_B}{\sqrt{2}V_{\text{in}}}\sin(x)}{1+\frac{N_2}{N_R}-\frac{\sqrt{2}V_{\text{in}}}{V_B}\sin(x)}dx=1 \quad (9)$$

where η is the assumed efficiency of the converter and I_o is the output (load) current.

As can be concluded by inspecting (9), V_B increases as the line voltage increases and/or the output current decreases. Therefore, V_B is the highest at high line and light load. Depending on the minimum load specifications, V_B might exceed the desired voltage level ($<$450 V_{dc}) even with the maximum possible induced voltage on winding N_2. In that case, the desired V_B can be achieved either by VSF control or by operating L_F in DCM at light loads. Namely, from (9), it can be seen that V_B is inversely proportional to f_S. Therefore,

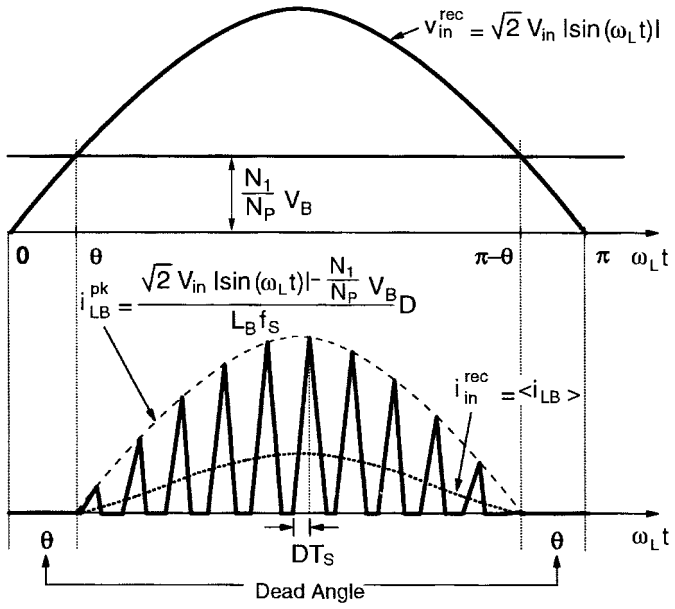


Fig. 5. Line voltage and current waveforms of S^{4}ICS forward converter with L_B operating in DCM.

by increasing the switching frequency as the load decreases and/or line voltage increases, voltage V_B can be limited to the desired level. One implementation of the VSF control is described in [9]. At light loads, V_B can also be limited by resorting to DCM operation of L_F. As described in [6], when both L_B and L_F operate in DCM, V_B is independent of the output current, but only depends on the L_B/L_F ratio.

B. CCM Operation of Boost Inductor

In the preceding explanation, it was arbitrarily assumed, for the sake of description simplification, that the inductance of boost inductor L_B is small so that L_B always operates in DCM. However, the proposed ICS circuit shown in Fig. 2 can also properly operate for larger values of L_B which result in the CCM operation of L_B. To facilitate the explanation of the circuit operation with L_B operating in CCM, Figs. 6 and 7 show the topological stages and the key waveforms, respectively. It should be noted that while the leakage inductances of the transformer have no significant effect on the operation of the circuit with L_B operating in DCM and, consequently, were neglected in the preceding explanation, the leakage inductances of auxiliary windings N_1 and N_2 play a major role in the operation of the circuit with L_B operating in CCM and cannot be neglected. As a result, in Fig. 6, the leakage inductances of windings N_1 and N_2 are shown as leakage inductance L_{lk1} in series with winding N_1 and leakage inductance L_{lk2} in series with winding N_2.

Due to the CCM operation of L_B, at the moment immediately before primary switch SW is turned on, the entire boost-inductor current i_{LB} is flowing through winding N_2 and rectifier D_2 into bulk capacitor C_B. After switch SW is closed at $t = T_0$, current i_{LB} starts commutating from winding N_2 to winding N_1. According to Fig. 6(a), the i_{LB} commutation is governed by

$$V_B - \frac{N_2}{N_P} V_B + L_{ek2} \frac{di_2}{dt} - L_{ek1} \frac{di_1}{dt} - \frac{N_1}{N_P} V_B = 0. \quad (10)$$

Since during the commutation interval $[T_0 - T_1]$ boost-inductor current i_{LB} does not change significantly due to a relatively large inductance of boost inductor L_B required for the CCM operation, it can be assumed that

$$i_{LB} = i_1 + i_2 = \text{const.}, \quad \text{i.e.} \quad \frac{di_1}{dt} = -\frac{di_2}{dt}. \quad (11)$$

From (10) and (11), the slopes of currents i_1 and i_2 during commutation interval $[T_0 - T_1]$ are approximately given by

$$\frac{di_1}{dt} = -\frac{di_2}{dt} = \frac{\left(1 - \frac{N_1 + N_2}{N_P}\right) V_B}{L_{ek1} + L_{ek2}}. \quad (12)$$

Also, it should be noted that during $[T_0 - T_1]$, the voltage of the common node of the boost inductor, winding N_1, and winding N_2 [node Y in Fig. 6(a)] is given by

$$V_Y^{\text{ON}} = \frac{\left(1 - \frac{N_2}{N_P}\right) L_{ek1} + \frac{N_1}{N_P} L_{ek2}}{L_{ek1} + L_{ek2}} V_B \quad (13)$$

as indicated in Fig. 7(b).

After the commutation of i_{LB} is completed at $t = T_1$, the entire i_{LB} flows through winding N_1 as shown in Fig. 6(b). During $[T_1 - T_2]$ interval, boost-inductor current i_{LB} is given by

$$\frac{di_{LB}}{dt} = \frac{di_1}{dt} = \frac{v_{\text{in}}^{\text{rec}} - \frac{N_1}{N_P} V_B}{L_B + L_{ek1}} \approx \frac{v_{\text{in}}^{\text{rec}} - \frac{N_1}{N_P} V_B}{L_B} \quad (14)$$

where the approximation assumes $L_B \gg L_{lk1}$. From (14), it can be seen that if the instantaneous rectified-line voltage $v_{\text{in}}^{\text{rec}}$ is smaller than the dc voltage across winding N_1, i.e., $v_{\text{in}}^{\text{rec}} < (N_1/N_P)\, V_B$, no i_{LB} can build up in inductor L_B. As a result, the line current (average of i_{LB}) contains zero-crossing distortions caused by dead angle θ [which can be calculated from (7)] of current i_{LB}. On the other hand, for $v_{\text{in}}^{\text{rec}} > (N_1/N_P)\, V_B$, i_{LB} can flow after commutation interval $[T_0 - T_1]$ is completed, as shown in Fig. 7(c). However, during the time intervals for which $v_{\text{in}}^{\text{rec}}$ is only slightly higher than $(N_1/N_P)\, V_B$, i_{LB} is discontinuous. Therefore, during one half of a line period, the boost inductor operates in both DCM and CCM, as illustrated in Fig. 8.

From Fig. 6(a) and (b) and Ampere's law, it follows that secondary current i_S is given by

$$i_S = \frac{N_P}{N_S} i_P + \frac{N_1}{N_S} i_1 - \frac{N_2}{N_S} i_2 \quad (15)$$

during commutation interval $[T_0 - T_1]$ and

$$i_S = \frac{N_P}{N_S} i_P + \frac{N_1}{N_S} i_{LB} \quad (16)$$

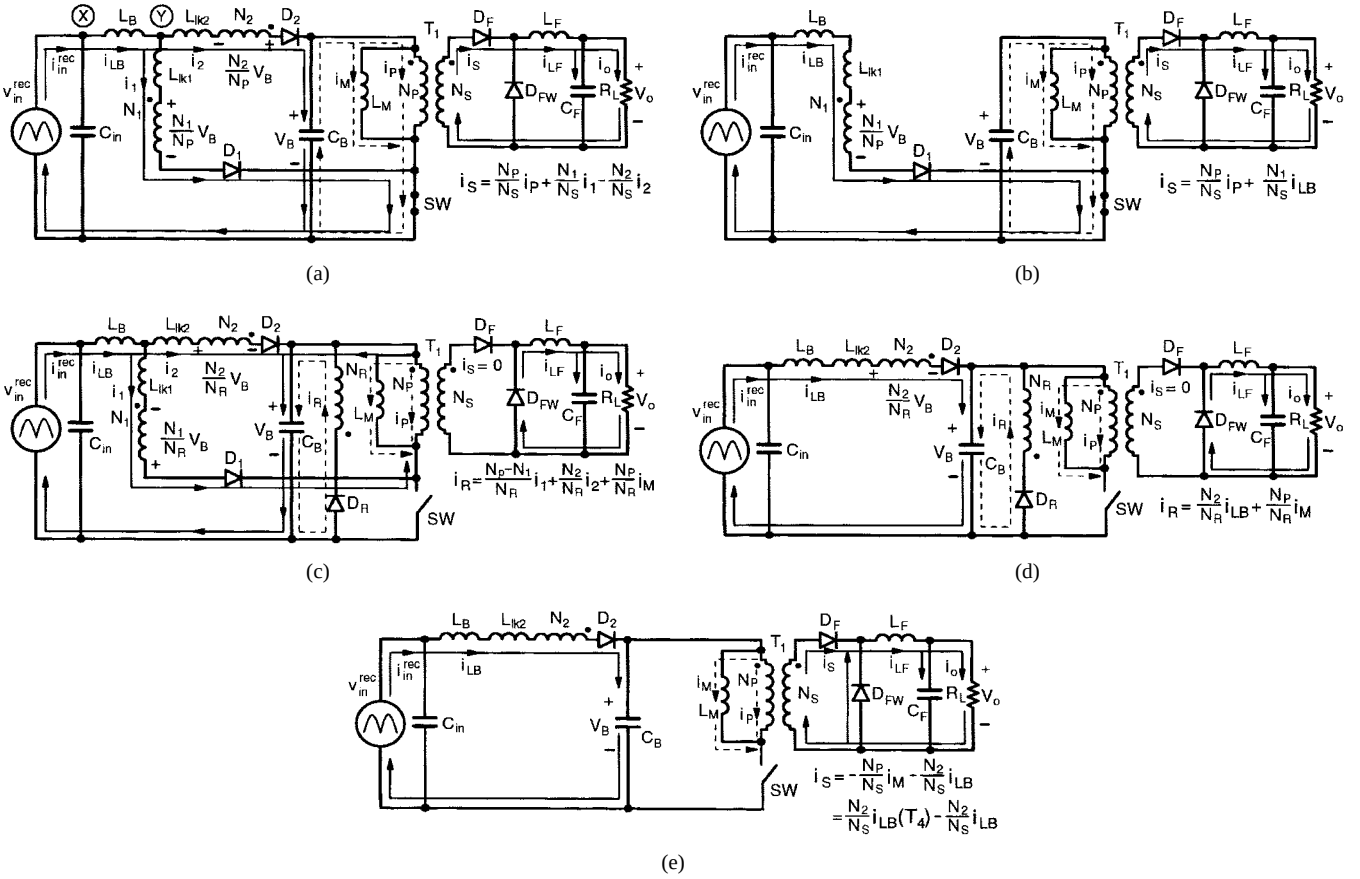


Fig. 6. Topological stages of S^{4}ICS forward converter with L_B in CCM.

during $[T_1 - T_2]$ interval. During turn-on interval $[T_0 - T_2]$, the output energy is supplied from bulk capacitor C_B by current i_P and directly from the source by current i_{LB}, as indicated in Fig. 7(d) by hatched areas.

After switch SW is turned off at $t = T_2$ (Fig. 7), boost-inductor current i_{LB} begins commutating from winding N_1 to winding N_2. At the same time, the transformer core starts the reset phase by transferring magnetizing inductance i_M to the reset winding N_R, thus discharging the energy stored in the core into bulk capacitor C_B.

From Fig. 6(c), using (11), the slopes of currents i_1 and i_2 during commutation interval $[T_2 - T_3]$ can be calculated as

$$\frac{di_1}{dt} = -\frac{di_2}{dt} = -\frac{\left(1 - \dfrac{N_1 + N_2}{N_R}\right) V_B}{L_{ek1} + L_{ek2}}. \tag{17}$$

From Fig. 6(c) and Ampere's law, reset-winding current i_R during $[T_2 - T_3]$ is given by

$$i_R = \frac{N_P - N_1}{N_R}\, i_1 + \frac{N_2}{N_R}\, i_2 + \frac{N_P}{N_R}\, i_M. \tag{18}$$

The downslope of i_R during $[T_2 - T_3]$ is

$$\frac{di_R}{dt} = -\left[\frac{(N_P - N_1 - N_2)(N_R - N_1 - N_2)}{N_R^2 (L_{ek1} + L_{ek2})}\, V_B + \left(\frac{N_P}{N_R}\right)^2 \frac{V_B}{L_M}\right]. \tag{19}$$

Since according to (6), for proper operation of the circuit $N_P > N_1 + N_2$ and for a typical design $N_R = N_P$, the di_R/dt rate is indeed negative, as shown in Fig. 7(g).

The voltage of node Y during commutation interval $[T_2 - T_3]$, V_Y^{OFF} can be calculated from the circuit in Fig. 6(c), with the help of (17), as

$$V_Y^{\mathrm{OFF}} = \frac{\left(1 + \dfrac{N_2}{N_R}\right) L_{ek1} + \left(2 - \dfrac{N_1}{N_R}\right) L_{ek2}}{L_{ek1} + L_{ek2}}\, V_B. \tag{20}$$

After the commutation interval is completed at $t = T_3$, the entire boost-inductor current i_{LB} flows through auxiliary winding N_2 into bulk capacitor C_B, as shown in Fig. 6(d). As the transformer continues to reset after $t = T_3$, reset current i_R continues to decrease with the slope given by

$$\frac{di_R}{dt} = -\left[\frac{N_2}{N_R}\, \frac{\left(1 + \dfrac{N_2}{N_R}\right) V_B - v_{\mathrm{in}}^{\mathrm{rec}}}{L_B} + \left(\frac{N_P}{N_R}\right)^2 \frac{V_B}{L_M}\right] \tag{21}$$

where the approximation $L_B \gg L_{lk2}$ is used. Equation (21) is obtained from (18) by setting $i_1 = 0$ and $i_2 = i_{LB}$ and by using the expression for di_{LB}/dt during $[T_3 - T_4]$ interval given in (23). Since the slope of i_{LB} in (23) is much smaller than the slope of i_1 and i_2 in (17) due to a relatively large value of L_B, the di_R/dt rate during $[T_3 - T_4]$ is much smaller

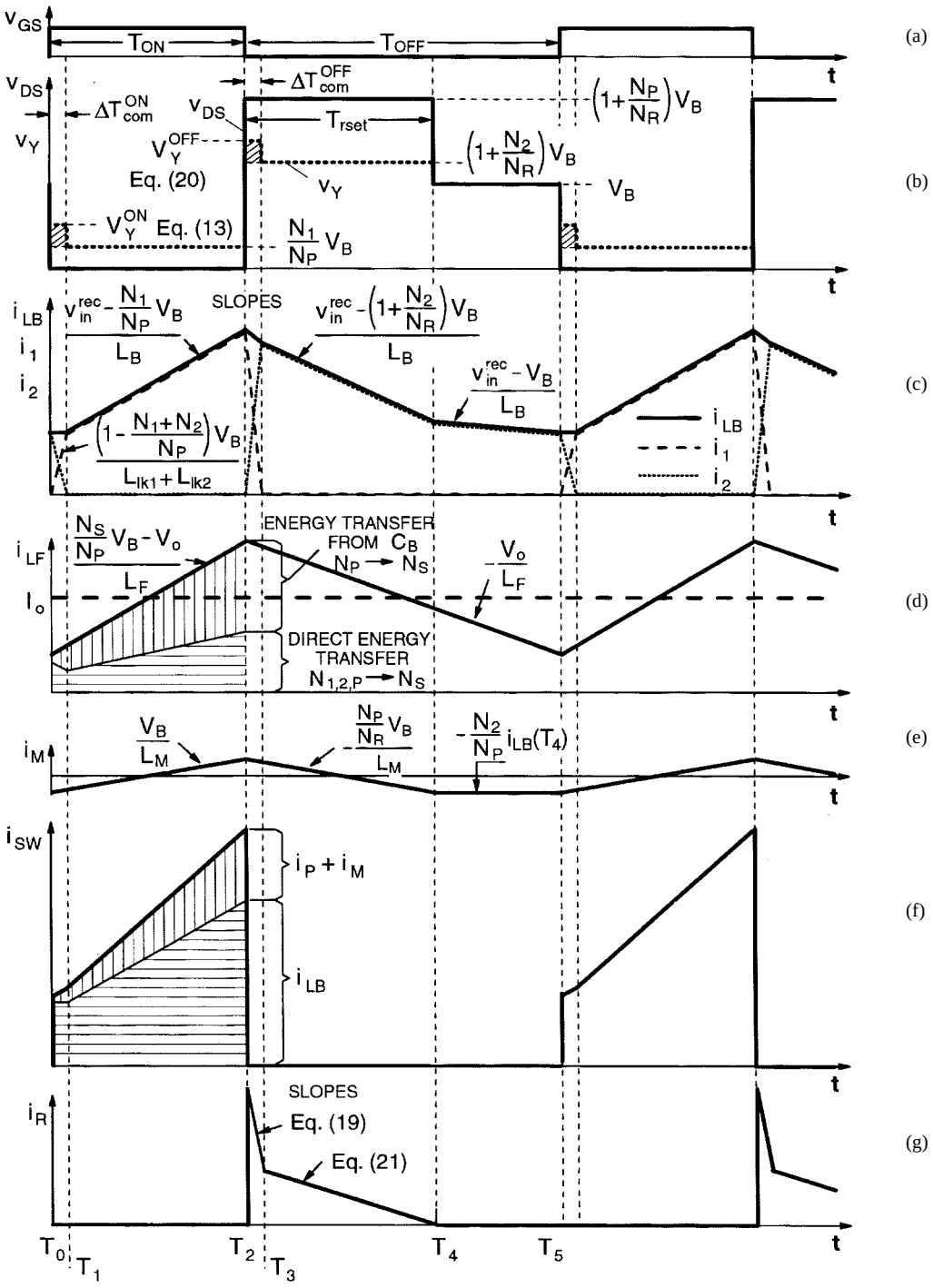


Fig. 7. Key waveforms of S^{4}ICS forward converter with L_B in CCM.

than that during commutation interval $[T_2 - T_3]$, as indicated in Fig. 7(g).

The transformer reset is completed at $t = T_4$ when reset current i_R becomes zero. It should be noted that when i_R reaches zero at $t = T_4$, magnetizing current i_M is negative and equal to

$$i_M(t = T_4) = -\frac{N_2}{N_P}\, i_{LB}(t = T_4) \tag{22}$$

as shown in Fig. 7(e).

During $[T_3 - T_4]$ interval, the downslope of boost-inductor current i_{LB} is given by

$$\frac{di_{LB}}{dt} = -\frac{\left(1 + \dfrac{N_2}{N_R}\right) V_B - v_{\text{in}}^{\text{rec}}}{L_B + L_{\epsilon k2}} \approx -\frac{\left(1 + \dfrac{N_2}{N_R}\right) V_B - v_{\text{in}}^{\text{rec}}}{L_B}. \tag{23}$$

After the reset of the transformer core is completed at

$t = T_4$, the voltages across all transformer windings become zero. As a result, the voltage across switch SW becomes equal to voltage V_B, as shown in Fig. 7(b). At the same time, a part of magnetizing current i_M, which is negative at $t = T_4$, starts flowing through secondary winding N_S and rectifier D_F. Since the voltage across the transformer windings is zero, i_M stays constant until the next switching cycle is initiated at $t = T_5$. From Fig. 6(e), applying Ampere's law for the final time, secondary current i_S during $[T_4 - T_5]$ interval is given by

$$i_S = -\frac{N_P}{N_S}\, i_M - \frac{N_2}{N_S}\, i_{LB} = \frac{N_2}{N_S}\, i_{LB}(t = T_4) - \frac{N_2}{N_S}\, i_{LB}. \tag{24}$$

During $[T_4 - T_5]$, i_{LB} continues to decrease with a smaller downslope given by

$$\frac{di_{LB}}{dt} = -\frac{V_B - v_{\text{in}}^{\text{rec}}}{L_B + L_{ek2}} \approx -\frac{V_B - v_{\text{in}}^{\text{rec}}}{L_B} \tag{25}$$

as shown in Fig. 7(c).

From the preceding analysis of the proposed S^{4}ICS circuit operating with L_B in CCM, it can be seen that the leakage inductances L_{lk1} and L_{lk2} of auxiliary windings N_1 and N_2 play significant roles only during commutation intervals $[T_0 - T_1]$ and $[T_2 - T_3]$. Namely, assuming negligible leakage inductances, i.e., $L_{lk1} = L_{lk2} = 0$ in Fig. 6, the volt-second-product balance during the on and off times is given by

$$\begin{aligned}\Lambda_{\text{ON}} &= \left(v_{\text{in}}^{\text{rec}} - \frac{N_1}{N_P}\, V_B\right) T_{\text{ON}} = \Lambda_{\text{OFF}} \\ &= \left(V_B + \frac{N_2}{N_R}\, V_B - v_{\text{in}}^{\text{rec}}\right) T_{\text{rset}} \\ &\quad + (V_B - v_{\text{in}}^{\text{rec}})(T_{\text{OFF}} - T_{\text{rset}})\end{aligned} \tag{26}$$

where Λ_{ON} and Λ_{OFF} are the volt-second products during the on and off times, respectively, and T_{rset} is the reset time of the transformer core, indicated in Fig. 7(b).

Since for the fast-output-voltage control the duty cycle of switch SW is constant over a half of a line, T_{ON} and T_{OFF} are also constant. Therefore, as rectified-line voltage $v_{\text{in}}^{\text{rec}}$ increases toward its peak, Λ_{ON} increases while Λ_{OFF} decreases. As a result, a volt-second-product balance of the L_B core cannot be maintained. The resulting large imbalance eventually leads to the saturation of the L_B core. To maintain the required volt-second-product balance, it is necessary to proportionally reduce Λ_{ON} and/or proportionally increase Λ_{OFF} as $v_{\text{in}}^{\text{rec}}$ increases. The desired reduction of Λ_{ON} and increase of Λ_{OFF} in the proposed circuit in Fig. 2 are brought about by leakage inductances L_{lk1} and L_{lk2}. Namely, the volt-second-product balance, which takes into account the leakage-inductance effect, is

$$\begin{aligned}&\left(v_{\text{in}}^{\text{vec}} - \frac{N_1}{N_P}\, V_B\right) T_{\text{ON}} - \left(V_Y^{\text{ON}} - \frac{N_1}{N_P}\, V_B\right) \Delta T_{\text{com}}^{\text{ON}} \\ &\quad = \left(V_B + \frac{N_2}{N_R}\, V_B - v_{\text{in}}^{\text{vec}}\right) T_{\text{rset}} \\ &\qquad + (V_B - v_{\text{in}}^{\text{rec}})(T_{\text{OFF}} - T_{\text{rset}}) \\ &\qquad + \left[V_Y^{\text{OFF}} - \left(1 + \frac{N_2}{N_R}\right) V_B\right] \Delta T_{\text{comm}}^{\text{OFF}}\end{aligned} \tag{27}$$

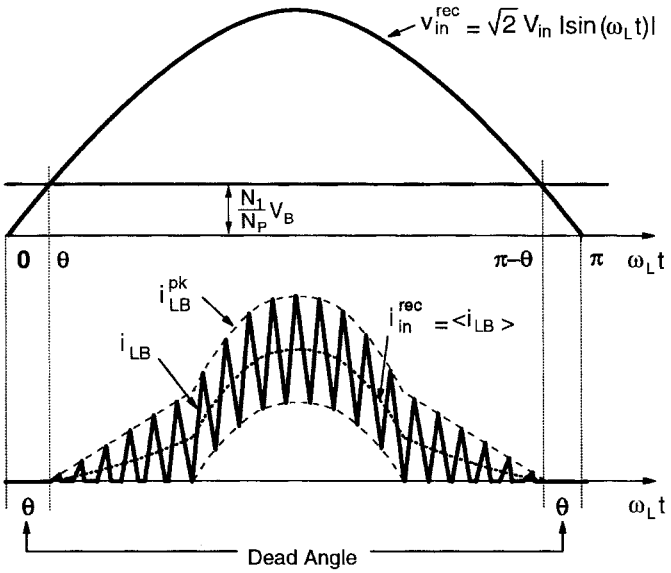


Fig. 8. Line voltage and current waveforms of S^{4}ICS forward converter with L_B operating in CCM.

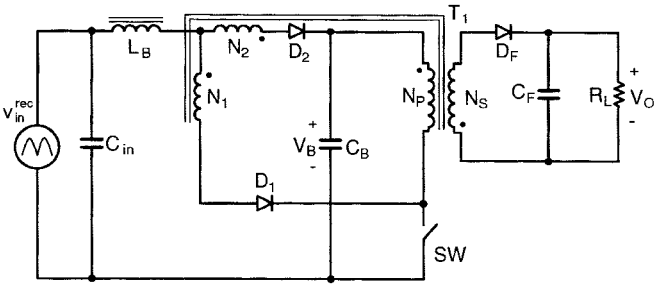


Fig. 9. Flyback implementation of S^{4}ICS.

where V_Y^{ON} and V_Y^{OFF} are the voltages of node Y in Fig. 6(a) given by (13) and (20), respectively, while $\Delta T_{\text{com}}^{\text{ON}}$ and $\Delta T_{\text{com}}^{\text{OFF}}$ are the commutation intervals $[T_0 - T_1]$ and $[T_2 - T_3]$, respectively, as indicated in Fig. 7(b). As can be seen comparing (26) and (27), leakage inductances L_{lk1} and L_{lk2} decrease Λ_{ON} for

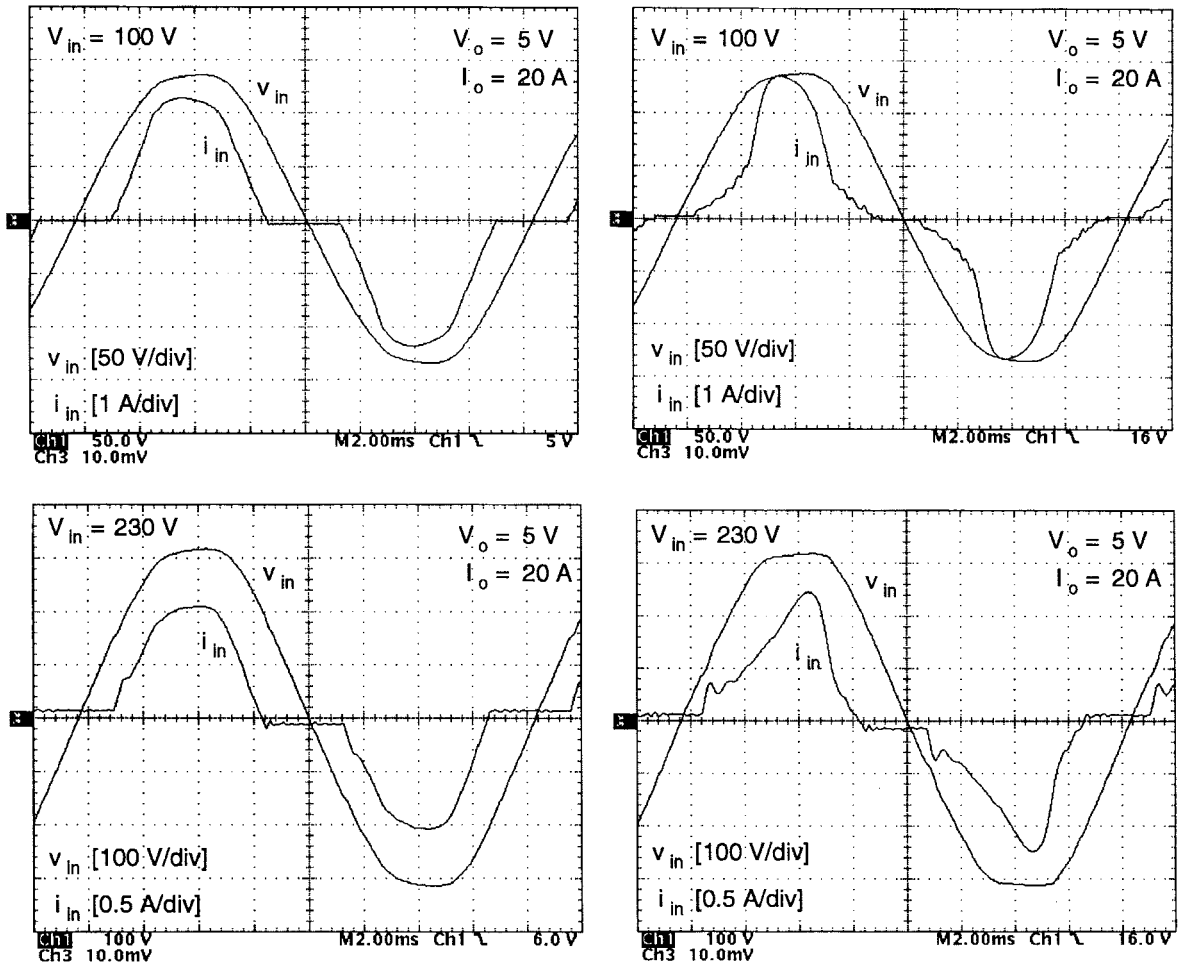
$$\Delta\Lambda_{\text{ON}} = -\left(V_Y^{\text{ON}} - \frac{N_1}{N_P}\, V_B\right) \Delta T_{\text{com}}^{\text{ON}} \tag{28}$$

and increase Λ_{OFF} for

$$\Delta\Lambda_{\text{OFF}} = \left[V_Y^{\text{OFF}} - \left(1 + \frac{N_2}{N_R}\right) V_B\right] \Delta T_{\text{com}}^{\text{OFF}} \tag{29}$$

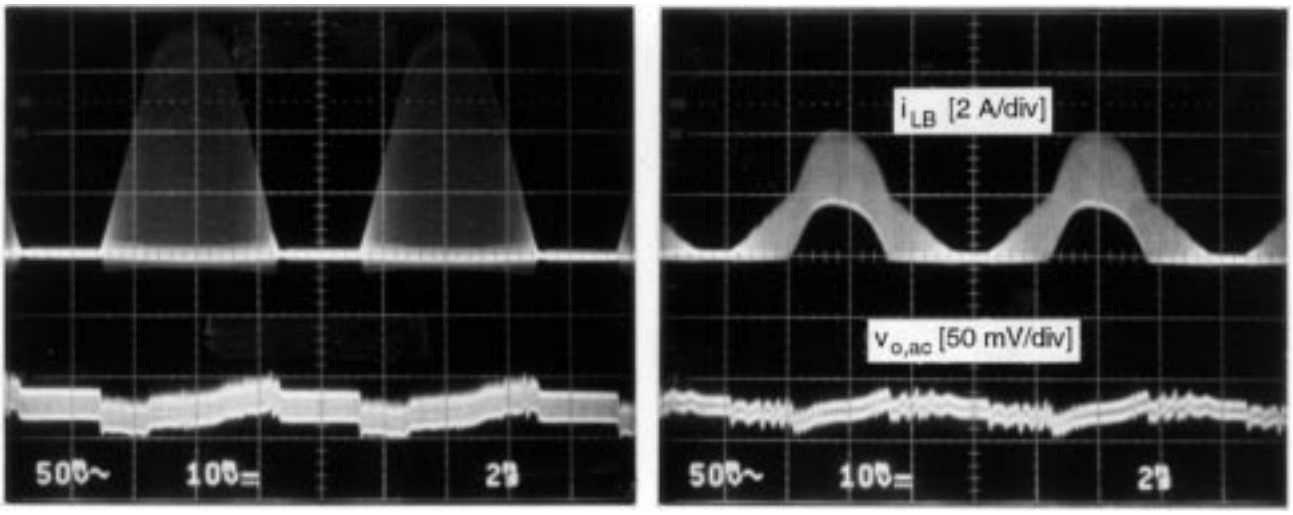
where $\Delta\Lambda_{\text{ON}}$ and $\Delta\Lambda_{\text{OFF}}$ are the hatched areas in Fig. 7(b).

Because according to (12) and (17) the slopes of currents i_1 and i_2 are constant, commutation times $\Delta T_{\text{com}}^{\text{ON}}$ and $\Delta T_{\text{com}}^{\text{OFF}}$ are proportional to the instantaneous values of i_{LB} at the moment switch SW is closed and open, respectively. As a result, $|\Delta\Lambda_{\text{ON}}|$ and $|\Delta\Lambda_{\text{OFF}}|$ increase as the line voltage increases toward its peak because i_{LB} increases, as illustrated in Fig. 8. Therefore, with properly selected leakage inductances L_{lk1} and L_{lk2}, the volt-second-product balance on the L_B core can be maintained during a half of a line period even with a constant duty cycle of switch SW.



(a) (b)

Fig. 10. Line voltage and current waveforms of (a) DCM and (b) CCM implementation of experimental converter.



(a) (b)

Fig. 11. Boost-inductor-current and output-voltage-ripple waveforms of (a) DCM and (b) CCM implementation of experimental converter ($V_{\rm in} = 100$ V, $V_o = 5$ V, $I_o = 20$ A, i_{LB} [2 A/div], and $v_{o,\rm ac}$ [50 mV/div]).

Finally, the voltage across switch SW during off time is

$$V_{\rm SW} = \left(1 + \frac{N_P}{N_R}\right) \cdot V_B = 2 \cdot V_B \tag{30}$$

where $N_R = N_P$ is assumed. The maximum stress occurs at high line when V_B is maximum. Therefore, for universal line-voltage applications, the required rating of the switch is in the 800–900-V range.

TABLE I
MEASURED PERFORMANCE COMPARISONS BETWEEN DCM AND CCM IMPLEMENTATIONS ($V_o = 5$ V AND $I_o = 20$ A)

	DCM				CCM			
V_{in} [V]	*PF*	*THD*	V_B [V]	η [%]	*PF*	*THD*	V_B [V]	η [%]
90	0.935	34.9	130	75.4	0.860	54.2	120	76.9
100	0.936	34.5	145	75.9	0.858	55.1	135	77.9
120	0.934	36.0	175	76.6	0.854	56.5	163	78.7
230	0.923	37.5	335	75.4	0.857	56.5	314	78.3
265	0.917	37.6	385	74.3	0.857	55.0	361	77.7

C. Other Implementations

The concept explained in this paper can be extended to any other single- or multiple-switch topology. Fig. 9 shows the implementation with the flyback topology. As can be seen from Fig. 9, this implementation does not require a separate reset winding because the transformer reset is done by the output voltage through the secondary winding. Also, it should be noted that in the flyback implementation, a direct energy transfer from the input to the output occurs during the off time.

III. EXPERIMENTAL RESULTS

To verify the operation and performance of the proposed S^{4}ICS technique for both the DCM and CCM operation of L_B, a 100-W/5-V universal line-voltage range (90–265 V_{ac}), forward converter S^{4}ICS shown in Fig. 2 was built. The following components were used for the implementation of the circuit with L_B operating in the DCM mode: C_{in}—1 μF; D_1, D_2, and D_R—BYM26E; D_F and D_{FW}—IR 40CPQ045; SW—IXTK21N100; C_B—330 μF/450 V; L_F—2 μH; C_F—3 $\times$ 2200 μF; L_B—58 μH; and T_1—EER35 core with $N_P = N_R = 48$ turns, $N_1 = 20$ turns, $N_2 = 26$ turns, $N_S = 5$ turns, and leakage inductance $L_{lk1} + L_{lk2} \approx 5$ μH. For the implementation with L_B operating in CCM, except for boost inductor L_B and transformer T_1 windings, all other components were the same as for the DCM operation. In the CCM implementation, $L_B = 100$ μH and T_1 with $N_P = N_R = 48$ turns, $N_1 = 18$ turns, $N_2 = 12$ turns, $N_S = 5$ turns, and leakage inductance $L_{lk1} + L_{lk2} \approx 50$ μH were taken. The large leakage inductance between windings N_1 and N_2 in the CCM implementation is achieved by placing winding N_2 on the central leg and winding N_1 on the outer leg of the transformer core. In both implementations, the same low-cost current-mode pulse-width-modulation (PWM) integrated circuit controller (UC3845) was used to implement a fast-output-voltage feedback control. The switching frequency of both implementations was constant at 75 kHz throughout the entire line voltage and load range.

Fig. 10(a) and (b) shows the typical line voltage and current waveforms of the experimental converter for the DCM and CCM implementations, respectively, whereas, Table I summarizes the power factor (PF), THD, bulk-capacitor voltage (V_B), and efficiency measurements [including in-rush-current limiter and electromagnetic interference (EMI) filter] for the two implementations at full load ($I_o = 20$ A). As can be seen from Table I, both implementations work with a high PF and relatively low THD, while keeping V_B below 400 V_{dc}. The DCM implementation can achieve a higher PF and lower THD, while the CCM implementation operates with a lower voltage on the bulk capacitor and is more efficient. The maximum bulk-capacitor-voltage, which is obtained at high line ($V_{in} = 265$ V) and L_F operating at the DCM-CCM boundary, is equal to 405 and 390 V for the DCM and CCM implementations of L_B, respectively. Finally, Fig. 11 shows the waveforms of the boost inductor current and output voltage ripple, which is kept below 50 mV by a fast-output-voltage regulation loop.

IV. SUMMARY

A new S^{4}ICS technique, which combines the boost-like ICS with a CCM dc/dc output stage, is presented. Due to the ability to keep a relatively low voltage on the energy-storage capacitor ($V_B < 450$ V_{dc}), this technique is suitable for the universal line-voltage applications. The voltage V_B is kept within the desirable range by the addition of two transformer windings. By connecting the windings so that the voltages across them are in opposition to the input voltage when they conduct the boost-inductor current, the volt-second balance of the boost-inductor core is achieved at a substantially lower voltage V_B compared to the other known approaches.

In this technique, the boost inductor can operate in both DCM and CCM. Generally, the DCM implementation can achieve a higher PF and lower THD compared to the CCM implementation. However, the CCM implementation is more efficient and operates with a lower voltage on the energy-storage capacitor.

The proposed S^{4}ICS technique is suitable for power ranges up to 150–250 W for universal line-voltage applications and up to 250–350 W for narrow-line-voltage-range applications.

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