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Aftab M. Hussain, Nimer Wehbe, Muhammad Mustafa Hussain

Institutions: King Abdullah University of Science and Technology

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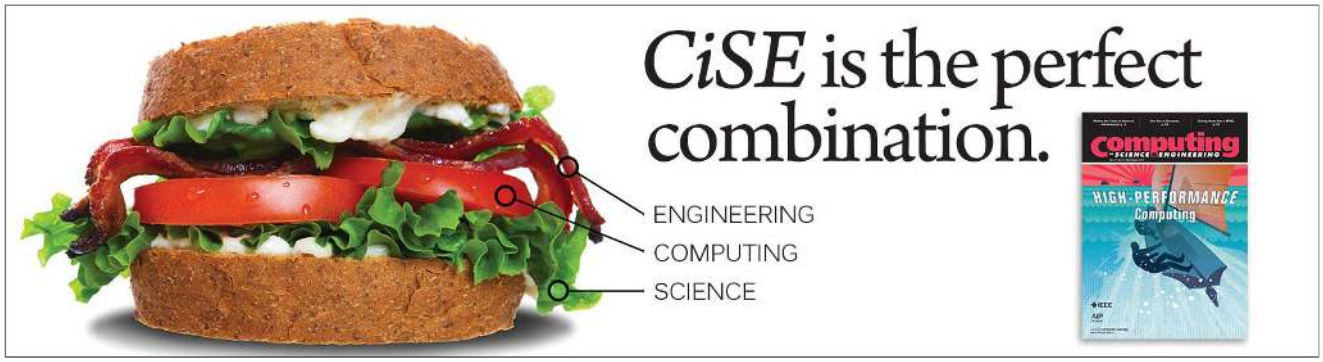

SiSn diodes: Theoretical analysis and experimental verification

Aftab M. Hussain,[1] Nimer Wehbe,[2] and Muhammad M. Hussain[1,a)]
[1]*Integrated Nanotechnology Laboratory, Computer Electrical Mathematical Science and Engineering (CEMSE) Division, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia*
[2]*Imaging and Characterization Laboratory, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia*

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We report a theoretical analysis and experimental verification of change in band gap of silicon lattice due to the incorporation of tin (Sn). We formed SiSn ultra-thin film on the top surface of a 4 in. silicon wafer using thermal diffusion of Sn. We report a reduction of 0.1 V in the average built-in potential, and a reduction of 0.2 V in the average reverse bias breakdown voltage, as measured across the substrate. These reductions indicate that the band gap of the silicon lattice has been reduced due to the incorporation of Sn, as expected from the theoretical analysis. We report the experimentally calculated band gap of SiSn to be 1.11 ± 0.09 eV. This low-cost, CMOS compatible, and scalable process offers a unique opportunity to tune the band gap of silicon for specific applications. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4929801]

Silicon-based complementary metal oxide semiconductor (CMOS) electronics constitute the major portion of all the currently used electronic devices. The exponential increase in the performance of these devices has been realized by physical scaling of the transistor dimensions. However, with the transistor dimensions already down to sub-20 nm, the end of physical scaling is in sight.[1] Further the increase in leakage current with reduction in gate dielectric thickness leads to higher static power consumption and elevated surface temperatures for the electronics. With these challenges at hand, semiconductor research has been focused on alternative channel materials, transistor architectures, and physics to advance the state-of-the-art CMOS technology toward future generation.[2–13]

Silicon (Si) and tin (Sn) belong to group IV-A of the Periodic Table, along with carbon (C), germanium (Ge), and lead (Pb). These elements crystallize into a diamond lattice and have a band gap that decreases from C (5.5 eV) up to Sn (nearly zero). The semiconducting properties of Si, Ge, and their alloy SiGe have been well studied in the last forty years.[14–18] Recently, the semiconducting and optoelectronic properties of an alloy, GeSn, have been reported.[19–25] Group IV-A semiconducting alloys are of interest particularly because their band gap can be adjusted by changing their relative concentration. In our previous work, we have shown that SiSn band gap can indeed be varied by changing the Sn concentration in silicon lattice.[26–29] It is expected from literature that Sn atoms in SiSn occupy the substitutional position in the silicon lattice.[30] This causes the band structure of the lattice to change, since there is change in the 3D potential distribution due to the incorporation of a large positively charged nucleus at a substitutional position. This change in band structure leads to change in band gap, effective mass, DOS, etc. While this is an interesting result in itself, it is important to note that the variation in band structure, and in particular, band gap, has profound impact on the performance of the semiconductor in electronic circuitry. Hence, in this work, we present the impact of the change in band gap of silicon with incorporation of tin, from a device perspective.

The most simple and fundamental electronic device is a p-n junction diode. An abrupt junction is formed when p-type and n-type semiconductors are brought together into physical and electrical contact. Since there is no current in thermal equilibrium, the net diffusion current is zero. This necessitates that there is no change in Fermi level across the junction. Figure 1 shows the formation of an abrupt, homogenous junction, using a heavily doped n-type (n++) and a lightly doped p-type (p−) semiconductor. Since the Fermi levels are conserved, the conduction and valence bands shift equivalently in opposite directions to form the p-n junction. This shift in bands is responsible for the formation of a built-in potential across the junction. This junction potential can

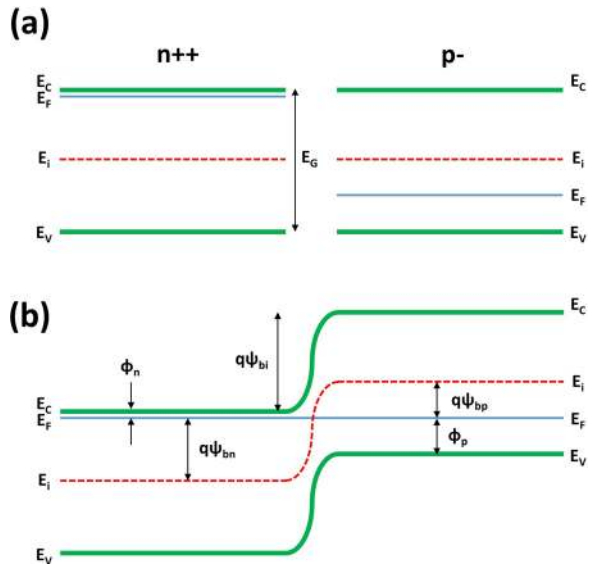

FIG. 1. Two semiconductor regions with opposite doping (a) before and (b) after formation of the abrupt, homogenous p-n junction. The Fermi level aligns after junction formation, since there is no diffusion current in steady state.

[a)]Author to whom correspondence should be addressed. Electronic mail: MuhammadMustafa.Hussain@kaust.edu.sa

be physically understood by considering the migration of some majority carriers from both sides across the junction, so that the impurity kernels are exposed and an electric field is formed opposing the said migration. In mathematical terms, the built-in potential can be obtained from the shift in conduction and valence bands of the initial samples as

$$q\psi_{bi} = q\psi_{bp} + q\psi_{bn}, \tag{1}$$

$$q\psi_{bi} = E_g - (q\varphi_n + q\varphi_p). \tag{2}$$

Now, the departure of Fermi level from the intrinsic energy level is obtained from Boltzmann's statistics for non-degenerate semiconductors as

$$\varphi_n = \frac{kT}{q}\ln\left(\frac{N_c}{N_d}\right); \quad \varphi_p = \frac{kT}{q}\ln\left(\frac{N_v}{N_a}\right), \tag{3}$$

where k is the Boltzmann's constant, T is the temperature, q is the electronic charge, N_c and N_v are the density of states for the conduction and valence bands, respectively, while N_a and N_d are the acceptor and donor concentrations, respectively. Thus, the built-in potential is obtained as

$$q\psi_{bi} = E_g - kT\ln\left(\frac{N_c N_v}{N_a N_d}\right). \tag{4}$$

Hence, the built-in potential of a p-n junction is directly dependent on the band gap of the semiconductor. It is interesting to note that the quantities in the natural logarithm in Equation (4) are dependent on the effective mass of the semiconductor. Thus, it is expected that a change in band gap and DOS parameters of a semiconductor will affect the built-in potential of the diode. Further, the band gap also directly affects the breakdown of a p-n junction diode. Breakdown occurs when a high reverse voltage is applied across the junction. This high electric field accelerates the electrons travelling across the junction, such that they have enough kinetic energy to create an electron-hole pair. This phenomenon, known as impact ionization, results in the creation of more carriers that are themselves accelerated, creating even more carriers. This process, known as avalanche breakdown, is a positive feedback process causing a very high current at a particular reverse voltage. This reverse voltage which causes the breakdown should be enough to accelerate the carriers to an energy that is slightly above the band gap energy of the semiconductor to cause impact ionization and start the breakdown. In case of lower band gaps, the energy for impact ionization is lower, thus leading to lower breakdown voltages. Hence, it is also expected that the reverse breakdown voltage for a semiconductor with lower band gap should be lower. Since we have shown the band gap of SiSn to be lower than silicon in our previous work,[26–29] we expect the built-in potential and the reverse breakdown voltage to be lower for SiSn compared to silicon.

We fabricated abrupt, homogenous junction diodes to verify the change in band gap for the SiSn lattice as compared to silicon. To obtain SiSn with uniform Sn diffusion profile, we deposited a thin film of Sn (20 nm) on a lightly doped, p-type silicon substrate using argon plasma sputtering (10 sccm, 5 mTorr) on a tin target (Sn, 99.99%, Sigma Aldrich). We annealed the sample at 750 °C for 20 min in argon ambient to diffuse the Sn into the silicon lattice. The remaining Sn was removed using a dilute hydrochloric acid (HCl) bath for 10 min. The samples were then cleaned using piranha (H_2SO_4:H_2O_2) at 120 °C and buffered oxide etchant (BOE). We then deposited 300 nm of silicon oxide using plasma enhanced chemical vapor deposition (PECVD) at 300 °C. The active areas were exposed using photolithography and reactive ion etching (RIE) of silicon oxide (SiO_2). The active areas were implanted with arsenic (As, 30 keV, 5×10^{15} cm^{-2}, no tilt) to make the top surface of the lattice heavily doped n-type and hence form a p-n junction. We activated the implanted arsenic using rapid thermal anneal process (1000 °C, 30 s, N_2/H_2 ambient). We deposited a thin film of Ni (50 nm) using e-beam evaporation and annealed the sample (450 C, 5 min, argon ambient) to form nickel silicide on the active areas for ohmic contact to the heavily doped region. The residual nickel was removed using a chemical bath (H_2SO_4:H_2O_2, 120 °C, 10 min). Finally, 400 nm aluminum was deposited using argon plasma sputtering process (400 W, 25 sccm, 5 mTorr), and subsequently patterned using RIE to form metallic contacts to the active region. The process flow is schematically illustrated in Figure 2. To compare the performance of SiSn diodes with silicon, the control samples were fabricated following the same process steps and process conditions, apart from the Sn deposition step.

The formation of a junction and the diffusion of Sn into the silicon lattice were verified by performing secondary ion mass spectroscopy (SIMS) on the active area of the diode. The depth profiling experiment was carried out using a Dynamic-SIMS instrument (Hiden Analytical Ltd., Warrington, UK) under UHV conditions (10^{-9} Torr). The SIMS workstation is equipped with both argon and oxygen ion beams. While argon ions allow for a faster sputtering rate, the oxygen ions were used since they enhance the positive ion signals. The choice of oxygen was thus essential for improving the detection limit which is in the range of ppb for many elements. Before running a depth profile, the experimental conditions, including the energy and the current of the sputtering oxygen beam, were first optimized. Using oxygen at energy of 2 keV, the sputtering rate was high enough to allow for a reasonable analysis time and low enough to keep a good depth resolution. The oxygen beam was precisely centered in the middle of the diode active area. The raster of the sputtered area was estimated to be $300 \times 300\ \mu m^2$. In order to avoid the edge effect for the active area, it was necessary to acquire data from a small area located in the middle of the region. Using an adequate electronic gating, the acquisition area from which the depth profiling data were extracted was approximately $50 \times 50\ \mu m^2$. Throughout the sputtering process, the selected positive ions ascribed to tin, silicon, arsenic, and aluminum were sequentially collected using a MAXIM spectrometer equipped with a quadrupole analyzer. Ions were collected from the sample by a shaped extraction field and energy filtered using a parallel plate system, with the energy resolution matched to that of the quadrupole analyzer. After passing through a triple filter system, detected ions were measured using a pulse counting detector having a 4 keV post acceleration potential to increase the detection efficiency at

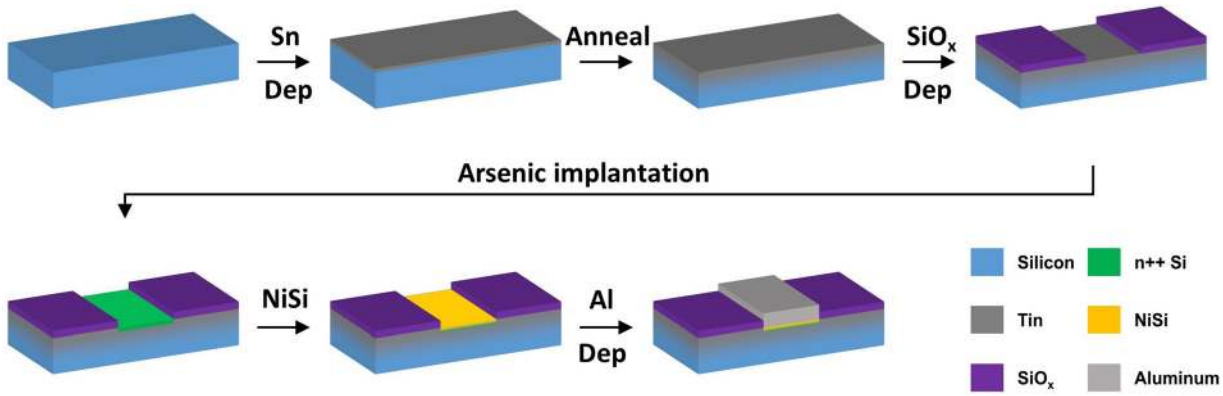

FIG. 2. Schematic illustration of the process flow followed for fabrication of SiSn diodes. Silicon control devices were formed using the same steps and process conditions, excluding the first two steps.

high masses. In order to convert the sputtering time scale to depth scale, the depth of the crater produced at the end of the experiment was scanned using a profilometer (Veeco Instruments Inc., NY, USA). The depth profiles of tin (Sn) and arsenic (As) are as shown in Figure 3 along with the scanning electron microscopy (SEM) images of the fabricated device. It can be clearly seen that the Sn level is maintained through a depth of 600–700 nm inside the silicon lattice, while the As level tails off exponentially after about 50–100 nm depth. Hence, we expect the junction formed to be homogenous (i.e., both n++ and p− regions are Sn alloyed with constant uniformity), and the built-in potential to be lower for the fabricated SiSn diodes in correspondence with the lower band gap of SiSn.

The fabricated SiSn and silicon control diodes were characterized using Keithley 4200 SCS semiconductor parameter analyzer coupled with a Cascade Microsystems MA150 probe station. For forward bias operation, a negative voltage was applied to the aluminum pad contacting the n++ region, while the substrate was grounded. Figure 4(a) shows the forward bias I-V characteristics for a representative device. The current increases exponentially after the built-in potential is applied to the junction, as expected from the diode characteristic equation

$$I = I_0\left(\exp\left(\frac{q(V-\psi_{bi})}{kT}\right) - 1\right), \tag{5}$$

where V is the applied potential difference across the junction. From Equation (5), it can be seen that the current remains negative until a forward bias equal to the built-in potential of the diode is applied. The current increases exponentially thereafter. Using Equation (5), we calculated the built-in potential for all the SiSn as well as silicon control diodes. Figure 4(b) shows the statistical distribution for the measured built-in potential. We report the difference between the average built-in potentials for SiSn and silicon to be 0.1 V. This lowering of built-in potential was expected from Equation (4). Figures 4(c) and 4(d) show the wafer map indicating the locations of the measured devices on a 4 in.

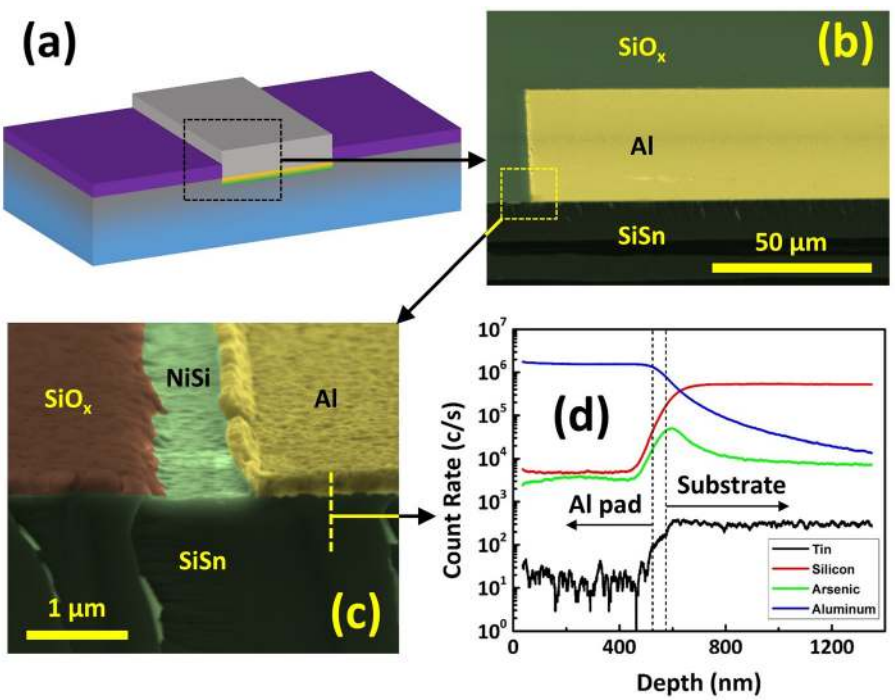

FIG. 3. (a) Schematic illustration and (b) and (c) scanning electron micrographs (SEMs) of the fabricated SiSn diode. The SEM in (b) is a tilted cross-section image with Al and SiO_x on the top horizontal plane and SiSn on the vertical plane. (d) Secondary Ion Mass Spectroscopy (SIMS) shows that the diffusion of Sn in silicon substrate is uniform up to 600–700 nm.

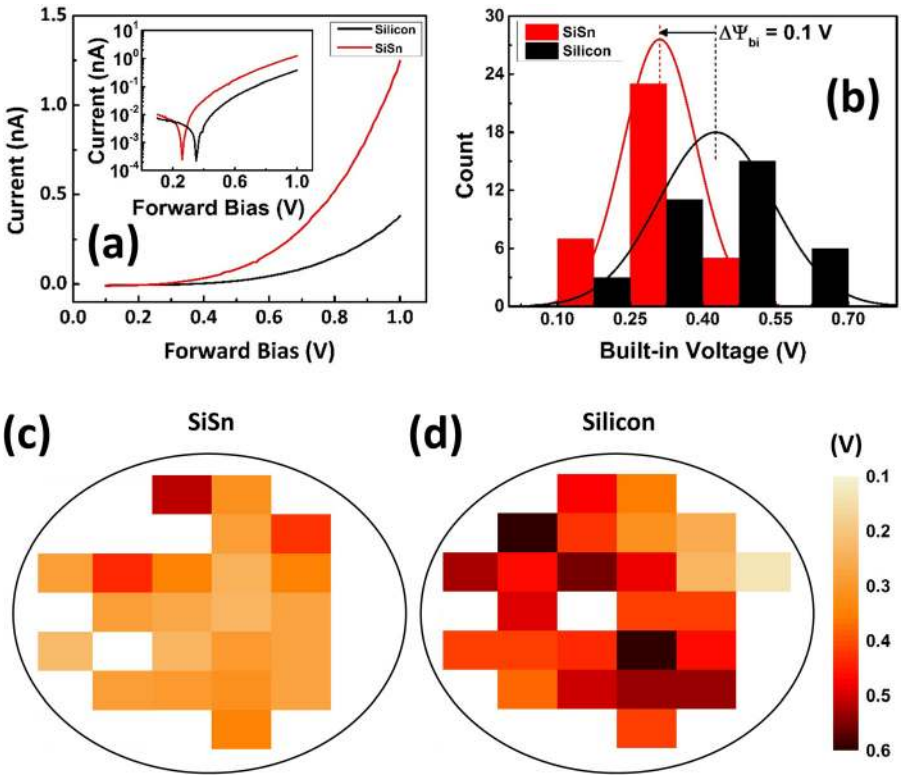

FIG. 4. (a) The I-V characteristic of a representative SiSn and silicon device. Inset: I-V characteristics of the devices in semi-log scale. (b) Statistical distribution of built-in potential for SiSn and silicon diodes shows that the average built-in potential decreased by 0.1 V for SiSn devices compared to silicon control. Wafer maps show the physical location of the measured devices and the built-in potentials for (c) SiSn and (d) silicon devices. The white spaces represent dies with no working diodes.

wafer and their respective built-in potentials. The locations with no color indicate failed devices. The die yield for the four wafers fabricated for this work was observed to be 64.2%.

For reverse bias operation, a high positive voltage was applied at the aluminum pad, while the substrate was grounded. Figure 5(a) shows the representative I-V curve for a reverse biased SiSn and silicon device. Before breakdown, the reverse bias current mainly comprises of diffusion current (from the minority carriers) and current from the generation of electron-hole pairs in the depletion region due to thermal emission (since $pn < n_i^2$). The emission current increases with the increase in depletion region, which is in turn strongly dependent on the applied electric field. Hence, reverse current increases steadily with applied voltage (before the breakdown). At breakdown, a surge in current can be clearly seen (Figure 5(a)). This surge in current indicated the avalanche breakdown of the diode and hence the potential at which it occurred was the measured breakdown voltage. Figure 5(b) shows the statistical distribution of measured breakdown voltages. We report a decrease of 0.2 V in the average breakdown voltage for SiSn diodes as compared to the silicon control devices. This lowering was, again, as expected from theory since the band gap of SiSn is lower thus requiring a lower potential to create impact ionization across the junction. The breakdown voltage for an abrupt junction diode is given by[31,32]

$$V_{Br} = 5.2 \times 10^{13} N_a^{-\frac{3}{4}} E_g^{\frac{3}{2}}. \tag{6}$$

With the acceptor concentration assumed to be invariant with the incorporation of Sn, the band gap of SiSn can be expressed as

$$E_{g(SiSn)} = E_{g(Si)} \left(\frac{V_{Br(SiSn)}}{V_{Br(Si)}} \right)^{\frac{2}{3}}. \tag{7}$$

Now, both $V_{Br(SiSn)}$ and $V_{Br(Si)}$ are statistical variables with the distribution shown in Figure 5(b). The band gap of silicon is well known and is considered constant at 1.16 V for this analysis. When these statistical values are used to calculate the value of the band gap of SiSn using the above

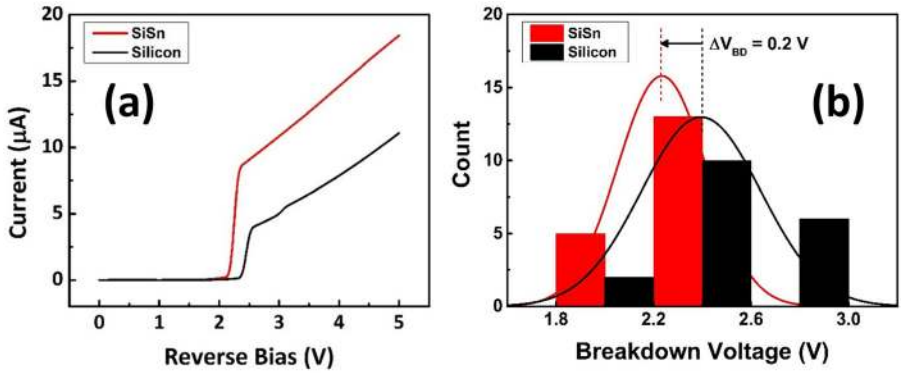

FIG. 5. (a) The reverse bias I-V characteristic of a representative SiSn and silicon device. (b) Statistical distribution of reverse breakdown voltage for SiSn and silicon diodes shows that the average breakdown voltage decreased by 0.2 V for SiSn devices compared to silicon control.

equation, following the standard rules of error propagation for statistical variables, the experimental band gap is obtained as 1.11 ± 0.09 eV. This is in agreement with the expected value of close to 1.13 eV for ~1% Sn in silicon.[27,33] The agreement between the expected and calculated values of band gap of SiSn provides evidence that the fabricated devices follow p-n junction physics and the observed effects are from band gap changes rather than parasitic effects like Fermi level pinning.

In conclusion, we report the lowering of both measured built-in potential and breakdown voltage for SiSn diodes as compared to silicon control devices by 0.1 V and 0.2 V, respectively. This lowering was as expected from the theoretical analysis presented in the paper. We report the experimentally calculated band gap of SiSn to be 1.11 ± 0.09 eV. The incorporation of Sn thus offers a unique opportunity to alter silicon lattice band gap without compromising its semiconductor properties. The fabrication of diodes after Sn diffusion shows that the SiSn thin film is stable and can withstand device processing. Hence, a low-cost, scalable, and CMOS compatible process has been developed to alter the band gap of silicon for select applications.

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