

# Sleep Switch Dual Threshold Voltage Domino Logic With Reduced Standby Leakage Current

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**Abstract**—A circuit technique is presented for reducing the subthreshold leakage energy consumption of domino logic circuits. Sleep switch transistors are proposed to place an idle dual threshold voltage domino logic circuit into a low leakage state. The circuit technique enhances the effectiveness of a dual threshold voltage CMOS technology to reduce the subthreshold leakage current by strongly turning off all of the high threshold voltage transistors. The sleep switch circuit technique significantly reduces the subthreshold leakage energy as compared to both standard low-threshold voltage and dual threshold voltage domino logic circuits. A domino adder enters and leaves a low leakage sleep mode within a single clock cycle. The energy overhead of the circuit technique is low, justifying the activation of the proposed sleep scheme by providing a net savings in total power consumption during short idle periods.

**Index Terms**—Domino carry lookahead adder, domino logic, dual threshold voltage CMOS technologies, dynamic circuits, high speed, idle mode, longer battery life, low power, multiple threshold voltage CMOS, reduced standby leakage energy, sleep mode, sleep switch, subthreshold leakage current.

## I. INTRODUCTION

THE POWER consumed in high-performance microprocessors has increased to levels that impose a fundamental limitation to increasing performance and functionality [1]–[3]. If the current trend in increasing power continues, high performance microprocessors will soon consume thousands of watts. The power density of a high performance microprocessor will exceed the power density levels encountered in typical rocket nozzles within the next decade [2]. The generation, distribution, and dissipation of power are at the forefront of current problems faced by the integrated circuit industry [1]–[5].

Dynamic switching power, the dominant component of the total power consumed in current CMOS technologies, is quadratically reduced by lowering the supply voltage. Lowering the supply voltage, however, also degrades circuit speed due to reduced transistor currents. Threshold voltages are scaled to reduce the degradation in speed caused by supply voltage scaling while maintaining the dynamic power consumption within acceptable levels [1]–[5]. At reduced threshold voltages, however, subthreshold leakage currents increase exponentially. As depicted in Fig. 1, subthreshold leakage power is soon

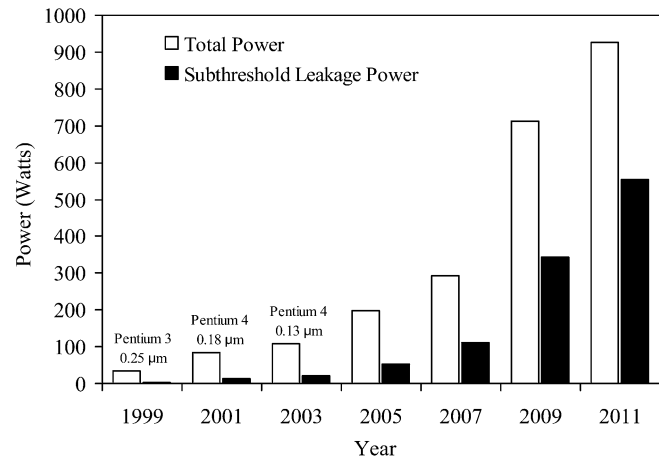


Fig. 1. Power trends of high performance microprocessors.

expected to dominate the total power consumed by a CMOS circuit [1], [2], [5]. Energy efficient circuit techniques aimed at lowering leakage currents are, therefore, highly desirable.

Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [7]–[14]. A dual threshold voltage (dual- $V_t$ ) circuit technique was proposed in [9] for reducing the subthreshold leakage energy consumption of domino logic circuits. The technique proposed in [9] utilizes both high and low threshold voltage transistors. High threshold voltage (high- $V_t$ ) transistors are employed on the noncritical precharge paths. Alternatively, low threshold voltage (low- $V_t$ ) transistors are employed on the speed critical evaluation paths. Gating all of the inputs of the first stage of a domino pipeline is proposed to place the idle domino gates into a low leakage state [9].

The energy and delay overhead for entering and leaving the sleep mode, however, has not been addressed in [9]. Due to the additional gates at the inputs, significant dynamic switching energy is consumed to activate the sleep mode with the technique described in [9]. Additional energy is dissipated to precharge all of the dynamic nodes while reactivating a domino logic circuit at the end of an idle period. In order to justify the use of additional circuitry to place a dual- $V_t$  circuit into a low leakage state, the total energy consumed to enter and leave the standby mode must be significantly less than the savings in the standby leakage energy. Gating all of the inputs of the first stage of a domino circuit in a domino pipeline also increases the circuit area and active mode power. Furthermore, the circuit performance during the active mode is degraded due to the additional gates at the inputs. A circuit technique with low delay and energy overhead

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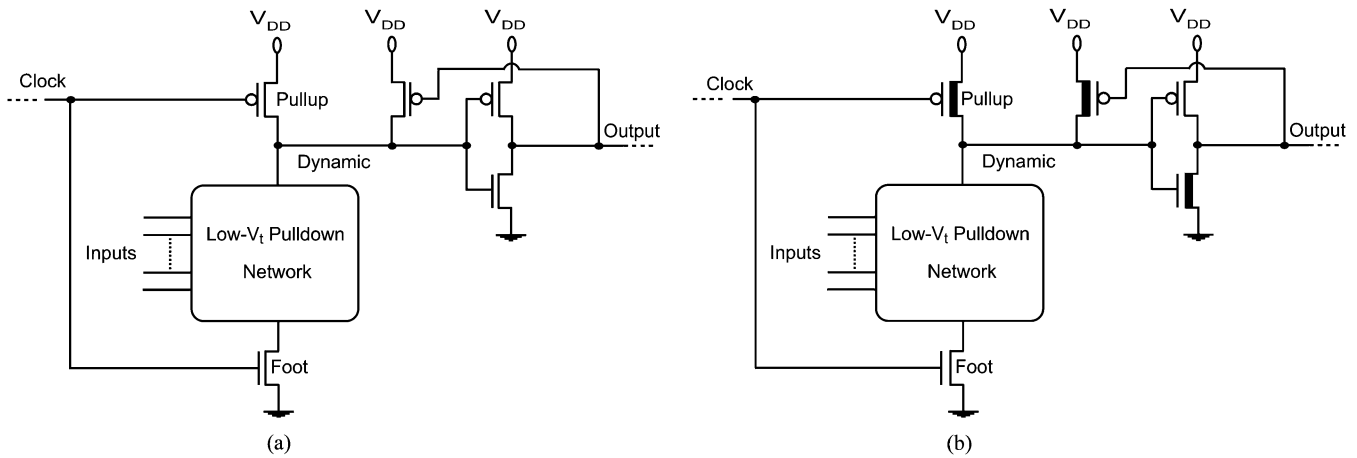


Fig. 2. Standard domino logic circuits. (a) Standard low- $V_t$  domino logic circuit. (b) Standard dual- $V_t$  domino logic circuit. High- $V_t$  transistors are symbolically represented by a thick line in the channel region.

for placing a dual- $V_t$  domino logic circuit into a low leakage state is, therefore, highly desirable.

A circuit technique is proposed in this paper for lowering the subthreshold leakage energy consumption of domino logic circuits. The proposed circuit technique employs sleep switches and a dual threshold voltage CMOS technology in order to place an idle domino logic circuit into a low-leakage state. An eight bit domino carry lookahead adder is designed based on the circuit technique. The sleep switch circuit technique reduces the leakage energy by up to 830 times as compared to a standard low-threshold voltage domino circuit. The sleep switch dual- $V_t$  domino adder enters and leaves the sleep mode within a single clock cycle. The sleep switch circuit technique enhances the effectiveness of a dual- $V_t$  CMOS technology to reduce the subthreshold leakage current by strongly turning off all of the high- $V_t$  transistors, independent of the input vector. The sleep switch circuit technique lowers the subthreshold leakage energy by up to 714 times as compared to a standard dual- $V_t$  domino logic circuit. The energy overhead of the circuit technique is low, permitting the sleep transistors to be activated during idle periods as short as 57 clock cycles so as to reduce the total power consumption.

The standard dual- $V_t$  domino logic circuit technique is reviewed in Section II. Previously published leakage control techniques applicable to dual- $V_t$  domino logic circuits are also discussed in Section II. The operation of the sleep switch dual- $V_t$  domino logic circuit technique is described in Section III. Simulation results characterizing the standby leakage energy and active mode delay and power of the sleep switch technique as compared to standard dual- $V_t$  and low- $V_t$  domino circuits are presented in Section IV. The effect of a dual threshold voltage CMOS technology on the noise immunity characteristics of a domino logic circuit is evaluated in Section V. Some conclusions are provided in Section VI.

## II. DUAL THRESHOLD VOLTAGE DOMINO LOGIC

Employing dual threshold voltage (dual- $V_t$ ) transistors for leakage reduction in domino logic circuits was first proposed by Kao [9]. Standard low- $V_t$  and dual- $V_t$  domino logic circuits are

shown in Fig. 2. The critical signal transitions that determine the delay of a domino logic circuit occur along the evaluation path. In a dual- $V_t$  domino circuit, therefore, all of the transistors that can be activated during the evaluation phase have a low- $V_t$ . Alternatively, the precharge phase transitions are not critical for the performance of a domino logic circuit. Therefore, those transistors that are active during the precharge phase have a high- $V_t$  [see Fig. 2(b)].

If all of the high- $V_t$  transistors are cutoff in a dual- $V_t$  domino logic circuit, the leakage current is significantly reduced as compared to a low- $V_t$  circuit. The clock is gated high, cutting off the high- $V_t$  pullup transistors when a domino logic circuit is idle. In a standard dual- $V_t$  domino logic circuit, the modes of operation of the remaining dual- $V_t$  portion of the high- $V_t$  transistors (other than the pullup transistors) are determined by the input vectors applied after the clock is gated high.

Subthreshold leakage current exponentially decreases with increasing threshold voltage. The leakage current of a cutoff high- $V_t$  transistor is orders of magnitude lower as compared to a low- $V_t$  transistor [5], [6]. Assuming a subthreshold slope of 85 mV/decade (a typical number in current CMOS technologies [15], [16]), an 85 mV increase in the threshold voltage of a transistor reduces the subthreshold leakage current by ten times. Leakage currents in a dual- $V_t$  circuit can be reduced by employing a greater number of high- $V_t$  transistors [5]. Unless all of the high- $V_t$  transistors are strongly cutoff, the potential savings in energy from the dual- $V_t$  domino circuit technique cannot be fully exploited. Circuit techniques to place a domino logic circuit into a low leakage state regardless of the input vectors and the initial circuit node voltage states (before the clock is gated) are desirable. Dual- $V_t$  domino logic circuit techniques with different standby control mechanisms have been proposed in the literature [9]–[14].

A dual- $V_t$  circuit technique was proposed in [9] to reduce the leakage current in domino pipelines. The dual- $V_t$  circuit technique described in [9] requires the input signals of the first stage circuits in a domino pipeline to be gated. After forcing the first stage of the domino gates to evaluate and discharge, the domino gates of the subsequent stages in the pipeline also evaluate and discharge in a domino fashion. The technique proposed in [9],

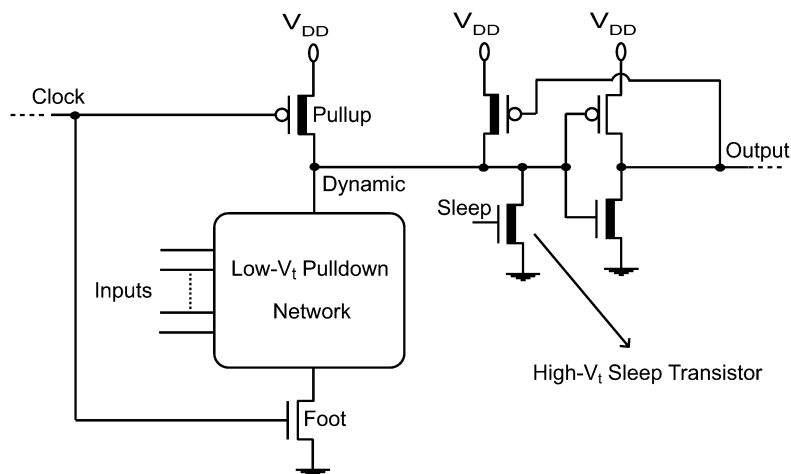


Fig. 3. Sleep switch dual- $V_t$  domino logic circuit technique. High- $V_t$  transistors are symbolically represented by a thick line in the channel region.

however, is ineffective in placing a circuit into a low leakage state if some of the domino gates in a cascaded domino logic circuit require inverted signals (such as an XOR domino gate generating a sum bit at the output stage of a domino carry lookahead adder). Most domino logic circuits cannot be placed into a minimum leakage state in which all of the high- $V_t$  transistors are strongly cutoff simply by gating the input vectors of the first stage of a domino circuit. The technique proposed in [9] also requires a significant dynamic switching energy overhead for activating the sleep mode due to the additional gates at the inputs. The dual- $V_t$  domino circuit proposed in [9] only offers a savings in energy if the circuit stays idle for a long time. Furthermore, gating all of the inputs of the first stage of a domino circuit in a domino pipeline increases the circuit area and active mode power. The circuit performance during the active mode is also degraded due to the additional gates at the inputs.

An alternative dual- $V_t$  technique was proposed in [12] to reduce the dynamic power, propagation delay, and area overhead as compared to the technique proposed in [9]. Although the delay and area overhead is reduced by the technique proposed in [12], the energy consumed during the standby mode is higher as compared to the circuit proposed in [9]. This increased standby energy is primarily due to the nMOS transistor inside the output inverter of the domino gates in the first stage of each domino pipeline not being completely turned off and because the keeper has a low- $V_t$  in the technique described in [12]. As discussed in [24], dual- $V_t$  domino logic circuits based on a low- $V_t$  keeper transistor consume significantly higher subthreshold leakage energy as compared to dual- $V_t$  circuit techniques based on a high- $V_t$  keeper transistor under similar noise immunity conditions.

The approach of utilizing the leakage currents of the pull-down path transistors was proposed in [14] in order to place a dual- $V_t$  domino logic circuit into a low leakage state. High- $V_t$  switches are employed in series with the keeper and the nMOS transistor of the output inverter in a domino circuit. When the circuit is active, these high- $V_t$  switches are on and the circuit operates similarly to a standard dual- $V_t$  circuit. When the circuit is idle, the high- $V_t$  series switches are cutoff by a sleep signal, isolating the dynamic node from the power supply. The floating

dynamic node slowly discharges due to the leakage current of the transistors along the pulldown path. The high- $V_t$  switch in series with the nMOS transistor of the output inverter ensures that no short-circuit power is consumed during the slow discharge of the dynamic node. A high- $V_t$  series transistor at the output inverter, however, degrades the precharge delay. Furthermore, a high- $V_t$  transistor in series with a keeper degrades the noise immunity. To minimize the degradation in noise immunity and precharge delay, the size of these series switches should be increased. Wider series transistors, however, increase the energy overhead of activating the standby leakage control mechanism. Increasing the series transistor size also increases the area overhead of this technique. Another disadvantage of this technique is the low speed of the proposed mechanism for placing a circuit into a low leakage state. The circuit technique proposed in [14], therefore, may not be feasible for fine-grain leakage reduction during short idle periods (a few tens to hundreds of clock cycles) in high performance integrated circuits.

### III. DUAL THRESHOLD VOLTAGE DOMINO LOGIC EMPLOYING SLEEP SWITCHES

A low energy and delay overhead circuit technique is proposed in this paper to lower the subthreshold leakage currents in an idle domino logic circuit. The circuit technique employs sleep switches to place a dual- $V_t$  domino logic circuit into a low leakage state within a single clock cycle. A domino logic circuit based on the sleep switch dual- $V_t$  circuit technique is shown in Fig. 3.

A high- $V_t$  nMOS switch is added to the dynamic node of a domino circuit as shown in Fig. 3. The operation of this transistor is controlled by a separate sleep signal. During the active mode of operation, the sleep signal is set low, the sleep switch is cut-off, and the proposed dual- $V_t$  circuit operates as a standard dual- $V_t$  domino circuit. During the standby mode of operation, the clock signal is maintained high, turning off the high- $V_t$  pull-up transistor of each domino gate. The sleep signal transitions high, turning on the sleep switch. The dynamic node of the domino gate is discharged through the sleep switch, thereby turning off the high- $V_t$  nMOS transistor within the

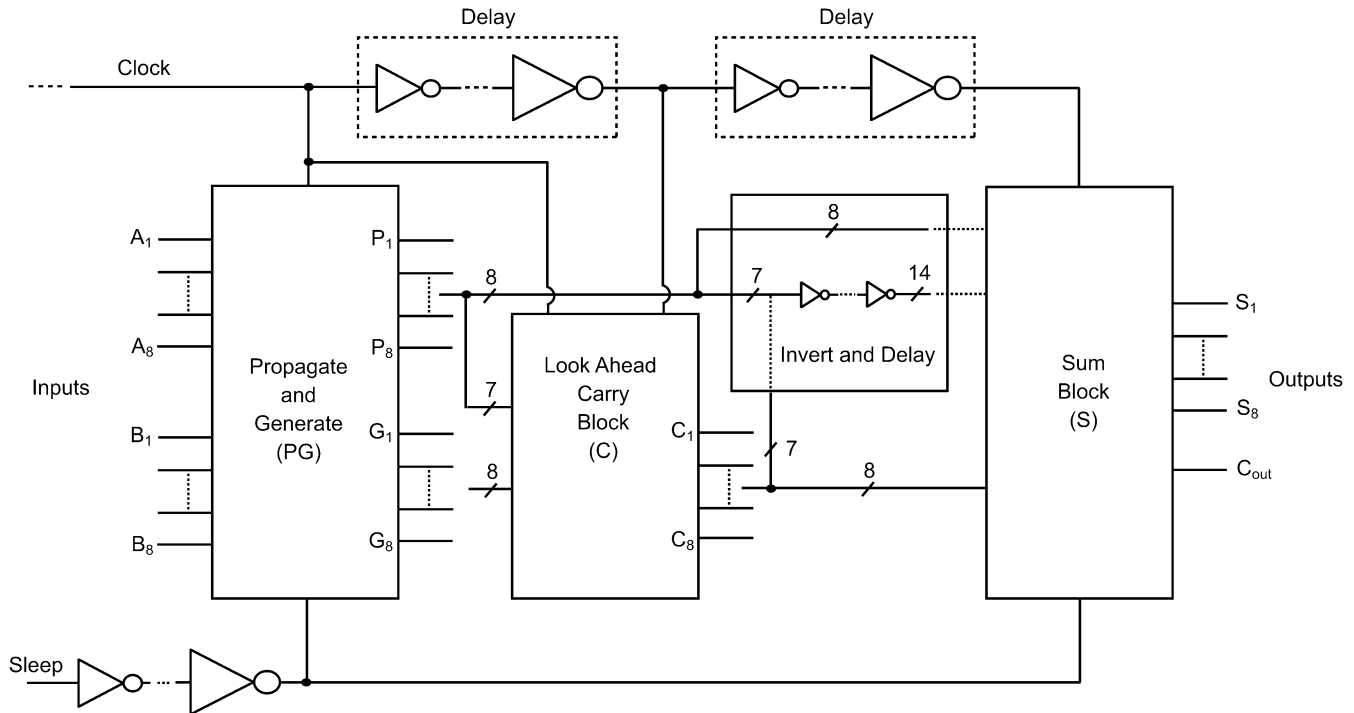


Fig. 4. Block diagram of a clock-delayed domino carry lookahead adder with the sleep switch dual- $V_t$  circuit technique.

output inverter. The output transitions high, cutting off the high- $V_t$  keeper. Following the low-to-high transition of the output of a sleep switch dual- $V_t$  domino gate, the subsequent gates (fed by the noninverting signals) also evaluate and discharge in a domino fashion. After the node voltages settle to a steady state, all of the high- $V_t$  transistors are strongly cut-off, significantly reducing the subthreshold leakage current. Note that this technique, requiring no additional gating on the input signals while strongly turning off all of the high- $V_t$  transistors within a single clock cycle, is significantly more power, delay, and area efficient as compared to the techniques proposed in [9], [12], and [14].

#### IV. SIMULATION RESULTS

Eight input clock-delayed domino carry lookahead adders based on the low- $V_t$ , standard dual- $V_t$ , and sleep switch circuit techniques are evaluated assuming a 0.18- $\mu\text{m}$  CMOS technology ( $V_{\text{tnlow}} = |V_{\text{tplow}}| = 200$  mV,  $V_{\text{tnhigh}} = |V_{\text{tphigh}}| = 500$  mV, and  $T = 110^\circ\text{C}$ ). The block diagram of a clock-delayed domino carry lookahead adder based on the sleep switch dual- $V_t$  circuit technique is shown in Fig. 4. Each sum output drives a capacitive load of 10 fF. A 1-GHz clock with a 50% duty cycle is applied to the domino logic circuits. All of the common transistors in the sleep switch and standard dual- $V_t$  adders are sized the same.

In the sleep switch adder, all of the propagate (P), generate (G), and sum (S) domino gates have sleep switches. When the domino adder is idle, the dynamic nodes of the P and G domino gates (in the first stage propagate and generate (PG) block) are forced to discharge via sleep switches. The domino gates within the lookahead carry (C) block do not contain sleep switches. Following the low-to-high transition at the outputs of the P and

TABLE I  
INPUT VECTORS APPLIED TO AN ADDER

	$V_0$	$V_1$	$V_2$	$V_3$	$V_4$	$V_5$
A	0	0	1	1	255	255
B	0	255	255	127	255	0

G gates, the domino gates within the carry block also evaluate and discharge in a domino fashion. Some of the signals originating from the PG and C blocks are inverted before being fed into the sum block (see Fig. 4). The domino logic circuits within the sum block, therefore, also require sleep switches in order to place the circuits into a low leakage state.

The input vectors applied to an adder are listed in Table I. The leakage characteristics of the circuits are evaluated for six input vectors,  $V_0$  to  $V_5$ .  $C_{\text{out}}(S_8)$  is evaluated through the critical path of the carry chain within the carry block for the input vector  $V_2(V_3)$ . The delay and active mode power are calculated for  $V_2$  and  $V_3$ .

The sleep switch circuit technique significantly reduces the subthreshold leakage current as compared to both low- $V_t$  and standard dual- $V_t$  circuits. The standby leakage energy characteristics of the adders based on the standard dual- $V_t$ , low- $V_t$ , and sleep switch circuit techniques are presented in Section IV-A. The subthreshold leakage current characteristics of a standard domino logic circuit displays a strong dependence on the input vectors when the circuit is at a high dynamic node voltage state. The stack effect on the subthreshold leakage current characteristics of a domino logic circuit at a high dynamic node voltage state is described in Section IV-B. The sleep switch circuit technique also enhances the active mode delay and power characteristics as compared to a low- $V_t$  circuit. The active mode delay and power characteristics of the circuit technique are discussed

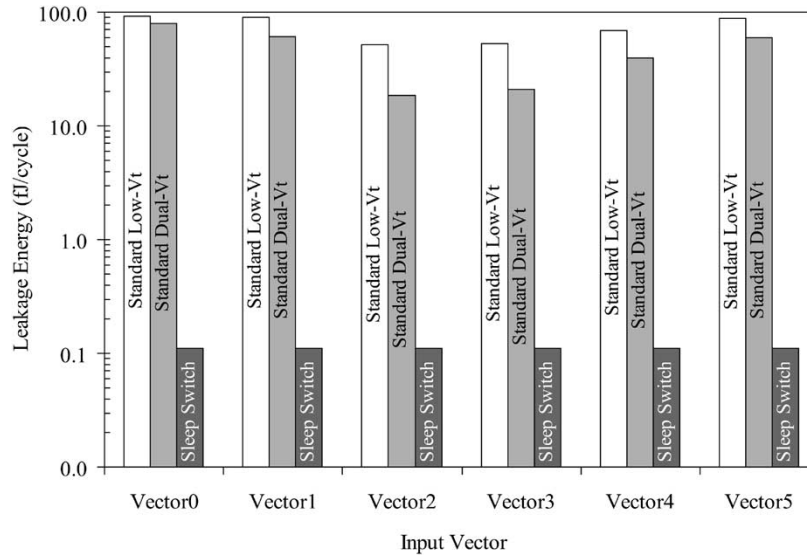


Fig. 5. A comparison of the leakage energy (per clock cycle) of the adder circuits with the low- $V_t$ , standard dual- $V_t$ , and sleep switch circuit techniques for six different input vectors.

in Section IV-C. The sleep/wake-up delay and energy overhead are presented in Section IV-D.

#### A. Subthreshold Leakage Energy Reduction

The standby leakage energy characteristics of the low- $V_t$ , standard dual- $V_t$ , and sleep switch dual- $V_t$  adders are evaluated in this section. When a low- $V_t$ , standard dual- $V_t$ , or sleep switch domino logic circuit is idle, the clock is gated high. In a sleep switch circuit, the sleep transistors are activated after clock gating. The leakage energy consumption (per clock cycle) of the low- $V_t$ , standard dual- $V_t$ , and sleep switch adders is shown in Fig. 5.

The leakage energy of a standard dual- $V_t$  circuit is reduced by  $1.2 \times$  to  $2.8 \times$  as compared to a low- $V_t$  circuit. The standby leakage energy of the standard low- $V_t$  and dual- $V_t$  circuits is dependent on the applied input vector after the clock signal is gated high. The dynamic nodes of all of the domino logic circuits are precharged when the clock is low. After the clock transitions high, a portion of these domino gates evaluates and discharges provided that a necessary input combination to discharge the dynamic node is applied. A high dynamic node voltage state is typically the highest leakage state for a dual- $V_t$  domino logic gate since all of the high- $V_t$  transistors (other than the pullup transistors) operate in the strong inversion region. As discussed in Section II, the advantages of a dual- $V_t$  CMOS technology for reducing the leakage current are maximized when all of the high- $V_t$  transistors are strongly cutoff during the idle mode. For  $V_0$ , the dynamic nodes of all of the domino logic gates of a standard dual- $V_t$  adder are maintained high during the idle mode. The  $V_0$  vector, therefore, produces the maximum leakage current in a standard dual- $V_t$  adder. For  $V_0$ , the subthreshold leakage current is produced by the low- $V_t$  transistors rather than the high- $V_t$  transistors in a standard dual- $V_t$  adder. The subthreshold leakage current of the domino gates within the standard low- $V_t$  and dual- $V_t$  adders is, therefore, similar for  $V_0$ . The small difference between the subthreshold leakage current characteristics of the standard low- $V_t$  and dual- $V_t$  adders for  $V_0$  is

caused by the reduced leakage of the dual- $V_t$  delay elements in a standard dual- $V_t$  domino adder.

As shown in Fig. 5, the proposed sleep switch circuit technique minimizes the leakage energy for all of the input vectors as compared to both the low- $V_t$  and standard dual- $V_t$  circuits. Activating the sleep transistors places all of the domino gates into a low leakage state for any given input vector. The reduction in leakage energy offered by the sleep switch circuit technique varies between  $461 \times (V_2)$  and  $830 \times (V_0)$  as compared to a low- $V_t$  adder. The proposed circuit technique enhances the effectiveness of a dual- $V_t$  CMOS technology to reduce the subthreshold leakage current by cutting off all of the high- $V_t$  transistors. An adder based on the sleep switch circuit technique dissipates  $167 \times (V_2)$  to  $714 \times (V_0)$  lower leakage energy as compared to a standard dual- $V_t$  adder.

#### B. Stack Effect in Domino Logic Circuits

For  $V_1$  and  $V_5$ , the dynamic nodes of the generate and carry gates are maintained high while the propagate and sum gates evaluate and discharge in a standard domino adder. In a standard dual- $V_t$  adder, the subthreshold leakage current in the propagate and sum gates is  $2415 \times$  and  $1149 \times$ , respectively, smaller for both  $V_1$  and  $V_5$  as compared to  $V_0$ . Similarly, in a standard low- $V_t$  adder, the subthreshold leakage current in the propagate and sum gates is  $3.3 \times$  and  $1.7 \times$ , respectively, smaller for  $V_1$  and  $V_5$  as compared to  $V_0$ . Despite this significant reduction in the subthreshold leakage current of the propagate and sum gates, the second and third highest leakage currents in standard low- $V_t$  and dual- $V_t$  domino logic circuits are observed for  $V_1$  and  $V_5$ , respectively, as shown in Fig. 5. The subthreshold leakage current of the generate and carry gates in standard dual- $V_t$  and low- $V_t$  adders approximately doubles for  $V_1$  and  $V_5$  as compared to  $V_0$ . This significant increase in subthreshold leakage current with input vector for a high dynamic node voltage state of the generate and carry gates is caused by the stack effect [18], [19].

The input vectors applied after clock gating determine which transistors produce subthreshold leakage current together with

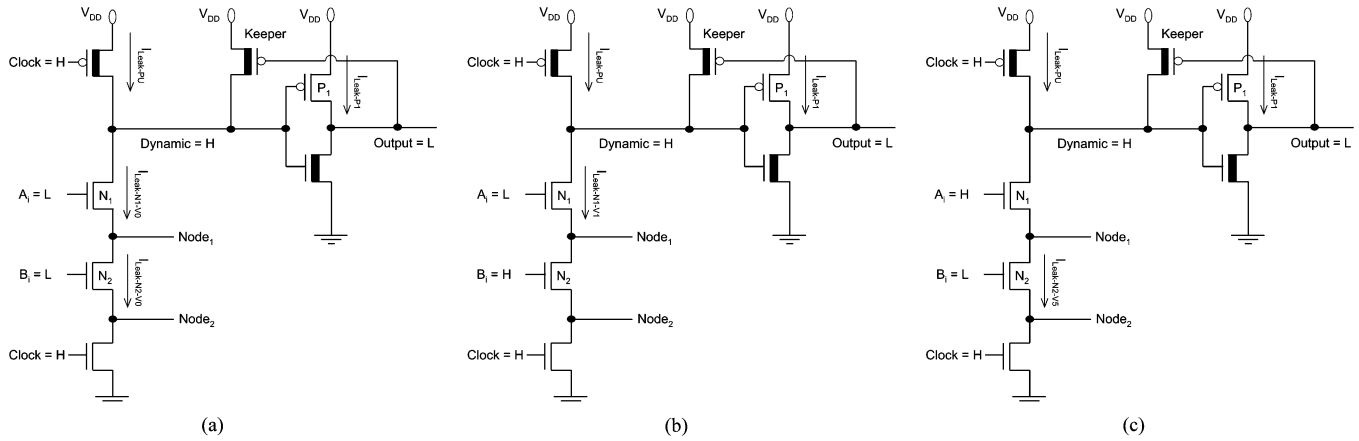


Fig. 6. Variation of subthreshold leakage current conduction paths with input vector for a high-voltage state at the dynamic node in a standard dual- $V_t$  domino logic circuit. (a) Sources of subthreshold leakage current for  $V_0$ . (b) Sources of subthreshold leakage current for  $V_1$ . (c) Sources of subthreshold leakage current for  $V_5$ . H: high. L: low.

the voltage state of the dynamic node. As discussed previously, a high dynamic node voltage state is typically the highest leakage state in a dual- $V_t$  domino logic gate. A variation of the subthreshold leakage current sources in the pulldown network of a standard dual- $V_t$  domino (generate) gate with the input vector for a high-voltage state at the dynamic node is shown in Fig. 6. The dynamic node voltage in the generate and carry gates is maintained high for three different input vectors,  $V_0$ ,  $V_1$ , and  $V_5$ , as shown in Fig. 6(a)–(c), respectively.

For  $V_0$ , both  $N_1$  and  $N_2$  operate in the weak inversion region. The voltage at Node<sub>1</sub> rises until the subthreshold leakage currents through  $N_1$  and  $N_2$  are equal (in the steady state condition). The total subthreshold leakage current at steady state is

$$I_{\text{subthreshold-H}} = I_{\text{Leak-PD}} + I_{\text{Leak-P1}} \quad (1)$$

$$I_{\text{Leak-PD}} = I_{\text{Leak-N1-V0}} = I_{\text{Leak-N2-V0}} \quad (2)$$

where  $I_{\text{Leak-P1}}$  is the subthreshold leakage current through the low- $V_t$  pullup transistor within the output inverter.  $I_{\text{Leak-N1-V0}}$  and  $I_{\text{Leak-N2-V0}}$  are the subthreshold leakage currents through  $N_1$  and  $N_2$ , respectively, for  $V_0$ .

For  $V_1$ ,  $N_1$  operates in the weak inversion region. Alternatively,  $N_2$  operates in the strong inversion region. The total subthreshold leakage current at steady state is

$$I_{\text{subthreshold-H}} = I_{\text{Leak-N1-V1}} + I_{\text{Leak-P1}} \quad (3)$$

where  $I_{\text{Leak-N1-V1}}$  is the subthreshold leakage current through  $N_1$  for  $V_1$ .

For  $V_5$ ,  $N_2$  operates in the weak inversion region while  $N_1$  is turned on (strong inversion). The total subthreshold leakage current at steady state is

$$I_{\text{subthreshold-H}} = I_{\text{Leak-N2-V5}} + I_{\text{Leak-P1}} \quad (4)$$

where  $I_{\text{Leak-N2-V5}}$  is the subthreshold leakage current through  $N_2$  for  $V_5$ .

For  $V_0$ ,  $N_1$  and  $N_2$  are cutoff. A steady state voltage is reached when the voltage at Node<sub>1</sub> rises to approximately 41 mV above ground, equalizing the subthreshold leakage currents through  $N_1$  and  $N_2$ . The subthreshold leakage current through a stack of cutoff transistors is significantly smaller than the

subthreshold leakage current through a single cutoff transistor [18], [19]. The subthreshold leakage current of a MOSFET is exponentially dependent on the threshold, gate-to-source, and drain-to-source voltages [20], [21]. The subthreshold leakage current through  $N_1$  exponentially decreases for  $V_0$  as compared to  $V_1$ , due to increased threshold voltage (reverse body bias), negative gate-to-source voltage, and lower drain-to-source voltage. For  $V_1$ , the voltages of Node<sub>1</sub> and Node<sub>2</sub> are both at approximately ground level since  $N_2$  operates in the strong inversion region. This condition eliminates the reverse body bias and negative gate-to-source voltage while increasing the drain-to-source voltage of  $N_1$ .  $I_{\text{Leak-N1-V1}}$  is, therefore, higher as compared to  $I_{\text{Leak-N1-V0}}$ . The total subthreshold leakage current of the generate gates is  $2.3 \times$  higher for  $V_1$  as compared to  $V_0$ . Similarly, the subthreshold leakage current of the carry gates is  $1.7 \times$  higher for  $V_1$  as compared to  $V_0$ . For  $V_5$ ,  $N_1$  is on while  $N_2$  is cutoff. The voltage at Node<sub>1</sub> is high, increasing the drain-to-source voltage of  $N_2$ .  $I_{\text{Leak-N2-V5}}$  is, therefore, higher than  $I_{\text{Leak-N2-V0}}$ , increasing the total subthreshold leakage current of the generate gates by  $2.1 \times$ . Similarly, the subthreshold leakage current of the carry gates is  $1.7 \times$  higher for  $V_5$  as compared to  $V_0$ . The subthreshold leakage currents in the standard low- $V_t$  carry and generate gates also significantly decrease for  $V_0$  as compared to  $V_1$  and  $V_5$ , due to the stack effect.

### C. Delay and Power Reduction in the Active Mode

The active mode delay, power, and power delay product (PDP) of low- $V_t$ , standard dual- $V_t$ , and sleep switch adders are shown in Fig. 7. The delay and power characteristics of a standard dual- $V_t$  adder are similar to the sleep switch adder. The sleep switch circuit technique enhances the evaluation speed by 12% and 21%, for  $V_2$  and  $V_3$ , respectively, as compared to a low- $V_t$  adder. The enhancement in speed with the proposed circuit technique is primarily due to the reduced contention current [7], [8], [17], [23] of a high- $V_t$  keeper.

The sleep switch circuit technique also reduces the active mode power consumption as compared to a low- $V_t$  circuit. The power dissipation is reduced by 14.4% and 14.6% for the input vectors  $V_2$  and  $V_3$ , respectively, as compared to a low- $V_t$  adder.

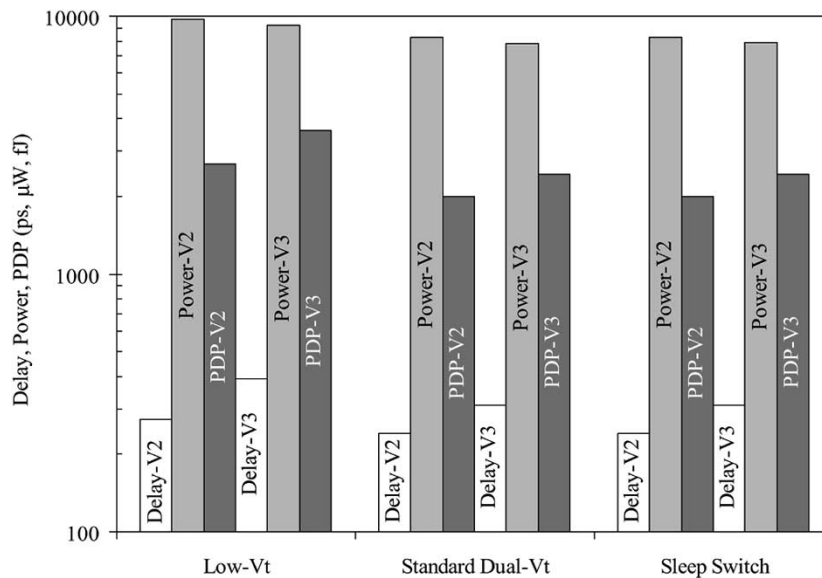


Fig. 7. A comparison of the delay, power, and PDP of adder circuits with low- $V_t$ , standard dual- $V_t$ , and sleep switch circuit techniques for the input vectors  $V_2$  and  $V_3$ .

A portion of the savings in active mode power is due to the reduced contention current [23] of the high- $V_t$  keeper transistor in a dual- $V_t$  circuit (see Figs. 2 and 3). Another important factor that reduces the power consumption of a dual- $V_t$  circuit is the lower power consumption in dual- $V_t$  delay elements.

#### D. Sleep/Wake-Up Delay and Energy Overhead of the Sleep Switch Circuit Technique

When a sleep switch domino logic circuit is idle, the clock is gated high. The sleep signal should be applied after the low-to-high edge of the clock signal propagates to the gates in the last stage of a clock-delayed domino logic circuit. Activating the sleep switches after the low-to-high transition of the clock ensures that no short-circuit power is consumed while entering the sleep mode. Activating the sleep switches forces all of the domino gates to a low dynamic node voltage state. After the node voltages settle, all of the high- $V_t$  transistors are strongly cut off, minimizing the subthreshold leakage currents with the proposed sleep switch circuit technique. Less than a clock period is required (depending upon the input vector, from 829 ps to 850 ps after the clock is gated) for the adder circuit to be placed in a low leakage state. Before the end of an idle mode, the sleep signal transitions low, cutting off all of the sleep switches. Disabling the sleep transistors before activating the clock is important in order to avoid short-circuit currents while leaving the idle mode. The clock is reactivated and all of the dynamic nodes are recharged to activate (wake-up) a sleeping domino circuit. The duration of reactivation is equal to the precharge time of a domino circuit. An adder circuit, therefore, is able to enter and leave the standby mode within a single clock cycle with the proposed circuit technique.

The energy overhead to enter and leave the sleep mode with the sleep switch technique is also evaluated. Activating the sleep switches to place a dual- $V_t$  domino logic circuit into standby mode requires a specific amount of energy. Additional energy

is dissipated at the end of an idle period while precharging the dynamic nodes in order to reactivate a domino logic circuit. Depending upon the input vectors, some or none of the dynamic nodes in the low- $V_t$  and standard dual- $V_t$  circuits are discharged during the sleep mode. Alternatively, all of the dynamic nodes in a sleep switch domino logic circuit are discharged during the sleep mode, independent of the input vectors. The activation energy required by the sleep switch circuit technique is, therefore, higher than the low- $V_t$  and standard dual- $V_t$  circuit techniques. In order to justify the proposed sleep switch circuit technique to force a dual- $V_t$  circuit into a low leakage state, the total energy consumed to enter and leave the sleep mode must be less than the total savings in standby leakage energy.

The cumulative energy dissipated in the standby mode by the low- $V_t$  and sleep switch adders is shown in Fig. 8. It is assumed that the junction temperature does not significantly change for the duration of the standby mode. The leakage energy per cycle is assumed to be constant. The cumulative energy of a low- $V_t$  domino circuit is only affected by the subthreshold leakage current during the standby mode. Alternatively, both the cumulative leakage energy and the energy overhead of entering and leaving the sleep mode are included in the energy characteristics of the sleep switch circuit. The total energy overhead of the sleep switch circuit technique is independent of the duration of the idle mode. The energy overhead for employing the sleep switch circuit technique is dissipated even if a domino circuit remains in the standby mode for only a single clock cycle. The total energy overhead of the proposed technique (composed of the energy dissipated in order to activate the sleep transistors while entering the sleep mode and disable the sleep transistors and reactivate the domino gates after the standby mode is over) is included as an energy step in the first cycle of the standby mode (see Fig. 8). Similar to the low- $V_t$  energy characteristics, after the first clock cycle, the sleep switch circuit energy is only due to the subthreshold leakage current. Since the standby leakage energy of a sleep switch circuit is significantly lower (up to 830

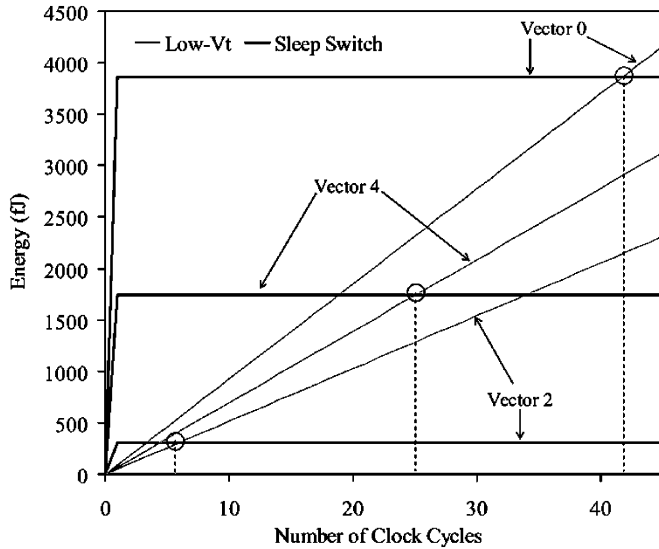


Fig. 8. Cumulative standby energy dissipation of the low- $V_t$  and sleep switch adders for three different input vectors.

times) than a low- $V_t$  circuit, the sleep switch energy characteristics have a much smaller slope as compared to the energy characteristics of the low- $V_t$  adder (see Fig. 8). A specific amount of time in the idle mode, also dependent upon the input vectors, is necessary for the cumulative leakage energy of a low- $V_t$  circuit to exceed the cumulative energy of a sleep switch circuit.

The intersection of the sleep switch and low- $V_t$  cumulative energy characteristics are evaluated to determine the necessary minimum duration of the sleep mode of operation such that the sleep switch circuit technique offers a net savings in energy as compared to a low- $V_t$  circuit. As shown in Fig. 8, the cumulative standby energy of the low- $V_t$  and sleep switch circuits exhibit different behavior depending upon the input vectors. The leakage current of a low- $V_t$  adder is smallest for  $V_2$  and highest for  $V_0$  (see Fig. 5). Alternatively, the leakage current of a sleep switch adder is virtually independent of the input vectors. Depending upon the input vectors, the energy overhead of the sleep switch scheme changes. For  $V_0$ , none of the dynamic nodes of a low- $V_t$  circuit are discharged during the standby mode. Alternatively, all of the dynamic nodes are discharged in a sleep switch circuit. The relative energy overhead of the sleep switch circuit technique required to charge the dynamic nodes to reactivate the circuit (to transition from standby mode to active mode) is, therefore, highest for  $V_0$ . As shown in Fig. 8, a minimum of 42 clock cycles is required for the proposed sleep switch circuit technique to provide a net savings in energy as compared to a low- $V_t$  circuit during the standby mode.

As discussed previously, a standard dual- $V_t$  circuit offers a savings in leakage current of  $1.2 \times$  to  $2.8 \times$  as compared to a low- $V_t$  circuit. The energy savings of a standard dual- $V_t$  domino circuit originates from the selective replacement of a group of high leakage low- $V_t$  transistors with a group of low leakage high- $V_t$  transistors. Unlike the proposed sleep switch circuit technique, a standard dual- $V_t$  circuit does not introduce any energy overhead in order to reduce the standby leakage current. Although the leakage energy of a sleep switch circuit is significantly reduced as compared to a standard dual- $V_t$  circuit, the

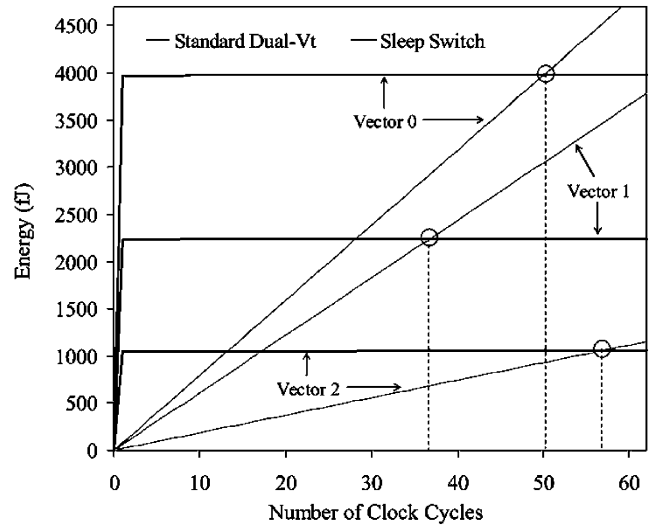


Fig. 9. Cumulative standby energy dissipation of the sleep switch and standard dual- $V_t$  adders for three different input vectors.

nonnegligible energy overhead of the proposed circuit technique must also be assessed to accurately compare the energy characteristics of the two circuit techniques. The cumulative energy dissipated during standby mode by the sleep switch and standard dual- $V_t$  adders is shown in Fig. 9.

The (step) change in energy of the sleep switch characteristics during the first cycle represents the energy overhead for activating the sleep switches (to enter the sleep mode) and for deactivating the sleep switches and recharging the domino gates (to exit the sleep mode). Since the sleep switch circuit technique reduces the standby leakage energy by  $167 \times$  to  $714 \times$  as compared to a standard dual- $V_t$  circuit, the sleep switch characteristics have a significantly smaller slope after the first cycle as compared to the energy characteristics of a standard dual- $V_t$  adder. As discussed previously,  $V_0$  produces the highest leakage state in a standard dual- $V_t$  circuit. Alternatively, the leakage energy of a standard dual- $V_t$  adder is lowest for  $V_2$ . No input combination exists that can place a standard dual- $V_t$  adder into a lower leakage state as compared to a sleep switch dual- $V_t$  adder. Circuit techniques based on the application of a selected input vector to place a circuit into a low leakage state (such as the technique described in [9] and [22]) are, therefore, ineffective for minimizing the leakage of the domino adder discussed in this paper.

As shown in Fig. 9, a minimum of 57 clock cycles is required for the proposed sleep switch circuit technique to provide a net savings in energy as compared to a standard dual- $V_t$  circuit during the standby mode. Although the leakage energy of the standard dual- $V_t$  domino adder is  $167 \times$  to  $714 \times$  higher as compared to the sleep switch adder, a standard dual- $V_t$  circuit technique is preferable in those applications with idle periods shorter than 57 clock cycles.

## V. NOISE IMMUNITY

In a standard domino logic gate, a feedback keeper is employed to maintain the state of the dynamic node against coupling noise, charge sharing, and subthreshold leakage current



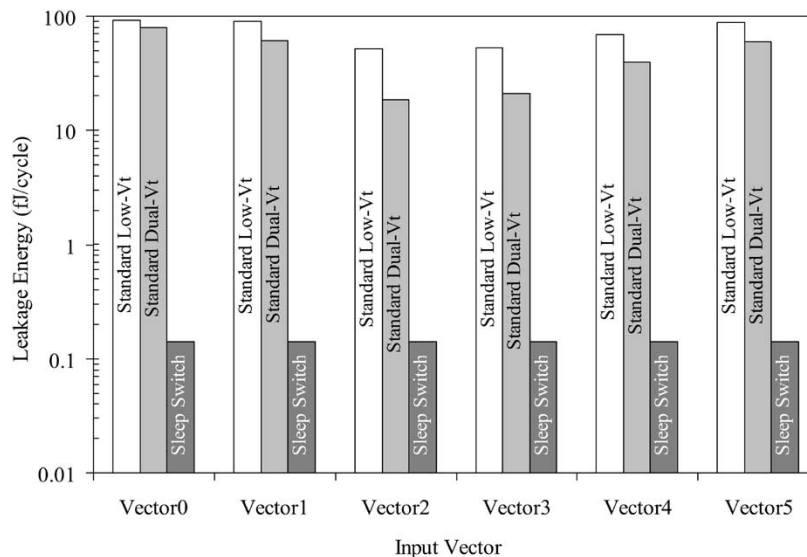


Fig. 10. Under similar noise immunity conditions, a comparison of the leakage energy (per clock cycle) of the adder circuits with the low- $V_t$ , standard dual- $V_t$ , and sleep switch circuit techniques for six different input vectors.

TABLE II  
DEGRADATION IN NOISE IMMUNITY OF STANDARD DUAL- $V_t$  AND SLEEP SWITCH ADDERS AS COMPARED TO THE LOW- $V_t$  ADDER WITH SAME SIZE TRANSISTORS

	Gate	Propagate	Generate	Carry	Sum
Average Reduction in Noise Immunity	Standard Dual- $V_t$	12.2%	14.0%	12.9%	11.3%
	Sleep Switch	12.2%	14.9%	12.9%	11.3%

[23]. In a dual- $V_t$  domino logic circuit, the keeper transistor has a high- $V_t$  [see Figs. 2(b) and 3]. The current supplied by a high- $V_t$  keeper to preserve the state of a dynamic node is reduced, thereby degrading the noise immunity as compared to a low- $V_t$  circuit. The degradation of noise immunity varies for different blocks within an adder.

During evaluation of the noise immunity characteristics, the same noise signal is coupled to all of the inputs of a domino logic circuit as this situation represents the worst case noise condition. In sleep switch circuits, the noise is also assumed to couple to the gates of the sleep transistors. The noise margin criterion used in this paper is similar to the criterion described in [17]. The noise immunity is the voltage amplitude of the DC noise signal that produces a signal with the same amplitude at the output of a domino logic circuit, assuming a 1-GHz clock with a 50% duty cycle. The average degradation in noise immunity for the propagate, generate, carry, and sum domino logic gates is listed in Table II. The degradation in noise immunity of the sleep switch domino logic gates varies between 11.3% and 14.9% as compared to the low- $V_t$  circuits. The effect of the sleep switches on the noise immunity characteristics of the dual- $V_t$  domino logic gates is very small. Sleep switch P and S gates have similar noise immunity as compared to the standard dual- $V_t$  P and S circuits. The noise immunity degradation in the sleep switch G gates as compared to the standard dual- $V_t$  G gates is less than 1.7%.

Both keeper and output inverter sizing are required in a dual- $V_t$  domino logic circuit with a high- $V_t$  keeper transistor in order to provide similar noise immunity as compared to a standard low- $V_t$  domino logic circuit [24]. An alternative

technique for enhanced noise immunity is to employ a low- $V_t$  keeper transistor in a dual- $V_t$  domino circuit. Unless the output inverter is resized, a dual- $V_t$  domino circuit with a low- $V_t$  keeper transistor is not capable of providing noise immunity comparable to a low- $V_t$  domino logic circuit. Under similar noise immunity conditions as compared to the standard low- $V_t$  domino logic circuits, the subthreshold leakage energy savings offered by a dual- $V_t$  circuit technique based on a high- $V_t$  keeper is significantly higher as compared to the leakage savings offered by a dual- $V_t$  circuit technique based on a low- $V_t$  keeper [24]. In this section, therefore, the high- $V_t$  keeper and output inverter pull-down transistor widths of each sleep switch and standard dual- $V_t$  domino gate are increased so as to maintain a similar noise immunity as compared to standard low- $V_t$  gates. A comparison of the subthreshold leakage energy (per clock cycle) of the low- $V_t$ , standard dual- $V_t$ , and sleep switch dual- $V_t$  domino adders under similar noise immunity conditions for different input vectors is shown in Fig. 10. The normalized leakage energy consumption of the low- $V_t$ , standard dual- $V_t$ , and sleep switch adders under similar and degraded noise immunity conditions is listed in Table III.

The subthreshold leakage energy consumed by a standard dual- $V_t$  domino adder is determined by the subthreshold leakage current of the domino gates which are at a high dynamic node voltage state. When the dynamic node voltage is high, the subthreshold leakage current characteristics is virtually independent of the width of the keeper and output inverter pull-down transistors [24]. Keeper and output inverter sizing for enhanced noise immunity, therefore, has little effect on the subthreshold leakage energy consumed by a standard dual- $V_t$  adder, as shown in Figs. 5 and 10.

The dynamic nodes of all of the domino gates in a sleep switch circuit are maintained in a low voltage state. In a dual- $V_t$  domino logic circuit at a low dynamic node voltage state, the subthreshold leakage current strongly depends on the width of the keeper and output inverter pull-down transistors [24]. The subthreshold leakage current in a sleep switch circuit, therefore,

TABLE III  
A COMPARISON OF NORMALIZED SUBTHRESHOLD LEAKAGE ENERGY OF LOW- $V_t$ , STANDARD DUAL- $V_t$ ,  
AND SLEEP SWITCH ADDERS UNDER SIMILAR AND DEGRADED NOISE IMMUNITY CONDITIONS

		$V_0$	$V_1$	$V_2$	$V_3$	$V_4$	$V_5$
Similar Transistor Size Degraded Noise Immunity	Standard Low- $V_t$	830	802	461	473	622	790
	Standard Dual- $V_t$	714	546	167	187	355	535
	Sleep Switch	1	1	1	1	1	1
Transistor Sizing Similar Noise Immunity	Standard Low- $V_t$	660	637	366	376	495	628
	Standard Dual- $V_t$	565	434	132	148	281	425
	Sleep Switch	1	1	1	1	1	1

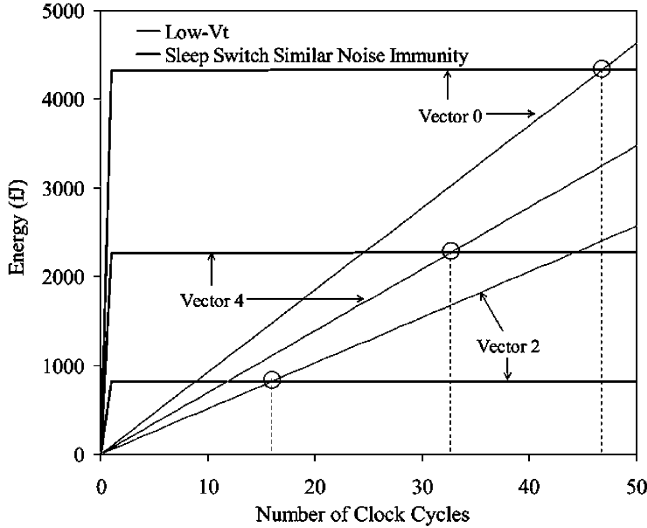


Fig. 11. Under similar noise immunity conditions, cumulative standby energy dissipation of the low- $V_t$  and sleep switch adders for three different input vectors.

increases after keeper and output inverter sizing, degrading the savings in subthreshold leakage energy as listed in Table III. The subthreshold leakage current in the sleep switch adder is  $366 \times$  to  $660 \times$  smaller as compared to the low- $V_t$  adder under similar noise immunity conditions. The subthreshold leakage energy dissipation of the sleep switch dual- $V_t$  adder is  $132 \times$  to  $565 \times$  smaller as compared to the standard dual- $V_t$  adder with similar noise immunity characteristics.

The cumulative energy dissipated in the standby mode by the low- $V_t$  and sleep switch adders under similar noise immunity conditions is shown in Fig. 11. The cumulative energy dissipated in the standby mode by the standard dual- $V_t$  and sleep switch dual- $V_t$  adders providing similar noise immunity characteristics is shown in Fig. 12. The minimum duration of the idle mode required to provide a net savings in the total energy dissipation increases due to the higher subthreshold leakage currents in the sleep switch domino adder after transistor sizing. As shown in Fig. 11, a minimum of 47 clock cycles is required for the sleep switch circuit to provide a net power savings as compared to a standard low- $V_t$  adder during the idle mode. Similarly, as shown in Fig. 12, a minimum of 69 clock cycles is required to provide a net savings in total standby energy consumption as compared to a standard dual- $V_t$  domino adder. The minimum number of clock cycles required for the sleep switch circuit to provide a net savings in total energy during the idle mode, for both similar transistor sizing (degraded noise immunity) and similar noise

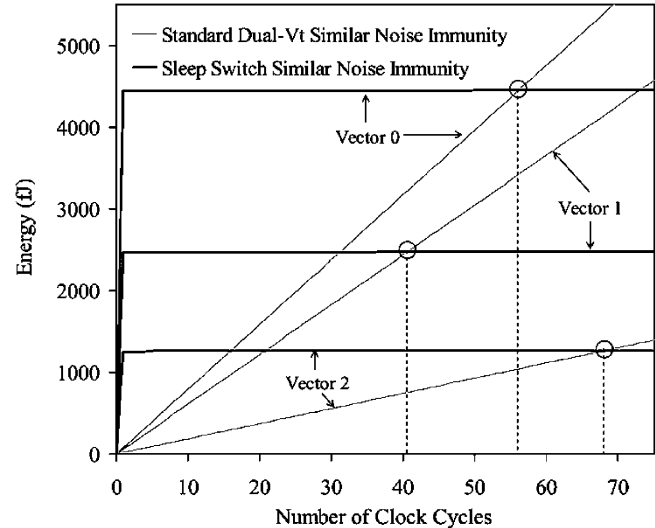


Fig. 12. Under similar noise immunity conditions, cumulative standby energy dissipation of the sleep switch and standard dual- $V_t$  adders for three different input vectors.

TABLE IV  
MINIMUM DURATION OF THE IDLE MODE REQUIRED FOR THE SLEEP SWITCH  
CIRCUIT TECHNIQUE TO PROVIDE A NET SAVINGS IN STANDBY ENERGY AS  
COMPARED TO THE STANDARD LOW- $V_t$  AND DUAL- $V_t$  ADDERS UNDER  
SIMILAR AND DEGRADED NOISE IMMUNITY CONDITIONS

Vector	Minimum Number of Clock Cycles Required			
	Similar Transistor Size Degraded Noise Immunity		Transistor Sizing Similar Noise Immunity	
	Standard Low- $V_t$	Standard Dual- $V_t$	Standard Low- $V_t$	Standard Dual- $V_t$
V0	42	51	47	57
V1	20	37	25	41
V2	6	57	16	69
V3	9	57	19	68
V4	26	56	33	61
V5	23	42	29	47

immunity conditions (increased keeper and output inverter pull-down transistor size), is listed in Table IV.

## VI. CONCLUSIONS

A circuit technique is proposed for reducing the standby leakage energy consumption of domino logic circuits. The proposed circuit technique employs sleep switches and a dual threshold voltage CMOS technology in order to place an idle domino logic circuit into a low leakage state, without degrading the delay and power characteristics during the active mode. A dual threshold voltage domino circuit enters and leaves the

sleep mode within a single clock cycle with the sleep switch circuit technique.

The sleep switch circuit technique reduces the leakage energy by up to  $830 \times$  as compared to a standard low- $V_t$  circuit. The circuit technique also reduces the active mode delay and power by up to 21% and 14.6%, respectively, as compared to a low- $V_t$  circuit.

Existing techniques based on the application of a selected input vector to place a dual- $V_t$  circuit into a low leakage state are ineffective for minimizing the subthreshold leakage currents in multiple stage domino circuits with inverted internal signals. The sleep switch circuit technique exploits the full effectiveness of a dual- $V_t$  CMOS technology to reduce subthreshold leakage current by strongly turning off all of the high- $V_t$  transistors, independent of the input signals. The sleep switch circuit technique reduces the leakage energy by up to  $714 \times$  as compared to a standard dual- $V_t$  circuit. The energy overhead of the circuit technique is low, justifying the use of the proposed sleep scheme during idle periods as short as 57 clock cycles in order to reduce standby leakage energy.

The noise immunity of the circuit blocks within a dual- $V_t$  domino adder is degraded by up to 14.9% as compared to a low- $V_t$  domino adder. The keepers and output inverter pulldown transistors are sized to provide similar noise immunity as compared to a low- $V_t$  adder. Under similar noise immunity conditions, the subthreshold leakage energy consumed by a sleep switch adder is up to  $660 \times$  and  $565 \times$  smaller as compared to a standard low- $V_t$  and dual- $V_t$  adder, respectively. A minimum of 47 and 69 clock cycles is required for the sleep switch circuit to provide a net savings in total energy consumption during the idle mode while providing similar noise immunity characteristics during the active mode as compared to a standard low- $V_t$  and dual- $V_t$  domino adder, respectively.

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