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Slew-Rate and Gain Enhancement in Two Stage Operational Amplifiers

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***Abstract*—A two stage op-amp with an effective technique to enhance slew-rate and gain is presented. The enhancement is provided by an auxiliary monitor circuit which is activated in slewing conditions, but can contribute to the gain in normal conditions. The amplifier, simulated in a 0.18 μm technology, achieves 74 dB DC gain, 160 MHz bandwidth and 26.8 V/μs slew-rate for a load capacitance of 1.75 pF with 362 μW power consumption, considering a supply voltage of 1.8 V.**

I. Introduction

The continuous market expansion for portable systems, such as wireless communication devices, consumer electronics, etc., requires more and more circuits operating in low power mode and with low supply voltages. When designing an op-amp, there is an intrinsic performance trade-off between gain and bandwidth. An high gain is usually achived by cascoding or by using multistage architectures operating at low bias current. The main drawback of the cascoding approach is the reduction in the output signal swing. In addition, the output swing performance is further limited when using low supply voltages with modern technologies. However, with multistage amplifiers, the output signal swing can be increased, but, for stability reasons, the number of stages is limited at two, [1]. For some applications, the op-amp drives large capacitive loads, thus requiring large currents in the output stage. In order to improve the power effectiveness, published circuit techniques dynamically increase the slew-rate, thus keeping low the quiescent current without using class AB solutions, [2-4].

This paper uses an auxiliary stage to enhance the slew-rate similarly to other published schemes (Section II), but it obtains higher effectiveness and also boosts the gain and the bandwidth of the op-amp. Section III describes the design of the slew-rate monitor circuit; Sections IV and V discuss how the auxiliary monitor circuit can be used to improve the main op-amp gain and slew-rate. The circuit has been designed at the transistor level with a 0.18 μm technology and simulation results (Section VI) demonstrate the effectiveness of the approach.

II. Conventional Solutions

Very few slew-rate enhancement techniques in single or two-stage amplifiers have been addressed in the open literature and all the presented methods are based on the diagram of Fig. 1. Basically, there is an additional auxiliary block, driven by the input signal, which monitors the slewing conditions of the op-amp and boosts the slewing performance.

Reference [5] is for a single-ended scheme which uses an extra differential pair. The latter generates two differential output currents that are zero in normal operation. In slewing, one of the currents is directly injected into the output node. For slewing in the opposite direction, the complementary current boosts the driving voltage of the current source, thus resulting in an asymmetrical improvement of the slewing.

The solution proposed in [6] is for a complex architecture that uses a telescopic cascode in the first stage. The structure aims at obtaining a very high gain, but it is not suitable for low voltage applications. Also, the proposed slew-rate boost is effective in only one direction, which limits its use to special situations.

The main op-amp of the reference [7] is a folded-cascode with extra current pumped into the load capacitance during slewing conditions. For low voltage applications, the folded-cascode scheme becomes problematic because of the limited output swing. Therefore, the solution is only suitable for moderate output dynamic range requirements.

III. Slew-Rate in Two Stage Op-Amps

Two stage amplifiers fulfill moderate gain and high output swing requirements, but the most challenging issues are imposed by the power consumption and by the slew-rate performance limited by the compensation capacitor. One of the possible solutions is to increase the quiescent current of the amplifier, but this leads to a power consumtion penalty.

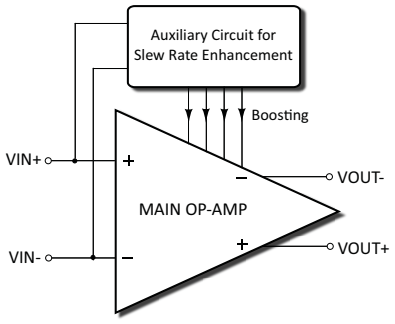

Fig. 1. General block diagram of an op-amp wih slew-rate enhancement.

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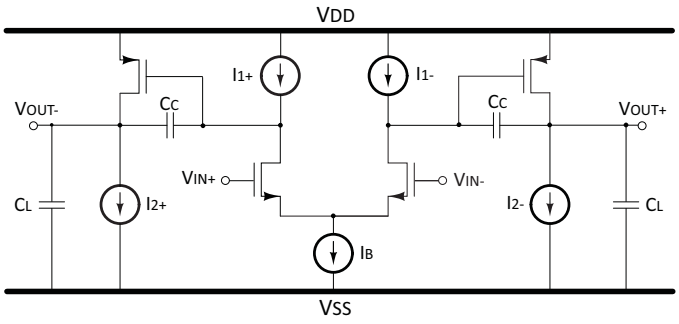

Fig. 2. Conventional fully differential two stage amplifier.

The slew-rate of a two stage fully differential amplifier, schematically indicated in Fig. 2, is limited by the maximum current of the current sources. During positive slewing ($V_{IN+} > V_{IN-}$), the current through C_C is limited by $I_B - I_{1+}$ while, in the other half circuit, the current through C_C is limited by I_{1-}. In the meantime, I_{2-} must discharge (C_C+C_L). For an optimal slewing operation of a conventional two stage amplifier, it is necessary to have

$$I_2 = I_1 \left(\frac{C_C + C_L}{C_C} \right), 2I_1 = I_B. \tag{1}$$

Therefore, for slew-rate enhancement, it is necessary to have a slew-rate monitor, which boosts output current sources I_{1+}, I_{2+} and I_B in one case, and I_{1-}, I_{2-} and I_B in the other direction. When considering to use a slew-rate enhancement circuit, condition (1) is not strictly necessary anymore since the auxiliary circuit provides the current required to improve the slew-rate. Suppose, for example, to increases the slew-rate by a factor k; generators I_B and I_1 must be supported by an extra current of $I_{BOOST} = (k-1)I_1$, while the current source I_2 needs an extra current of

$$I_1(k-1) \left(\frac{C_C + C_L}{C_C} \right) \tag{2}$$

Therefore, since the faster discharge of (C_C+C_L) is sustained by the extra boosting current, the current in the second stage can be optimum for gain and speed.

IV. Slew-Rate Monitor

Fig. 3 shows the used slew-rate monitor. A differential pair, M_{a1} and M_{a2}, injects its current in two diode connected transistors, M_{a5} and M_{a6}. The extra current generators αI_m adjust the quiescent current in M_{a5} and M_{a6}. By inspection of the circuit, in the quiescent conditions, I_{Ma5}=I_{Ma6}=(α-1/2)I_m. If $\alpha > 0.5$ the current is zero. There are four outputs, two for boosting the slewing of n-channel devices (V_A and V_C) and two for p-channel transistors (V_B and V_D).

When the input differential signal is large, the pair delivers the entire bias current I_m toward one of the two diode connected elements and obtains a significant boost of the output control even thanks to a possibly large output mirror factor. Indeed, it has to be distinguished between two cases: $\alpha > 0.5$ and $\alpha \leq 0.5$. In the former case, the output current in the quiescent condition is zero and a minimum unbalance is required for a boosting signal. The maximum current in the diode connected transistors is $(1-\alpha)I_m$, but, since the quiescent current is zero, the mirror factor can be very large. However, switching transistors from the off to the on state causes a delay that limits the boost speed.

If $\alpha \leq 0.5$ the quiescent current in the diode connected elements is $(1/2-\alpha)I_m$. A full unbalance brings this current to $(1-\alpha)I_m$ with a relative increase by $(1-\alpha)/(1/2-\alpha)$. Therefore, if $\alpha = 0.3$ the current increases by 3.5, a good figure for practical cases. An important advantage of the case $\alpha \leq 0.5$ is the signal term in the boost quiescent current that, depending on its use, possibly enhances the gain.

The slew rate monitor uses the bias current I_m that, obviously, increases the consumed power.

Fig. 4 shows the slew-rate monitor response for different values of α. For $\alpha = 0.5$, the output current is zero in quiescent conditions and starts rising when the differential signal is larger that 10 mV differential. The output current reaches its maximum $I_m/2$ for large unbalance. With $\alpha = 0.25$ the current in the diode connected transistors ranges from $0.25I_m$ to $0.75I_m$ in the slewing status. The other displayed case is for $\alpha = 0$

A. Use of the Slew-Rate Monitor in the Two Stage OTA

As mentioned above, for improving the slew-rate it is necessary to increase the currents indicated with the symbols I_1, I_2 and I_B in Fig. 2. Therefore, for the slewing situation depicted in Fig. 5, it is necessary to provide extra currents as shown in the bottom part of the figure. This is done with additional transistors that operate as current sources biased with the two boosted signals generated by the auxiliary circuit.

In quiescent conditions, the possible current from the auxiliary section is equivalent to a bias component; therefore, the regular current sources can be diminished or, at the limit, brought to zero. Moreover, the signal components possibly enhance the small signal gain. By inspection of the circuit it results that a signal in parallel to I_B is ineffective, being a common-mode component. A signal added to I_2 is irrelevant being injected in the output nodes. On the contrary, a signal in parallel to I_1 contributes as $g_{m,in}v_{in}$ does and boosts the

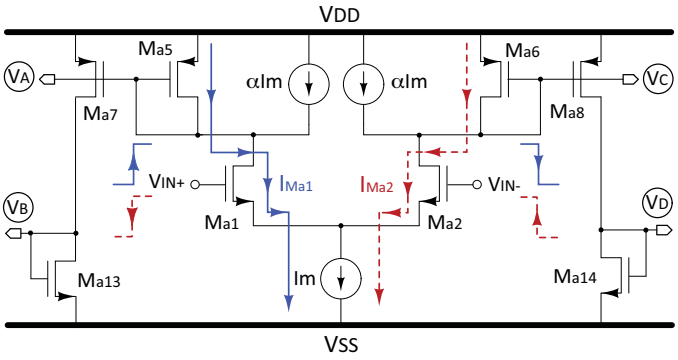

Fig. 3. Schematic diagram of the proposed auxiliary slew-rate monitor circuit.

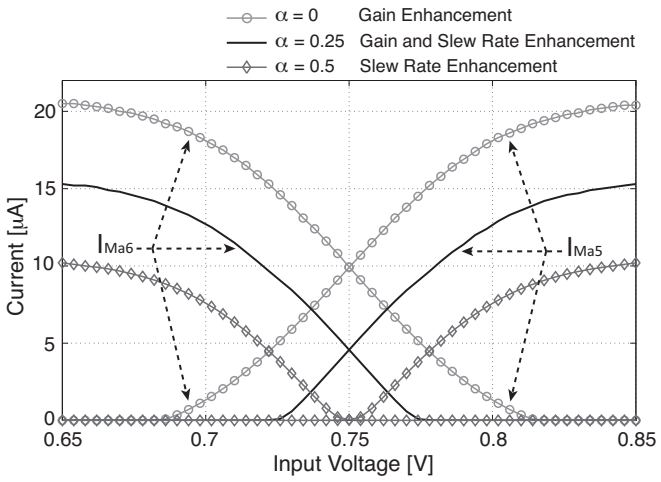

Fig. 4. Simulated slew-rate monitor circuit response for different α.

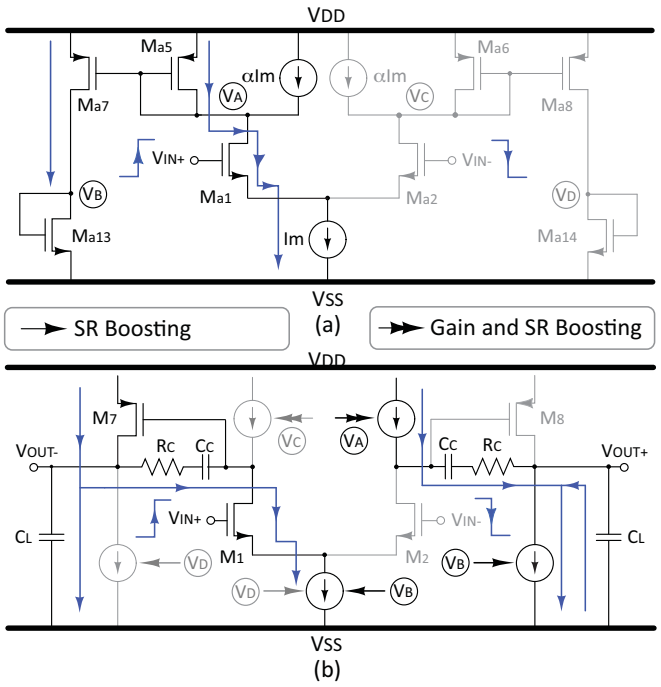

Fig. 5. Slew-rate behavior of a two stage op-amp for $V_{IN+} > V_{IN-}$. (a) Auxiliary monitor circuit. (b) Main circuit.

gain as outlined in the scheme.

B. Gain Boost Benefit

The circuit diagram of the complete op-amp is shown in Fig. 6. The main amplifier uses four more n-channel transistors in parallel with the current sources M_7, M_8 and M_9. The current in the differential pair is enhanced for slewing in both directions, while M_7 and M_8 are alternately intensified. The controls for the n-channel boost uses a larger mirror factor to allow a scaling of the current in the second stage. At this purpose, the auxiliary circuit drains a fraction of the current that mirror the p-channel output and diminishes its quiescent value. For the sake of simplicity the same controls augment

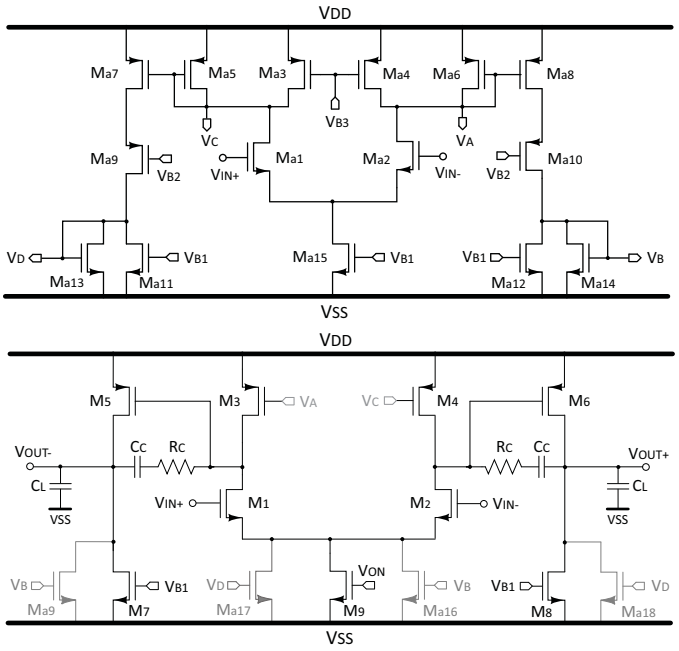

Fig. 6. Schematic diagram of the complete op-amp (monitor circuit at the top, main circuit at the bottom).

the differential pair current. The p-channel current sources of the main op-amp are directly driven by the boost controls with their quiescent current suitably regulated by proper mirror factors.

The circuit uses $\alpha = 0.3$; therefore, the gain increases thanks to the signal current injected through the P-channel auxiliary inputs. By inspecting the circuit, the transconductance gain of the auxiliary path is

$$g_{aux} = \frac{g_{m,a1}}{g_{m,a5}} \frac{(W/L)_3}{(W/L)_{a5}} g_{m,3} = g_{m,3} k \tag{3}$$

being k a gain boost design parameter.

The auxiliary transconductance added to the input transconductance $g_{m,1}$ obtains an input enhanced transconductance

$$g'_{m,1} = g_{m,1} \left[1 + k \frac{g_{m,3}}{g_{m,1}} \right]; \tag{4}$$

therefore, the factor in brackets gives the gain increase.

The used circuit can be represented by the small signal equivalent circuit in Fig. 7 where the first stage has, actually,

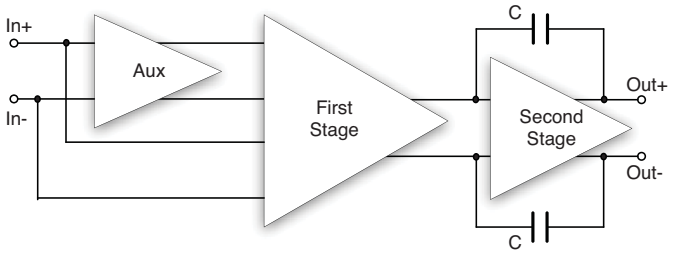

Fig. 7. Equivalent nested configuration of the proposed circuit.

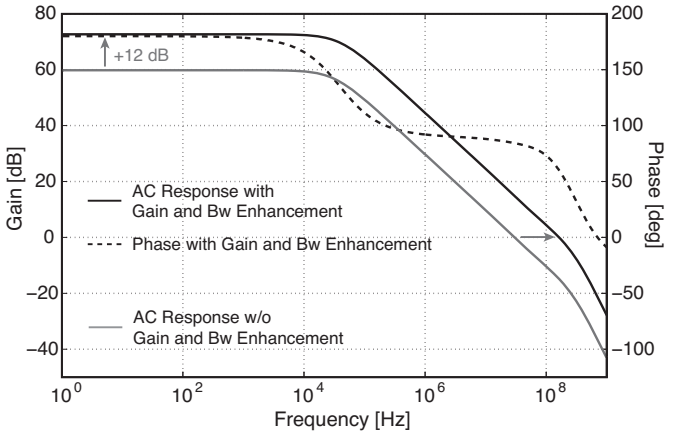

Fig. 8. AC response of the amplifier (X axis is in log scale).

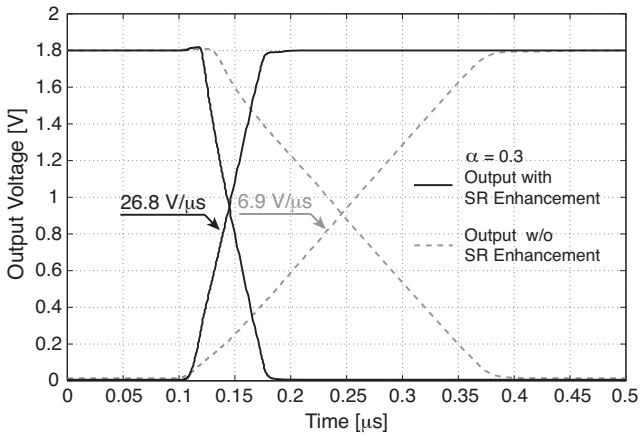

Fig. 9. Simulated slew-rate response.

four inputs, the main n-channel and the auxiliary p-channel that are controlled by the auxiliary amplifier in a nested configuration, [8]. Therefore, the stability of the circuit is not significantly affected as it happens for nested architectures.

V. Simulation Results

The circuit of Fig. 6 has been simulated by using a 0.18-μm standard CMOS technology with 1.8 V supply voltage. Fig. 8 compares the amplifier responses with and without gain boost. The gain increases by 12 dB and the bandwidth also augments by the same factor. In order to achieve a good phase margin, the compensation capacitor must be increased from 0.5 pF to 1.5 pF. This increase partially limits the benefit of the slewing enhancement because of the larger compensation element.

The slewing responses with a 1.75 pF load are compared in Fig. 9. The figure outlines a slew-rate improvement by approximately 3.7 times (from 6.9 to 26.8 V/μs). Table I summarizes the performance of the amplifier with and without booster. As expected, the power of the boosted scheme is higher than the one of the conventional circuit. However, a proper trimming of the mirror factors enables a good reduction of the current in the second stage of the op-amp. The performance are unchanged while the total consumed power is only 4% more than the conventional counterpart.

VI. Conclusions

The proposed slew-rate boosting technique also obtains an increase of gain and bandwidth; a proper design optimization significantly reduces the extra power needed. The benefits of the proposed method can be quantified by two figures of merit, defined in [6], that measure the power effectiveness in achieving bandwidth and slew-rate

$$FoM_{BW} = \frac{f_T.C_L}{P_{tot}}; \quad FoM_{slew} = \frac{SR.C_L}{P_{tot}} \qquad (5)$$

where f_T is measured in MHz, the capacitance in pF, the slew-rate in $V/\mu s$ and the power in mW. A table of state-of-the-art results given in [6] shows that the best FoM_{BW} obtained is equal to 423. This design obtains $FoM_{BW} = 772$. For the FoM_{slew}, the best figure reported in [6], with two values recalculated on the basis of the figures provided in the original papers, is 102; this design achieves 129.

TABLE I
Op-amp Performance
Power Supply = 1.8 V, C_L = 1.75 pF, α = 0.3

Parameter	SR+ [V/μs]	SR- [V/μs]	Gain [dB]	BW [MHz]	Power [μW]
Without Boost	6.9	6.9	60	40.1	350
With Boost	26.8	26.6	72	160	477
Boost with Power Optim.	26.7	26.6	74	160	362

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References

[1] F. Maloberti, "Analog Design for CMOS VLSI Systems", Kluwer Academic Publishers, Dordrecht, 2001, ISBN 0792375505.

[2] R. Klinke, B.J. Hosticka, and H. Pfleiderer, "A Very High Slew-Rate CMOS Operational Amplifier", *IEEE Journal of Solid-State Circuits*, vol. 24, pp. 744-746, June 1989.

[3] H. Lee and P.K.T. Mok, "A CMOS Current-Mirror Amplifier with Compact Slew Rate Enhancement Circuit for Large Capacitive Load Applications", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 220-223, May 2001.

[4] H. Lee and P.K.T. Mok, "Single-Point Detection Slew-Rate Enhancement Circuits for Single-Stage Amplifiers", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 831-834, May 2002.

[5] K. Nagaraj, "Slew Rate Enhancement Technique for CMOS Output Buffers", *Electronics Letters*, vol. 25, no. 19, pp. 1304-1305, Sept. 1989.

[6] H. Y. Huang, B. R. Wang and J. C. Liu, "High-Gain and High-Bandwidth Rail-toRail Operational amplifier with Slew Rate Boost Circuit", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 906-910, May 2006.

[7] H. Huang and E. I. El-Masry, "A Fast Settling CMOS Operational Amplifier", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, Vol. 1, pp. I-265-I-268, May 2003.

[8] A. Thomsen, D. Kasha, and W. Lee, "A Five Stage Chopper Stabilized Instrumentation Amplifier Using Feedforward Compensation", *Symposium on VLSI Circuits Dig. Tech. Papers*, pp. 220-223, June 1998.