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Sliding-Mode Control Strategy for Three-Phase Three-Level T-Type Rectifiers With DC Capacitor Voltage Balancing

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ABSTRACT A sliding mode control (SMC) strategy with dc capacitor voltage balancing is proposed for three-phase three-level T-type rectifiers. The proposed SMC strategy is designed in the *abc* frame rather than the *dq* frame. In this case, the necessity of three-phase current transformations is eliminated. The proposed SMC is based on the errors of the line currents. The amplitude of line current references is generated by controlling the dc voltage using a proportional-integral (PI) controller. In order to obtain unity power factor, the generated reference amplitude is multiplied by the corresponding sinusoidal waveform obtained from the phase locked loop (PLL) operating with grid voltages. The dc capacitor voltage balancing is achieved by adding a proportional control term into the line current reference obtained for each rectifier leg. The performance of the proposed control strategy is validated by simulations and experiments during steady-state, transients caused by load change, and unbalanced grid conditions. The results show that the proposed control strategy offers excellent steady-state and dynamic performances with low THD in the line currents, zero steady-state error in the output voltage, and very fast dynamic response.

INDEX TERMS Three-level T-type rectifier, proportional-integral control (PI), sliding mode control.

I. INTRODUCTION

Three-phase ac-dc rectifiers are widely employed in various industrial applications due to their advantages such as controllable dc-link voltage, sinusoidal line currents with reasonably low total harmonic distortion (THD), and unity power factor. There are two types of rectifiers: current-source type [1] and voltage-source type [2]. While a three-phase two-level current-source type rectifier uses six unidirectional switches, a three-phase two-level voltage-source rectifier uses six bidirectional switches. However, the voltage-source rectifier topology is very popular due to its simple structure and ease of control [2]–[5]. In order to achieve dc voltage control, sinusoidal line currents with low THD and unity power factor, the two-level rectifiers should be operated with high switching frequencies. However, this would increase acoustic noise and switching losses. The acoustic noise can be reduced at the expense of increasing the volume and weight of the passive components. On the other hand, the performance of a two-level rectifier is not good at medium and high voltages.

In the last two decades, multilevel converters are emerged as an alternative topology to be employed at medium and high voltage levels [6]. As in the case of two-level converters, voltage-source based multilevel converters are more popular which can be categorized as neutral point clamped (NPC) [7]–[9], flying capacitor (FC) [10], cascaded H-bridge (CHB) [11], packed-U-cell (PUC) [12], T-type [13], and hybrid type [14]–[16].

Among these multilevel converter topologies, the T-type converter merits attention due to its significant advantages such as low switching losses, reduced component count, better efficiency and reduced control complexity. If the efficiency and cost are important, then a T-type converter is a good choice in low voltage applications rather than an NPC converter [17]. Also, the T-type converter topology

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has reduced component count compared to three-level NPC converter topology in [18]. Comparing NPC- and T-type converters, one can see that both topologies use four switches in one converter leg. However, unlike the T-type converters, the NPC converters need additional two clamping diodes per converter leg. The clamping of neutral point to positive or negative dc voltages is achieved by the clamping diodes in an NPC converter. In a T-type converter, an active bidirectional switching device connected between the midpoint of each converter leg and midpoint of series connected dc-link capacitors is used to achieve this voltage clamping. Hence, the T-type converters have reduced component count than the NPC converters which implies that T-type converters have smaller losses than that of NPC-type converters [17].

In spite of attractive features of multilevel converters, the dc capacitor voltage balancing is essential which increases the controller complexity. In [7], the dc capacitor voltage balancing is accomplished via predictive control strategy for an NPC-type rectifier. The authors in [8] proposed a modulation strategy to balance the capacitor voltages in an NPC-type rectifier. However, the regulation of dc voltage and line currents can be achieved by employing three proportional-integral (PI) controllers. In [9], an H_∞ controller is proposed to balance the dc capacitor voltages of an NPC-type rectifier. It is reported that the control of an NPC-type rectifier requires three control loops, namely, instantaneous power tracking loop, dc voltage regulation loop, and dc capacitor voltage balancing loop. The objective of instantaneous power tracking loop is to achieve instantaneous active and reactive power tracking. The objective of the dc voltage regulation loop is to ensure output voltage regulation such that that the sum of dc capacitor voltages is equal to the reference output voltage. Finally, the voltage balancing loop eliminates the imbalance between the dc capacitor voltages. Similar requirements also exist in FC-type rectifier [10], and CHB-type rectifier [11]. Although the PUC-type rectifier topology is the simplest topology among the multilevel rectifier topologies, but it is not mature yet and did not find any application in the industry due to its complicated control structure [12].

In the last few years, three-level T-type rectifiers are increasingly stuided in the literature [13], [19]–[27]. In [13] and [19], open-switch fault detection and tolerance control techniques are proposed to improve the reliability of the three-level T-type rectifier during an open-switch fault. In [20], open-switch fault tolerance control methods are compared. In [21], a proportional-resonant (PR) control is used to damp the resonance in the LLCL filter. Although the T-type converter topology exists in the literature more than one decade, there are not many studies addressing its application as rectifier. The other studies devoted for three-level T-type rectifiers are based on EMI filter size minimization [22], improved modulation scheme for neutral-point potential balancing and circulating current suppression [23], and carrier-based [24] and open-circuit [19] fault-tolerant control methods with neutral-point voltage oscillations suppression. The authors in [25] proposed predictive observer based control method for single-phase T-type rectifier. Although the proposed method exhibits good performance, its implementation is complicated. Furthermore, it is sensitive to the system parameters.

Since T-type rectifier is emerged a few years ago, its control is not studied extensively. In this study, sliding mode control (SMC) of three-phase three-level T-type rectifier is proposed. The main advantages of SMC include fast dynamic response, easy implementation, robustness against disturbances and variations in the system parameters. Although the SMC is recognized as one of the popular and powerful control tools in wide range of power converters [28]–[32], its adoption for T-type rectifiers is found only in [33] where the dynamic response is fast and unity power factor operation is accomplished satisfactorily. However, the presented SMC is sensitive to the disturbances. Furthermore, steady-state error exists in the dc voltage. On the other hand, the proposed SMC is fundamentally different from the existing SMC methods which are generally based on a state variable and its derivative.

In this study, a SMC strategy is proposed to regulate the dc voltage, achieve the line current control and dc capacitor balancing control. While dc voltage control is accomplished by a PI controller, the line currents are controlled by SMC in the *abc* frame. The formulation of the proposed SMC is intentionally made in *abc* frame to eliminate the transformations that would be needed in the *dq* frame. The reference amplitude of the line currents is produced by the PI controller. The produced reference amplitude is then multipled with the corresponding sinusoidal waveforms which are generated via a phase locked loop (PLL) synchronized with the grid voltages. The waveforms obtained from each multiplication are used as reference line current for each phase. The imbalance between dc capacitor voltages are eliminated by adding the dc capacitor voltage error with the reference line current for each phase. Simulation and experimental results are presented to confirm the validity and effectiveness of the proposed SMC method.

II. OPERATION PRINCIPLE OF A T-TYPE RECTIFIER

Fig. 1 shows the circuit diagram of three-phase three-level T-type rectifier which consists of four switches per leg. Similar to the conventional two-level rectifiers, the inductor L connected between grid and midpoint of each phase achieves boost operation. The resistance of inductor is denoted by R and capacitors are represented by C_1 and C_2.

Considering the combination of switching states, the rectifier can produce three different pole voltages v_{kO} ($k = a, b, c$) which exist when the midpoint of each leg is connected to positive (P), neutral (O) and negative (N) points. Table 1 shows the operating states, switching states and generated pole voltage levels. When the switches S_{1k} and S_{2k} are turned ON and S_{3k} and S_{4k} are turned OFF, the rectifier operates in the P state which produces pole voltage equal to $v_{kO} = V_{dc}/2$. On the other hand, when S_{2k} and S_{3k} are turned

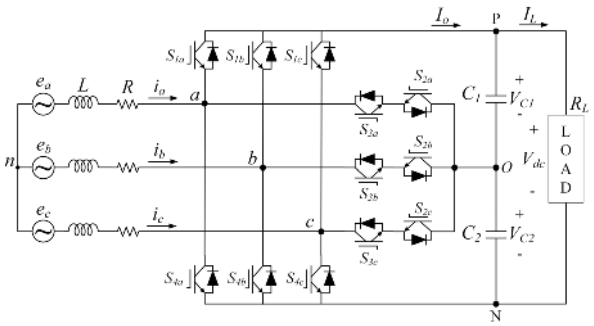


FIGURE 1. Three-phase three-level T-type rectifier.

TABLE 1. Operating states, switching states and pole voltages.

Operating State	S_{1k}	S_{2k}	S_{3k}	S_{4k}	v_{kO}
P	ON	ON	OFF	OFF	$V_{dc}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	$-V_{dc}/2$

ON and S_{1k} and S_{4k} are turned OFF, the rectifier operates in the O state producing pole voltage equal to 0V. Finally, when S_{1k} and S_{2k} are turned OFF and S_{3k} and S_{4k} are turned ON, the rectifier is in the N state which produces pole voltage $v_{kO} = -V_{dc}/2$. Hence, by using different switching combinations a five-level $(0, \pm V_{dc}/2, \pm V_{dc})$ line-to-line voltage can be produced.

III. MODELING OF T-TYPE RECTIFIER

Operation of the rectifier can be described by the following ac-side equation [34]

$$\mathbf{e} = L\frac{d\mathbf{i}}{dt} + R\mathbf{i} + \mathbf{v} \tag{1}$$

where

$$\mathbf{e} = \begin{bmatrix} e_a & e_b & e_c \end{bmatrix}^{\mathrm{T}}, \quad \mathbf{i} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^{\mathrm{T}}, \ \mathbf{v} = \begin{bmatrix} v_{an} & v_{bn} & v_{cn} \end{bmatrix}^{\mathrm{T}} \tag{2}$$

The three-phase grid voltages are defined as

$$e_a = E_m \cos(\omega t) \tag{3}$$
$$e_b = E_m \cos(\omega t - 2\pi/3) \tag{4}$$
$$e_b = E_m \cos(\omega t + 2\pi/3) \tag{5}$$

where E_m denotes the amplitude of the grid voltages. The voltages v_{an}, v_{bn}, and v_{cn} are expressed as

$$v_{an} = v_{aO} + v_{On} \tag{6}$$
$$v_{bn} = v_{bO} + v_{On} \tag{7}$$
$$v_{cn} = v_{cO} + v_{On} \tag{8}$$

Applying Kirchhoff's current law at the positive terminal of load and neutral-point, one can find the following dc-side equations

$$C_1\frac{dV_{C1}}{dt} = I_0 - I_L \tag{9}$$

$$C_2\frac{dV_{C2}}{dt} = C_1\frac{dV_{C1}}{dt} + I_n \tag{10}$$

$$I_n = C_2\frac{dV_{C2}}{dt} - C_1\frac{dV_{C1}}{dt} = C\frac{dv_e}{dt} \tag{11}$$

where I_n is the neutral-point current, $v_e = V_{C2} - V_{C1}$ is the dc capacitor voltage error. It is assumed that $C = C_1 = C_2$. Equation (11) implies that dc capacitor voltage error is influenced by the neutral-point current I_n.

As explained in Introduction, there are three control objectives for three-level T-type rectifier. These objectives are regulation of dc voltage (V_{dc}), control of line currents such that they are in phase with the corresponding grid voltages (achievement of unity power factor) and compensation of imbalance between dc capacitor voltages. Hence, there should be totally four loops in the controller.

IV. DESIGN OF CONTROL STRATEGY

A. OUTPUT VOLTAGE CONTROL AND REFERENCE LINE CURRENT GENERATION

The control of output dc voltage is achieved by a PI controller. It is well known that PI controllers offer good dynamic response as well as zero steady-state error in controlling a dc quantity. In this study, the PI controller processes output voltage error $(V_{dc}^* - V_{dc})$ and produces the reference amplitude of the line currents as

$$I^* = K_p(V_{dc}^* - V_{dc}) + K_i \int (V_{dc}^* - V_{dc})dt \tag{12}$$

where V_{dc}^* is the reference of V_{dc}, K_p is the proportional gain and K_i is the integral gain. In order to achive the unity power factor operation, the actual three-phase line currents must be in phase with the corresponding grid voltages. In the proposed controller, the use of reference line currents is essential. The sinusoidal signals synchronized with the grid voltages are obtained by using PLL. Then, the reference line current for each phase can be produced by multiplying the corresponding sinusoidal signals with I^* as follows

$$i_a^* = I^* \cos(\omega t) \tag{13}$$
$$i_b^* = I^* \cos(\omega t - 2\pi/3) \tag{14}$$
$$i_c^* = I^* \cos(\omega t + 2\pi/3) \tag{15}$$

B. DC CAPACITOR VOLTAGE BALANCING

As mentioned in Section I, the balancing of dc capacitor voltages is essential in the three-level T-type rectifier. It should be noted that this voltage balancing requirement is not only necessary for the T-type rectifiers, but also required for other multilevel rectifier topologies. The objective is to eliminate the dc value in v_e. When I_n is positive, while V_{C1} is decreased, V_{C2} is increased (see equation (11)). Similarly, when I_n is negative, while V_{C1} is increased, V_{C2} is decreased. In this study, this fact is used to achieve $v_e = 0$ V which balances the dc capacitor voltages. The neutral-point current is expressed in terms of line currents as follows [35]

$$I_n = d_a i_a + d_b i_b + d_c i_c \tag{16}$$

where d_k is the on-time duty cycle for each phase. Hence, considering (11) and (16), one can see that v_e is influenced by the line currents. Therefore, if the reference line currents in (13)-(15) are modified with a feedback control term which involves v_e, then the variations in v_e will be eliminated when the line currents track their references.

Now, let the reference line currents in (13)-(15) are modified as follows

$$i_{am}^* = I^* \cos(\omega t) + K_e v_e \tag{17}$$
$$i_{bm}^* = I^* \cos(\omega t - 2\pi/3) + K_e v_e \tag{18}$$
$$i_{cm}^* = I^* \cos(\omega t + 2\pi/3) + K_e v_e \tag{19}$$

where $K_e v_e$ is the feedback control term generated by a proportional controller with a gain K_e which is less than zero for stability. In this case, the line currents will track i_{km}^* ($i_{am}^*, i_{bm}^*, i_{cm}^*$) instead of i_k^* (i_a^*, i_b^*, i_c^*). Clearly, i_{km}^* decreases when $v_e > 0$ and increases when $v_e < 0$. Assuming that the line current control is accomplished ($i_k = i_{km}^*$) successfully, then the value of v_e is made zero by the proportional control loop in the steady-state. This fact can be shown mathematically as follows. Assuming that the line currents track their references ($i_k = i_{km}^*$) and using (11), equation (16) can be written as

$$\frac{dv_e}{dt} = \frac{1}{C}\left(d_a i_a^* + d_b i_b^* + d_c i_c^*\right) + \frac{1}{C}\left(d_a + d_b + d_c\right) K_e v_e \tag{20}$$

Since $\frac{1}{C}\left(d_a i_a^* + d_b i_b^* + d_c i_c^*\right) = 0$ in a balanced three-phase system, then (20) reduces to

$$\frac{dv_e}{dt} = \frac{1}{C}\left(d_a + d_b + d_c\right) K_e v_e \tag{21}$$

It is evident that (21) is a first-order differential equation whose solution is given by

$$v_e(t) = v_e(0) e^{\lambda t} \tag{22}$$

where $\lambda = (d_a + d_b + d_c)\frac{K_e}{C}$. Since $(d_a + d_b + d_c) > 0, C > 0$, and $K_e < 0$, then $v_e(t)$ converges to zero.

C. LINE CURRENT CONTROL USING SMC

In this study, the line current control is achieved by using sliding mode control. Now, let the sliding surface functions be defined as follows

$$\sigma_a = i_a - i_{am}^* \tag{23}$$
$$\sigma_b = i_b - i_{bm}^* \tag{24}$$
$$\sigma_c = i_c - i_{cm}^* \tag{25}$$

The modulating signals are sliding surface functions (σ_a, σ_b, σ_c) which are compared with level shifted triangular carrier signals to produce the required pulse width modulation (PWM) signals. The sliding mode occurs if the existence conditions are satisfied. Generally, existence conditions are derived from the sliding surface function (σ_k) and its derivative which should have opposite signs around the sliding line. Hence, the sliding mode is stable if the following condition holds [36], [37]

$$\sigma_k \frac{d\sigma_k}{dt} < 0 \tag{26}$$

Now, let us show that the condition in (26) holds for phase a. Substituting the derivative of (23) into (26) gives

$$\sigma_a \left(\frac{di_a}{dt} - \frac{di_{am}^*}{dt}\right) < 0 \tag{27}$$

Since I^*, V_{C1} and V_{C2} are constant in the steady-state, then the derivative of (17) can be written as

$$\frac{di_{am}^*}{dt} = -\omega I^* \sin(\omega t) \tag{28}$$

The expression for di_a/dt can be derived from (1) as follows

$$\frac{di_a}{dt} = \frac{1}{L}\left(E_m \cos(\omega t) - R i_a - v_{an}\right) \tag{29}$$

Now, substituting (28) and (29) into (27) and assuming that line current tracks its reference ($i_a = i_{am}^*$), we obtain

$$\sigma_a \left(\sqrt{(E_m - RI)^2 + (\omega L I)^2}\cos(\omega t + \theta) - v_{an}\right) < 0 \tag{30}$$

where phase shift θ is given by

$$\theta = \tan^{-1}\left(\frac{-\omega L I}{(E_m - RI)}\right) \tag{31}$$

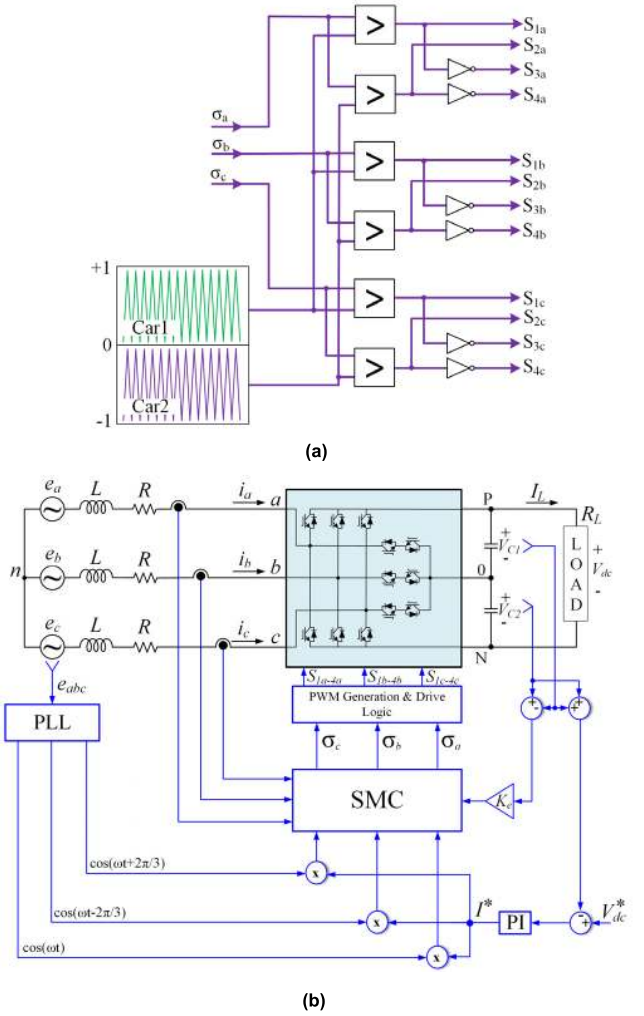
Equation (30) can be rewritten as

$$\sqrt{(E_m - RI)^2 + (\omega L I)^2}\cos(\omega t + \theta) < v_{an} \tag{32}$$

It is worth noting that the three-level T-type rectifier under consideration is a boost type rectifier which means that its output voltage is always greater than its input voltage. The voltage v_{an} at the ac-side of the rectifier is written in terms of the on-time duty cycles and dc voltage as follows

$$v_{an} = \frac{V_{dc}}{6}(2d_a - d_b - d_c) \tag{33}$$

Hence, since the fundamental of v_{an} is always greater than $\sqrt{(E_m - RI)^2 + (\omega L I)^2}$, then (32) is always satisfied and the proposed control strategy provides a stable operation for the rectifier. On the other hand, the chattering which is the main obstacle in SMC is solved by employing the method presented in [32]. Unlike the hysteresis current control, the proposed SMC generates PWM signals by comparing level shifted carrier signals with the line current errors without using any band. However, the chattering can also be tackled by using the second-order SMC method in [38].



(a)

(b)

FIGURE 2. Three-phase three-level T-type rectifier with: (a) the PWM generation block and (b) the proposed SMC strategy.

D. DETERMINATION OF LINE CURRENT AMPLITUDE AND MAXIMUM ALLOWABLE OUTPUT VOLTAGE

On the other hand, the expression for the line current amplitude can be obtained by considering the power balance of the rectifier as follows. The input power delivered by the three-phase grid into the rectifier is

$$P_{in} = \frac{3}{2} E_m I \tag{34}$$

Neglecting the switching losses in the rectifier, while some part of P_{in} is absorbed by R, the remaining part of P_{in} is absorbed by the load. Therefore, using power balance concept, we can obtain the following expression

$$\frac{3}{2} E_m I = \frac{3}{2} R I^2 + V_{dc} I_L \tag{35}$$

Equation (35) is a quadratic equation which is written as

$$I^2 - \frac{E_m I}{R} + \frac{2 V_{dc} I_L}{3R} = 0 \tag{36}$$

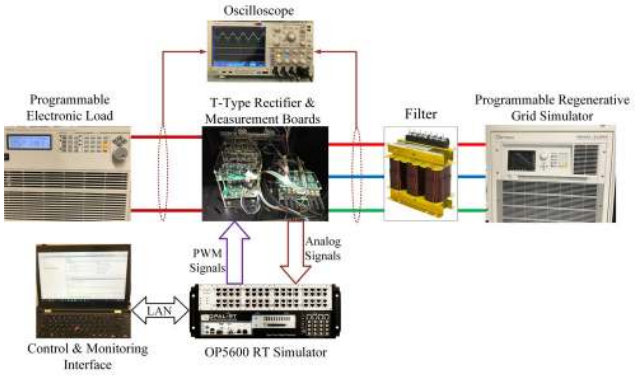


FIGURE 3. Experimental prototype.

TABLE 2. System and control parameters.

Description and Symbol	Value
Grid voltage amplitude, E_m	$120\sqrt{2}$ V
Inductance, L	1mH
Inductor resistance, R	0.1Ω
DC capacitors, $C_1 = C_2$	470μF
Load resistance, R_L	40Ω
DC-link voltage reference, V_{dc}^*	400V
PI gains, K_p and K_i	2 , 180
Imbalance compensation gain, K_e	-0.1
Switching frequency, f_{sw}	5kHz

The expression for I can be obtained by solving (36) as follows

$$I_{1,2} = \frac{\frac{E_m}{R} \pm \sqrt{\frac{E_m^2}{R^2} - \frac{8 I_L V_{dc}}{3R}}}{2} \tag{37}$$

It is obvious from (37) that there are two solutions for I which depend on the operating point of the rectifier. These solutions will be real if the following condition is satisfied

$$\left(\frac{E_m}{R}\right)^2 > \frac{8 I_L V_{dc}}{3R} \tag{38}$$

The maximum value of dc voltage can be determined as

$$V_{dc} < \frac{3 E_m^2}{8 R I_L} \tag{39}$$

In other words, V_{dc} cannot exceed $3E_m^2/8RI_L$. Equation (39) can be used to find the maximum dc voltage value that the rectifier can provide. For instance, V_{dc} cannot be greater than 540V when $E_m = 120\sqrt{2}$V, $R = 1\Omega$, and $I_L = 20$A. The block diagram of the PWM generation and proposed control strategy are shown in Fig. 2.

V. SIMULATION AND EXPERIMENTAL RESULTS

The theoretical considerations and feasibility of the proposed control strategy are validated by computer simulations using

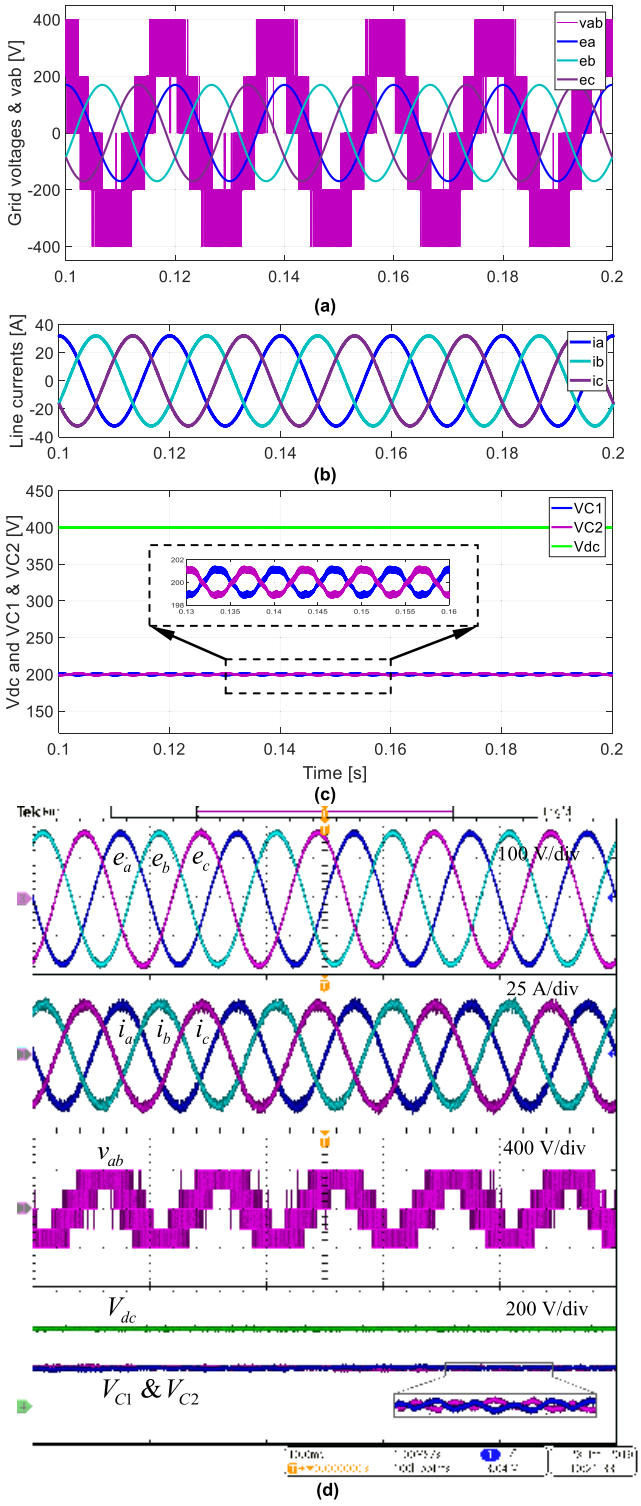


FIGURE 4. Simulated and experimental steady-state responses of (e_a, e_b, e_c), v_{ab}, (i_a, i_b, i_c), (V_{C1}, V_{C2}), and V_{dc} under 20Ω resistive load. (a)-(c) Simulation, (d) Experiment.

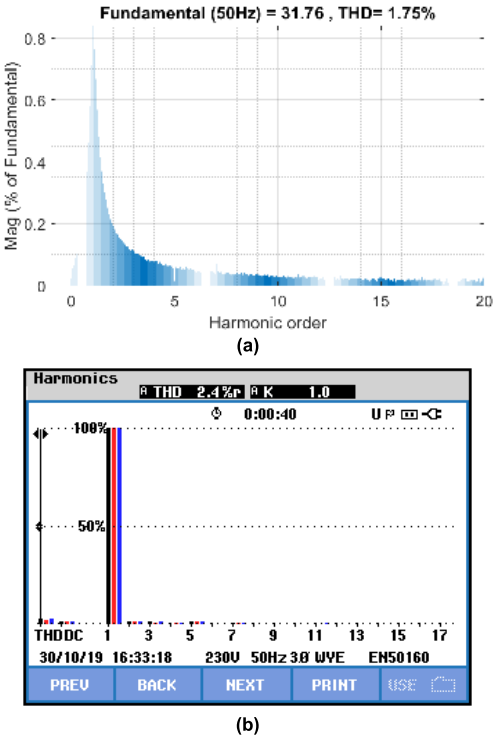


FIGURE 5. Simulated and experimental spectrums of line currents corresponding to Fig. 4. (a) Simulation, (b) Experiment.

Matlab/Simulink and experiments. The experimental results were obtained from a setup which was built to realize the system shown in Fig. 2(b). Fig. 3 shows the experimental prototype together with the equipment used to realize the proposed system. The proposed control technique was developed through the Matlab/Simulink environment and executed through OPAL-RT OP5600 real-time simulator, which was used as the main controller in this study. A programmable electronic load (Chroma-63804) is employed to emulate the DC side load. A regenerative grid simulator (Chroma61860) is used to emulate the grid. The T-Type rectifier was built by GeneSic hybrid SiC Schottky rectifier/Si IGBT modules. The gate drives and measurement boards (from Taraz Technologies) are used between OPAL-RT controller and T-Type rectifier to adapt the PWM and analog signal levels. Tektronix MSO4100 series oscilloscope is used to collect the experimental waveforms. The simulation and experimental results are obtained by using the system and control parameters presented in Table 2.

Fig. 4 shows simulated and experimentally obtained steady-state responses of grid voltages (e_a, e_b, e_c), line currents (i_a, i_b, i_c), line-to-line voltage between phase a and phase b (v_{ab}), capacitor voltages (V_{C1}, V_{C2}), and output voltage (V_{dc}) under a 20Ω resistive load.

It obvious from Figs. 4(c) and (d) that the first control objective (i.e.: regulation of dc output voltage) is achieved. The output voltage is regulated at $V_{dc}^* = 400\,\text{V}$. The second control objective (i.e.: sinusoidal line currents with unity power factor) is also satisfied. It is evident from Fig. 4(a), (b) and (d) that the line currents are sinusoidal and in phase with grid voltages. This means that the unity power factor requirement is satisfied. The theoretical value of I computed from (37) is 32.03A which is in good agreement

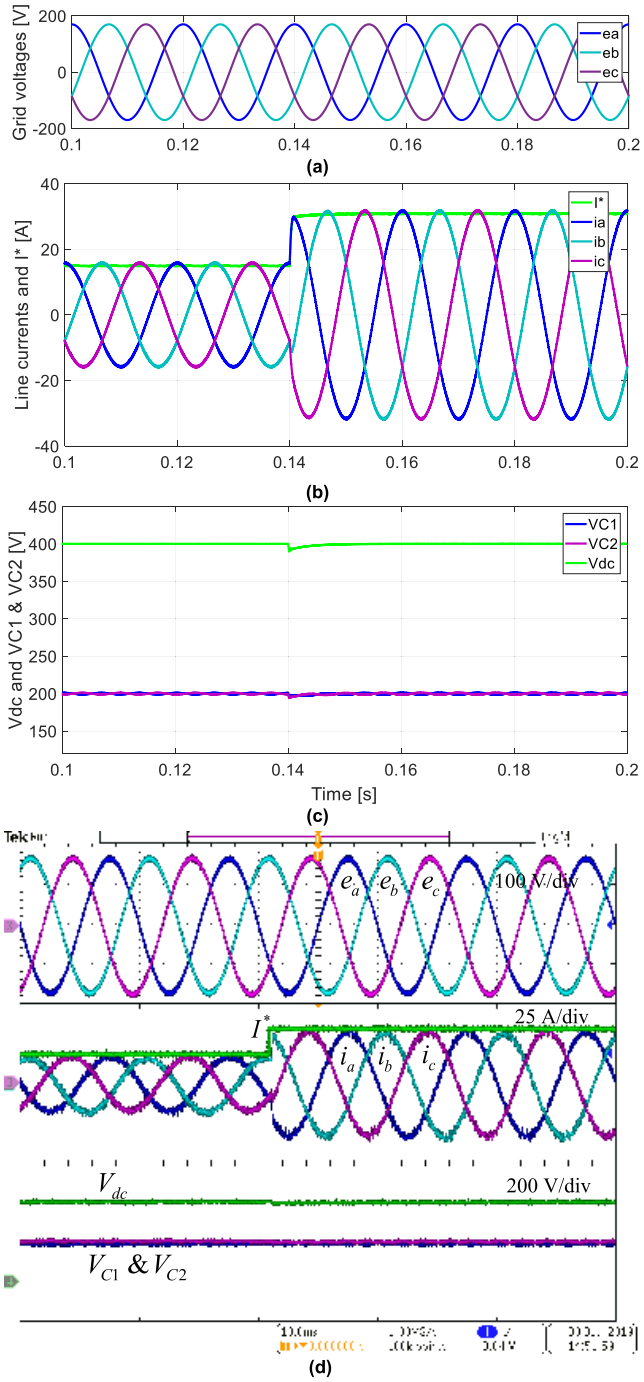


FIGURE 6. Simulated and experimental dynamic responses of (e_a, e_b, e_c), (i_a, i_b, i_c), I^*, (V_{C1}, V_{C2}), and V_{dc} for an abrupt change in R_L from 40Ω to 20Ω: (a)-(c) Simulation, (d) Experiment.

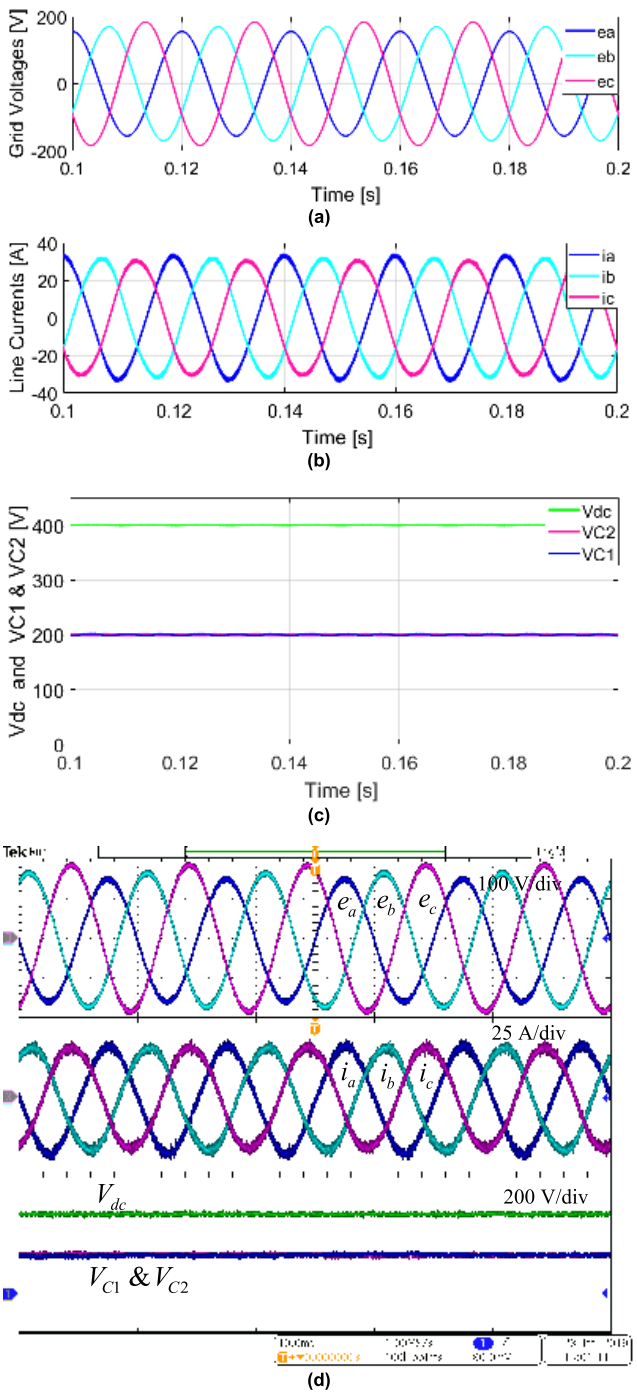


FIGURE 7. Simulated and experimental steady-state responses of (e_a, e_b, e_c), (i_a, i_b, i_c), (V_{C1}, V_{C2}), and V_{dc} for an unbalanced grid voltages under 20Ω resistive load. (a)-(c) Simulation, (d) Experiment.

with the simulation and experimental results. The line-to-line voltage (v_{ab}) obtained by simulation and experimentally has five levels (±400 V, ±200 V and 0V) which agrees well with the values in Table 1. The third control objective (i.e.: dc capacitor balancing) is also satisfied. Figs. 4(c) and (d) show the dc capacitor voltages which are balanced at 200V (half of V_{dc}).

The harmonic spectrum and THD of line currents are depicted in Fig. 5. Clearly, the harmonic components are negligibly small. The computed and measured THD values are 1.75% and 2.4%, respectively. The experimental THD is higher than that obtained by simulation. The main reason of this difference comes from the non-ideal environment in the experimental setup such as measurement errors, unforeseen

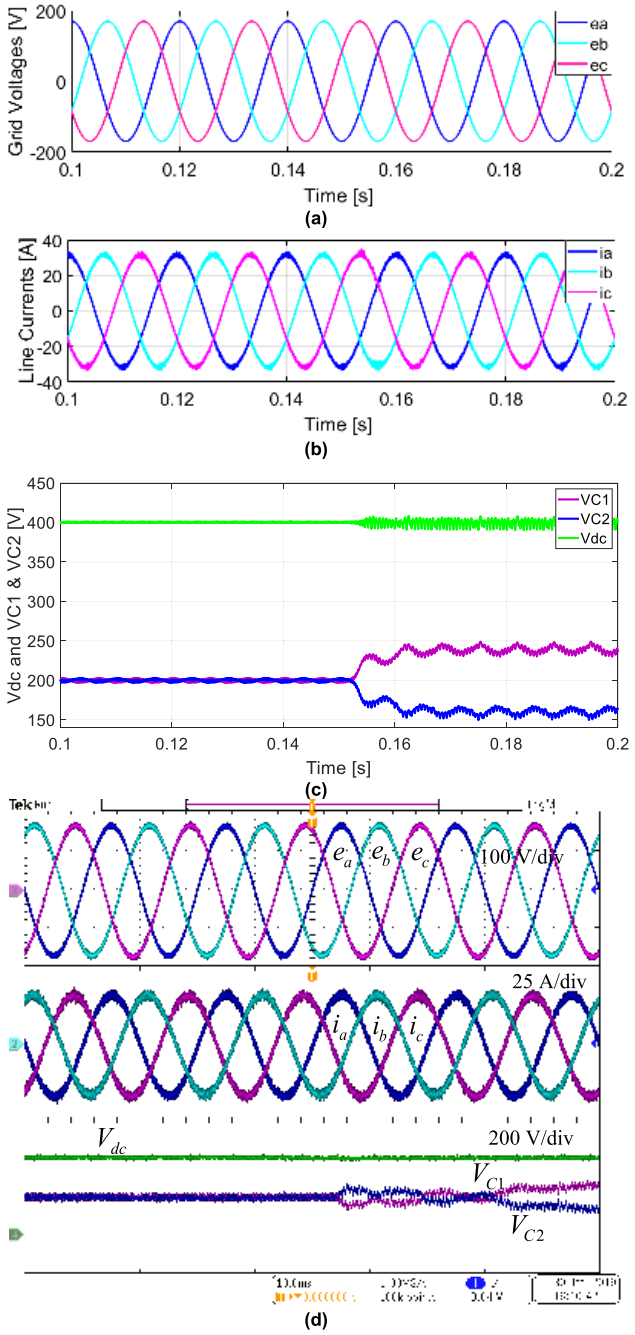


FIGURE 8. Simulated and experimental responses of (e_a, e_b, e_c), (i_a, i_b, i_c), (V_{C1}, V_{C2}), and V_{dc} with and without imbalance compensation control under 20Ω resistive load. (a)-(c) Simulation, (d) Experiment.

noise, dead-time effect and real rectifier which cannot operate same as in the simulation model. However, the measured THD value is within the range of international standard [39].

Fig. 6 shows the dynamic responses of grid voltages, line currents, reference amplitude (I^*), dc capacitor voltages, and dc output voltage for an abrupt change in the load resistance (R_L) from 40Ω to 20Ω. As shown in Figs. 6(b) and (d), the line currents exhibit very fast response to this load change so as to track their references. The reference amplitude produced by the PI controller is quite fast. Except for the transition period, the output voltage regulation is achieved as shown in Figs. 5(c) and (d). Clearly, the dynamic response of output voltage is slower than that of the line currents. However, such behavior is quite normal as the inner loop (current control) is usually much faster than the outer loop (dc voltage control) in such systems. On the other hand, the dc capacitor voltages are almost not influenced from the load change and are balanced at 200V.

Fig. 7 shows the steady-state responses of the line currents under unbalanced grid voltages. The amplitudes of grid voltages are $110\sqrt{2}$, $120\sqrt{2}$, and $130\sqrt{2}$, respectively. Despite the $\pm 8.3\%$ unbalanced grid voltages, the line currents are slightly affected and they are almost balanced. On the other hand, the other variables such as output voltage and dc capacitor voltages are controlled successfully.

Fig. 8 shows the dynamic responses of grid voltages, line currents, dc capacitor voltages, and output voltage obtained with and without capacitor voltage balancing control. Figs. 8(a), (b) and :(c) show the simulation results where the capacitor voltage balancing control was enabled from t = 0.1s to t = 0.155s and disabled during the interval from t = 0.155s to t = 0.2s. It is apparent that the output voltage, line current and capacitor voltage control are achieved successfully. However, when the capacitor voltage balancing control is disabled at t = 0.155s, an imbalance exists in the capacitor voltages such that the upper capacitor voltage (V_{C1}) becomes larger than the lower capacitor voltage (V_{C2}). The experimental result corresponding to this case is presented in Fig. 8(d). Comparing simulation and experimental results obtained when the capacitor voltage balancing control was active, one can see that both results are in good agreement. On the other hand, although the simulation and experimental results obtained without capacitor voltage balancing control agree well, there is a slight difference in the behavior of capacitor voltages immediately after the capacitor voltage balancing control is disabled. Nevertheless, addition of V_{C1} and V_{C2} always equal to V_{dc}.

VI. CONCLUSION

A SMC approach is presented for three-phase three-level T-type rectifiers with capacitor voltage balancing control. The proposed SMC strategy is formulated in the *abc* frame rather than the *dq* frame. The consequence of designing the current control strategy in the *abc* frame eliminates the three-phase current transformations that would be needed if the design is made in the *dq* frame. The dc voltage regulation is achieved by a PI controller which guarantees zero steady-state error in the output voltage. On the other hand, another important contribution of this work is the dc capacitor voltages balancing which is accomplished by using a proportional control. The proportional control feeds the dc capacitor voltages error through a suitable gain into the line current references. As a consequence of this feedback, the imbalance between the capacitor voltages is eliminated. The effectiveness of the proposed control strategy is validated by simulation and

experimental studies during steady-state, transients caused by load change, and unbalanced grid. The results show excellent steady-state as well as dynamic performances with low THD in the line currents, zero steady-state error in the output voltage, and very fast dynamic response.

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