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LETTER

Snapback-free base resistance controlled thyristor with floating N-region

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Abstract An analysis model of snapback voltage for the base resistance controlled thyristor (BRT) is developed in this paper. It's shown that, improving hole current flowing into P-base region is an important way to suppress snapback phenomenon during forward conducting state. Thus, a new BRT with a floating N-region in N-drift layer is proposed. In this new structure, the floating N-region introduces a hole potential barrier in parasitic PNP to prevent holes from being swept into cathode. Then, almost all of hole current flow into P-base to trigger latch-up effect and the parasitic PNP transistor is greatly suppressed. Thus, snapback is significantly suppressed. Numerical simulation results show that, when doping level and length of floating N-region are $8.0 \times 10^{15}\,\mathrm{cm}^{-3}$ and $5.0\,\mu\mathrm{m}$, snapback-free can be realized, and pulse discharge performance and turn on characteristics are greatly improved meanwhile the high blocking capability is maintained.

Keywords: base resistance controlled thyristor, floating N-region, snapback-free, turn-on

Classification: Power devices and circuits

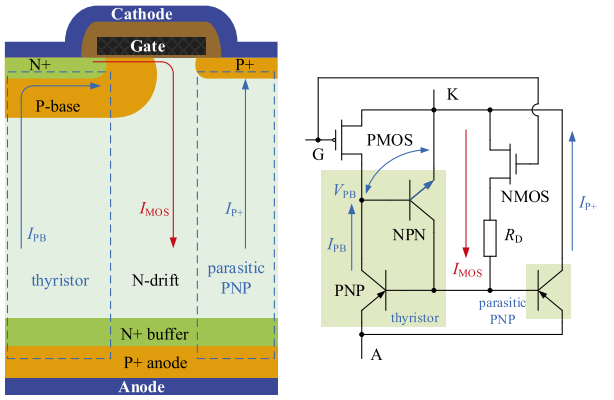

Fig. 1. Conventional BRT structure (left) and equivalent circuit (right).

1. Introduction

High voltage pulsed power technology [1, 2, 3, 4] has been widely used in industrial applications and military defense applications, such as food processing, medical treatment, environment protection and others [5, 6, 7, 8]. Over the past decades, solid-state power devices [9, 10, 11] have become the preferred choice of pulse switch in pulse modulators due to their high efficiency, long lifetime, light weight and low cost [12]. Among these devices, the base resistance controlled thyristor (BRT) [13, 14, 15, 16, 17, 18] attracted considerable attention because of its ultra-high current density, reduced forward voltage drop and double-diffusion process which compatible with IGBT [19, 20, 21]. However, snapback occurs during the transition from IGBT mode to thyristor mode, which may result in current hogging in multicell structures because of the non-uniform turn-on [22]. In [23, 24, 25, 26], self-aligned corrugated p-base is introduced into BRT, which increases resistance of P-base (R_{PB}) by lateral diffusion of boron. In this way, snapback phenomenon is effectively suppressed because the latching current of thyristor is decreased which determined by resistance R_{PB} [21]. In previous work [27], a N-type buried layer is adopted into BRT to improve the effective trigger current of thyristor, and significantly suppress snapback. But in this structure, snapback cannot be completely eliminated. In [28], BRT with semi-superjunction achieves snapback-free characteristics, reduced turn-off loss and better trade-off performance. But fabrication process of this structure is relatively difficult.

In this paper, an analysis model of snapback voltage (V_{SB}) is developed. Based on this model, improving hole current flowing into P-base region is an effective way to suppress snapback phenomenon. So a new BRT structure with floating N-region is proposed and investigated. Analyzed results show that, snapback-free can be realized, and pulse discharge performance and turn on characteristics are improved meanwhile maintaining the similar blocking capability.

2. Snapback analysis model

The cross section and equivalent circuit of conventional BRT are shown in Fig. 1. In BRT device, electron current (I_{MOS}) of surface NMOS flows into N-drift layer from N+ cathode, which serves as thyristor trigger current leading to strong injection of holes. The injected hole current (I_{PB}) flows into P-base region, and produces a voltage drop (V_{PB}) to trigger latch up effect. Part of hole current (I_{P+}) can also be directly swept into cathode by the reverse biased P+/N-

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drift junction of parasitic PNP transistor. BRT therefore operates in IGBT mode at low current. As the hole current increases, thyristor will be triggered to latch up when V_{PB} exceeds the built-in potential of PN junction (V_{bi}), which results in a suddenly drop of resistance. Then, snapback phenomenon occurs in forward conducting state.

The V_{PB} produced by injected hole current (I_{PB}) in P-base region is given by [21]

$$V_{PB} = I_{PB}R_{PB} = I_{PB}\rho_{PB}\frac{L_{PB}}{Z} \tag{1}$$

where Z, ρ_{PB}, L_{PB} are the length of cell in the orthogonal direction to cross section, the pinch sheet resistance and length of P-base region, respectively. The hole current (I_{PB}) flowing into P-base region is a part of collector current (I_{PNP}) of the wide base PNP transistor, which is amplified by β_{PNP} as the base drive current (I_{MOS}) of PNP. And thus, it's given by

$$I_{PB} = k_P I_{PNP} = k_P\beta_{PNP}I_{MOS} \tag{2}$$

where k_P is the ratio of hole current in P-base region to all of the collector current of PNP transistor.

For very small values of V_{DS}, the drain current of MOSFET can be written as [29]

$$I_{DS} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)V_{DS} \tag{3}$$

Then, considering the drift resistance (R_D) between NMOS and anode, thyristor trigger current (I_{MOS}) can be given by

$$I_{MOS} = \frac{V_{AK}}{\dfrac{Lt_{ox}}{\mu_n\varepsilon_{ox}Z(V_{GK} - V_{Tn})} + R_D} \tag{4}$$

where μ_n, ε_{ox}, t_{ox}, L, V_{Tn} are electron mobility in inversion layer, dielectric constant of oxidation, gate oxide thickness, channel length and threshold voltage of surface NMOS, respectively. Substituting Eq. (2) and (4) into Eq. (1), V_{PB} can be expressed as

$$V_{PB} = k_P\beta_{PNP}\rho_{PB}\frac{L_{PB}}{Z}\frac{V_{AK}}{\dfrac{Lt_{ox}}{\mu_n\varepsilon_{ox}Z(V_{GK} - V_{Tn})} + R_D} \tag{5}$$

The thyristor will be triggered to latch up when V_{PB} exceeds built-in potential (V_{bi}). And thus, the snapback voltage (V_{SB}) is given as

$$V_{SB} = \frac{ZV_{bi}}{k_P\beta_{PNP}\rho_{PB}L_{PB}} \times \left[R_D + \frac{Lt_{ox}}{\mu_n\varepsilon_{ox}Z(V_{GK} - V_{Tn})}\right] \tag{6}$$

From Eq. (6), it can be concluded that k_P and R_D are two important parameters to reduce the snapback voltage (V_{SB}). Obviously, R_D mainly relies on the doping level and thickness of N-drift layer, which are restricted by the breakdown voltage. Consequently, to suppress snapback phenomenon, it's very important to increase the proportion coefficient k_P.

In addition, due to the positive feedback in thyristor, BRT turn-on threshold voltage (V_{GT}) is much lower than the threshold voltage (V_{Tn}) of surface NMOS. In subthreshold region, the drain current of MOSFET is given by [30]

$$I_{MOS} = \mu_n\frac{Z}{L}\sqrt{\frac{\varepsilon_{si}qN_A}{4\psi_B}}\left(\frac{kT}{q}\right)^2 \times \left[1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right] \times \exp\frac{q(V_{GK} - V_{Tn})}{mkT} \tag{7}$$

$$m = 1 + \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{\frac{\varepsilon_{si}qN_A}{4\psi_B}} \tag{8}$$

where ε_{si}, ψ_B, N_A are dielectric constant of silicon, fermi potential and P-base doping level at NMOS region, respectively. Thus, substituting Eq. (2) and (7) into Eq. (1), V_{PB} is expressed as

$$V_{PB} = k_P\beta_{PNP}\rho_{PB}\frac{L_{PB}}{Z}I_{Tn}\exp\frac{q(V_{GK} - V_{Tn})}{mkT} \tag{9}$$

$$I_{Tn} = \mu_n\frac{Z}{L}\sqrt{\frac{\varepsilon_{si}qN_A}{4\psi_B}}\left(\frac{kT}{q}\right)^2\left[1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right] \tag{10}$$

BRT will be turned on when V_{PB} exceeds V_{bi}, and then the turn-on threshold voltage (V_{GT}) can be expressed as

$$V_{GT} = V_{Tn} + \frac{mkT}{q}\ln\frac{ZV_{bi}}{k_P\beta_{PNP}\rho_{PB}L_{PB}I_{Tn}} \tag{11}$$

It's clear from Eq. (11) that improving coefficient k_P can reduce BRT turn on threshold voltage. Then, turn on characteristics and pulse discharge performance are improved.

Given the above, the coefficient k_P of hole current flowing into P-base region is an important parameter to suppress snapback phenomenon and improve turn-on characteristics. Therefore, a new BRT structure with floating N-region is proposed and analyzed. In this structure, the floating N-region produces a hole potential barrier to push hole current into P-base. Thus, hole current in P-base is greatly improved.

3. BRT structure with floating N-region

Schematic cross section of the proposed BRT structure and NBL-BRT in previous work [27] are shown in Fig. 2. Unlike conventional BRT and NBL-BRT, the proposed BRT structure has a floating N-region in parasitic PNP transistor. The built-in potential ϕ_{bi} between floating N-region and N-drift layer produces a hole potential barrier in

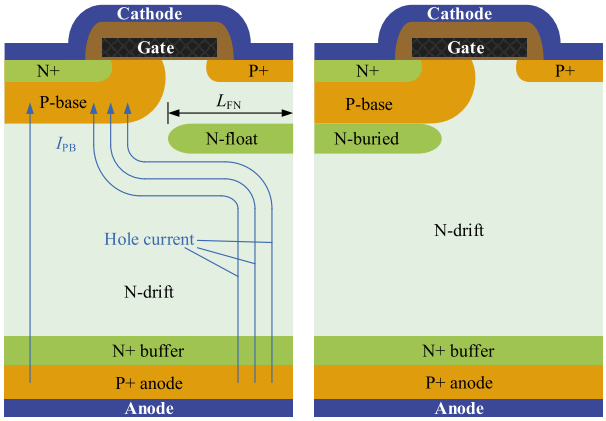

Fig. 2. Proposed BRT structure (left) and NBL-BRT in [27] (right).

parasitic PNP, which prevents holes from being swept into P+ cathode. Then, most of hole current flow into P-base region to trigger thyristor and only less or even no hole current go out through PNP transistor. Thus, coefficient k_P is greatly increased, and hole current density in P-base region is obviously improved. Snapback therefore can be significantly suppressed.

The built-in potential can be calculated as

$$\phi_{bi} = \frac{kT}{q} \ln \frac{N_{FN}}{N_D} \tag{12}$$

where N_{FN} and N_D are the doping concentration of floating N-region and N-drift layer, respectively. From Eq. (12), it can be concluded that improving the doping level of floating N-region (N_{FN}) is favorable to enhance hole potential barrier ϕ_{bi}, and then improves hole current in P-base region. In addition, the length of floating N-region (L_{FN}) is also optimized to suppress snapback phenomenon.

In numerical simulation, both of the proposed BRT, conventional BRT and NBL-BRT with blocking capability of 1400 V are analyzed by Sentaurus TCAD tools. The device parameters have been listed in Table I. In order to realize the blocking capability of 1400 V, the thickness and doping level of N-drift layer are optimized to 110 μm and 1.0×10^{13} cm^{-3}, respectively.

Table I. Devices structure parameters

Parameters	Pro.	Con.	NBL-BRT
Cell dimension, L_C/μm	10.0	10.0	10.0
Device active are, A/cm^2	0.65	0.65	0.65
N-float doping, N_{FN}/cm^{-3}	8.0×10^{15}	/	/
N-float length, L_{FN}/μm	5.0	/	/
N-drift thickness, W_D/μm	110	110	110
N-drift doping, N_D/cm^{-3}	1.0×10^{13}	1.0×10^{13}	1.0×10^{13}
N-buried doping, N_{BL}/cm^{-3}	/	/	1.0×10^{15}
N+ buffer thickness, W_B/μm	10.0	10.0	10.0
N+ buffer doping, N_B/cm^{-3}	1.0×10^{16}	1.0×10^{16}	1.0×10^{16}

3.1 Forward conduction characteristics

Fig. 3 shows forward conduction characteristics of the proposed BRT, conventional BRT and NBL-BRT at gate voltage of 10.0 V. It's clear that undesirable snapback phenomenon occurs in output curve of the conventional BRT, which has the ΔV_{SB} of ~1.0 V. And in the NBL-BRT, snapback phenomenon cannot be completely eliminated in spite of the fact that ΔV_{SB} is reduced by 61.6% when compared with conventional BRT. While the proposed structure shows snapback-free characteristics when compared with the NBL-BRT and conventional BRT. Consequently, the new structure is much more reliable than conventional device.

Fig. 4 shows hole current distribution during forward conducting state. As aforementioned, part of injected holes from bottom P+ anode are directly swept into P+ cathode by parasitic PNP region in conventional BRT, which are shown in Fig. 4(c). In the NBL-BRT, due to the existing of

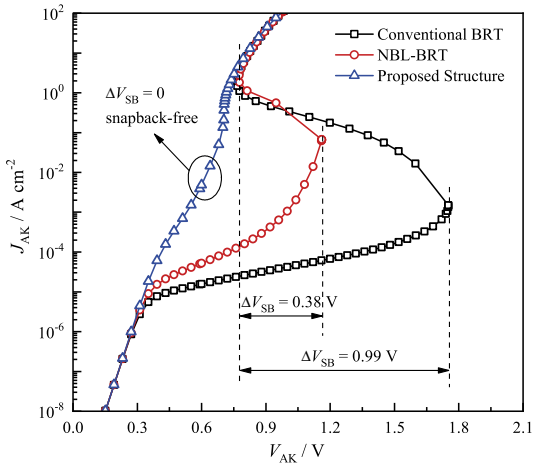

Fig. 3. Comparison of forward conduction characteristics of the proposed BRT, NBL-BRT and conventional BRT.

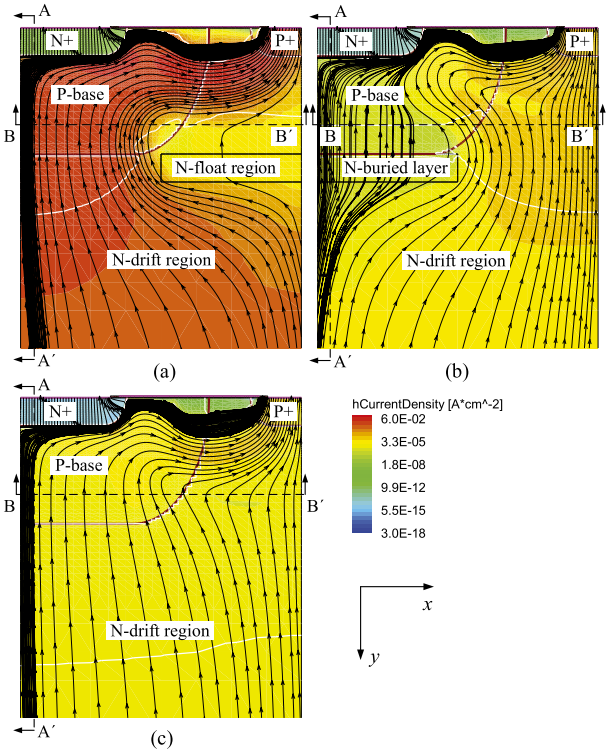

Fig. 4. Comparison of hole current flow lines for (a) the proposed BRT, (b) NBL-BRT and (c) conventional BRT.

N-buried layer, some of hole current in thyristor are also pushed into parasitic transistor. In the proposed BRT structure, as shown in Fig. 4(a), almost all of hole current flow into P-base region to trigger thyristor due to the floating N-region, and there is no hole current going through parasitic transistor. Thus, hole current in P-base region is greatly improved.

Fig. 5 shows the hole current density (J_p) along line AA′ and BB′ (see Fig. 4). Compared with the conventional BRT, hole current density in thyristor region of the proposed BRT is improved by about 3 orders of magnitude, which is shown in Fig. 5(a). It's clear in Fig. 5(b) that, for the proposed BRT, hole current density in P-base region is improved by 3 orders of magnitude, and the coefficient k_P has been improved from ~0.757 to ~0.998. Thus, almost

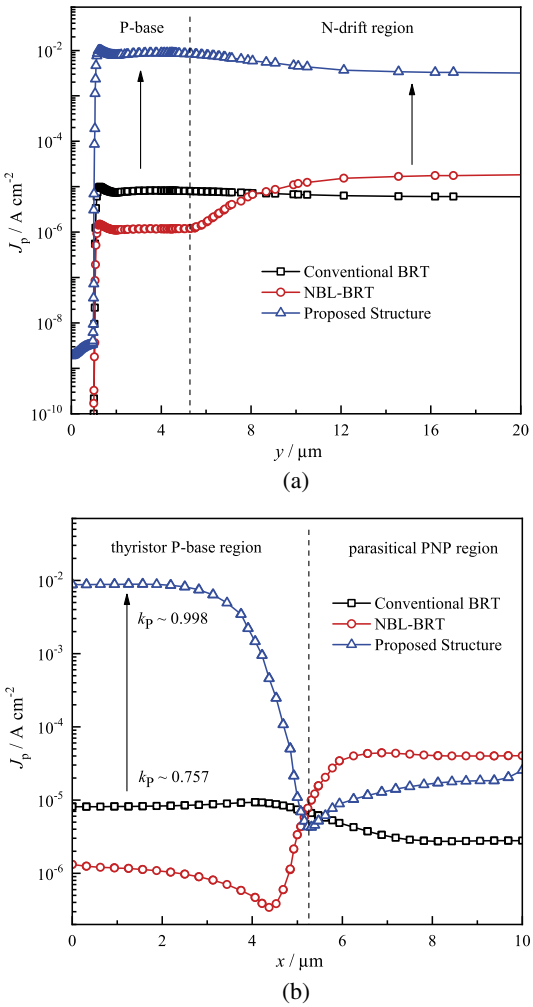

Fig. 5. Hole current density along line (a) AA′ and (b) BB′ in Fig. 4.

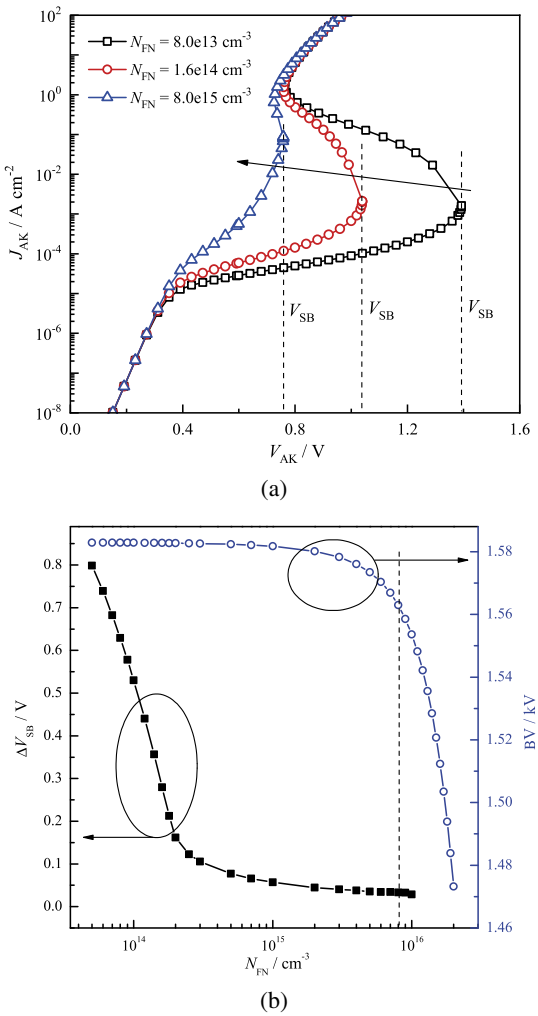

Fig. 6. (a) Output characteristics under different N_{FN} and (b) Dependence of ΔV_{SB} and BV on N_{FN}.

all of hole current flows into P-base region to trigger thyristor, and the parasitic PNP transistor is significantly suppressed.

3.2 Doping level and length of floating N-region

Dependences of ΔV_{SB} and BV (Breakdown Voltage) on N_{FN} are shown in Fig. 6. It's clear from Fig. 6(a) that the higher doping level (N_{FN}), the lower snapback voltage (V_{SB}). As expected, improving the doping concentration of floating N-region is favorable to enhance hole potential barrier (ϕ_{bi}), and then suppress snapback phenomenon. Fig. 6(b) shows that ΔV_{SB} decreases rapidly from 0.8 V to 0.1 V while N_{FN} increases from 5.0×10^{13} cm^{-3} to 3.0×10^{14} cm^{-3}, and then slowly reduces. But, the breakdown voltage will drop rapidly when N_{FN} is higher than 8.0×10^{15} cm^{-3} because it's harder for depletion layer to expand through floating N-region.

Dependences of ΔV_{SB} and BV on L_{FN} are shown in Fig. 7. It can be seen that ΔV_{SB} constantly decreases while L_{FN} increases from 1.5 μm to 5.0 μm. Thus, increasing the length of floating N-region can also effectively suppress snapback. And snapback phenomenon can be completely eliminated when the L_{FN} increases to 5.0 μm.

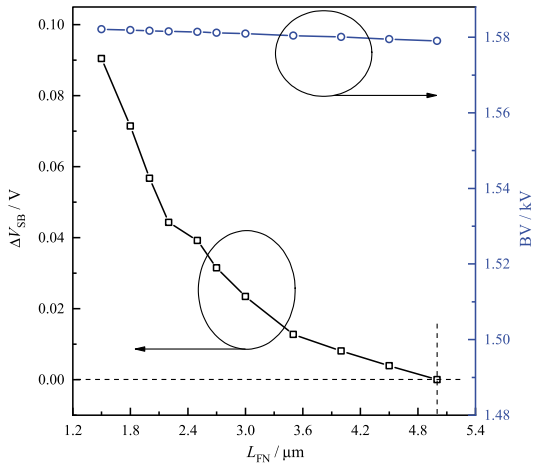

Fig. 7. Dependence of ΔV_{SB} and BV on L_{FN}.

3.3 Dynamic characteristics

The pulse discharge waveforms are plotted in Fig. 8. It's clear from Fig. 8(a) that the peak current (I_p) of ~3200 A and first pulse width (t_p) of ~0.14 μs which lead to di/dt of ~58 kA/μs are obtained for all structures. But the proposed BRT has a faster pulse discharge speed, and reduces turn on delay time by 45 ns when compared with conventional BRT. As aforementioned, in the proposed BRT, coefficient k_P is greatly improved due to the floating N-region, and then the

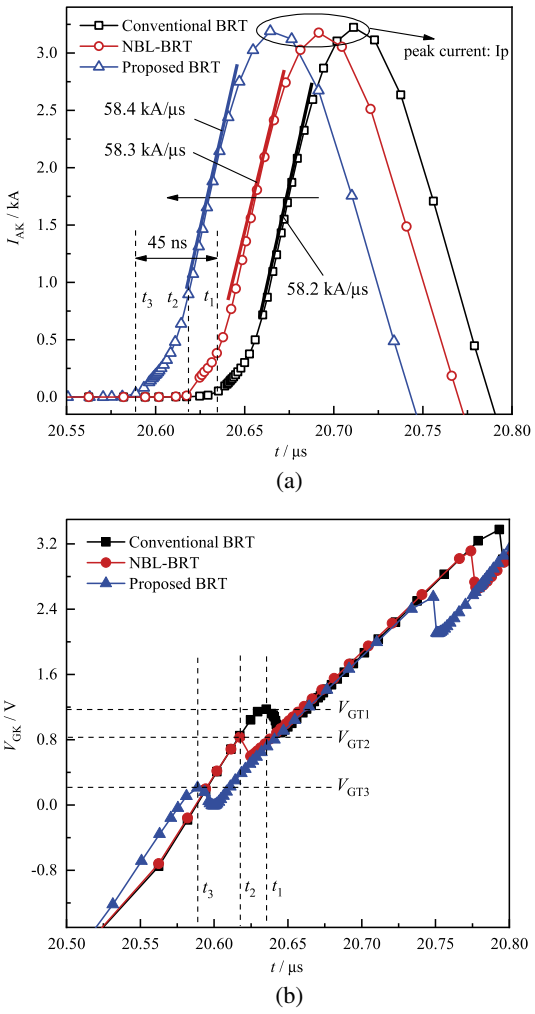

Fig. 8. (a) Anode current (I_{AK}) and (b) gate voltage (V_{GK}) of pulse discharge characteristics.

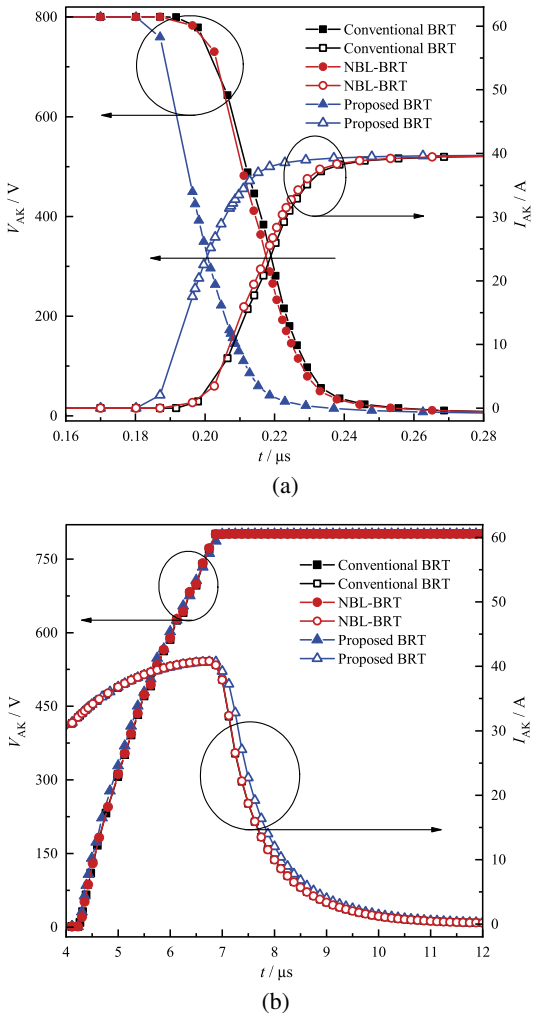

Fig. 9. (a) Turn-on and (b) turn-off waveforms of the proposed BRT, NBL-BRT and conventional BRT.

turn on threshold voltage (V_{GT}) is reduced. Fig. 8(b) shows that V_{GT} of the proposed BRT has been reduced by about 80% when compared with the conventional BRT.

Fig. 9 shows the turn-on and turn-off waveforms. It can be seen from Fig. 9(a) that the proposed structure has a faster turn-on speed than conventional BRT due to the reduced turn on threshold voltage (V_{GT}). At current density of 40.0 A/cm^2, the proposed BRT has a turn-on energy loss (E_{on}) of 0.223 mJ, which is reduced by 12.9% when compared with that of 0.256 mJ for the conventional BRT. Fig. 9(b) shows that both proposed BRT and conventional BRT have almost same turn-off characteristics.

4. Conclusion

In this paper, an analysis model of snapback voltage for BRT structure is developed. Based on this model, snapback phenomenon can be greatly suppressed by improving hole current flowing into P-base region. Therefore, a new BRT structure with floating N-region is proposed. The floating N-region introduces a hole potential barrier to prevent holes from being swept into cathode. Then, hole current in P-base region is greatly improved. Analyzed results show that, for the proposed BRT structure, when the doping level and length of floating N-region is 8.0×10^{15} cm^{-3} and 5.0 μm, snapback-free can be realized and pulse discharge performance and turn on characteristics are greatly improved meanwhile the high blocking capability is maintained.

Acknowledgments

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