Open access • Posted Content • DOI:10.20944/PREPRINTS201909.0014.V1

Soft-Core Architecture for Odd/Even Order Sampling I/Q Demodulator with Dual-Port Block Memory Considerations — Source link

Madodana Mfana, Ali N. Hasan

Published on: 01 Sep 2019

Soft-Core Architecture for Odd/Even Order Sampling I/Q Demodulator with Dual-Port Block Memory Considerations

Madodana Mfana[1] and Ali N. Hasan[1],

[1] Faculty of Engineering and the Built Environment, University of Johannesburg, Johannesburg 2092, South Africa; mydmfana@gmail.com

* Correspondence: mydmfana@gmail.com; Tel.: +27-84-693-2562

Abstract: Soft-Core architecture for Analogue to Digital Converter (ADC) sampling is useful for mixed signal applications. Soft-core architecture for cutting edge odd or even ADC sampling with interface to block RAM memory has not been found. Soft-core architecture as a concept has become popular due to the advantage of customization for different applications as compared to general-core architecture suited for single application. The latest generation of piecewise sampling is odd sampling and was introduced in the second decade of the 20th century. Odd and even order sampling techniques are analogue in nature driven by a tuned (tuned for odd or even) mixer. This paper proposes a third-generation piecewise sampling with soft-core architecture that enables an option to select both odd and even while interfacing to memory mapping. The proposed odd/even has superior SNR performance of 6 dB as compared to existing architecture such as Mod-Δ which recorded worst performance of 18 dB. Advances in soft-core technology have allowed a niche odd/even switching field to be identified and studied, the study has also been extended to include memory architecture.

Keywords: Soft-Core Architecture, System on Chip (SoC), Radio Frequency System on Chip (RFSoC), Adaptive Compute Acceleration Platform (ACAP), Scalar Processing, Vector Processing, I/Q demodulator, Odd Order Sampling, Even Order Sampling, Analogue to Digital Converter (ADC)

1. Introduction

A new soft-core architecture that allows automatic switching between odd and even sampling with direct efficient memory interface was designed and tested in Matlab. The methodology used to investigate performance parameters of the soft-core architecture was through an empirical experimental study. Empirical experimental study involved a new mathematical model development for odd or even sampling with memory mapping architecture, the performance of the model was tested using Matlab and laboratory experimental setups. Performance parameters that were improved were sample frequency and memory size optimization, the sample frequency was halved while memory size was optimization from 512 bytes to 256 bytes without changing the design parameters for I/Q demodulator and ADC. Findings from this study can lead to adaptation of soft-core architecture for odd/even sampling to Radar and Electronic Warfare (REW) mixed signal applications.

A. Analog to Digital Converter (ADC) Digital Formation Problem

In Electronic Warfare (EW) mixed signal processing have become normal processing techniques where analogue Radar is sampled to digital using ADC's. Pulse doppler Radar techniques such as Frequency Modulated Continuous Wave (FMCW) and Linear Frequency Modulation (FM) with variant frequency introduces the problem of digital formation of I/Q signal in the EW segment [1].

During digital formation process several factors such as sample frequency, the number of bits produced and mean squared error distortion between input and digitally reconstructed signal. A novel even order sampling I/Q demodulator date back as far as [2] and was later followed by the development of odd order sampling I/Q demodulator as recent as [1]. Odd order I/Q demodulator which is derived from even order I/Q demodulator, is characterized by linear phase/frequency relation. Such a signal attributes help relieve complexities in digital formation such as samples produced per second and distortion error of for wide bandwidth I/Q signals [1, 2].

I. Moshkin, A Nikolaev and N. Nikitin et al [3] studies complexity dynamic range related to the number of bits produced through quantization resolution while exploring phase. Several measurements error performances with different resolutions were conducted phase, 1-bit quantization showed the worst phase error performance. To reduce the number of bits produced by the ADC, dynamic range quantization encoder digital architecture design is presented in [4]. Number of bits produced introduce a sample storage capacity complexity, sample storage capacity is addressed by the design of sample and hold circuit with the purpose to extend the input signal range which allows for higher input voltages to be tolerated [5], [6] is also addressing similar issue but using NI Multisim simulation tool.

Advances in solutions that address digital formation has led to development of design and development of CMOS technology prototypes [7, 8, 9, 10, 11, 12]. To optimize dynamic range O Ordentlich, G Tabak, PK Hanumolu, AC Singer, and GW Wornell at el [13] introduces the idea of modulo ADC which reduces the dynamic range of the input signal, this technique allows 5 volts signal to be processed as 2.5 volts for a modulo 2 and processed as 1.5 volts for a modulo 4 implementations. A second order delta-sigma implementation is introduced in [14], block architecture is like that of first order delta-sigma design with a difference of a second order integrator before the quantization step. A high-performance DAC approximated ADC architecture for Synthetic Aperture Radar (SAR), the only architecture advance is the switch mode which allows switch between positive and negative quantitation [15, 16].

To address dynamic range quantization inefficiencies a low bit error encoder is designed and tested using CMOS technology [17]. The different approach to the design that addresses dynamic range resolution, [18] aim to increase the dynamic range by using the advantage of capacitance charging capabilities. The capacitance act as a sample and hold stage after the quantizer thus allowing them to maintain high resolution digital signal. [19] achieve the same designs but at low power. Different digital conversion technologies were evaluated towards the design of a PID controller [20], for digital control the ADC stage is very important and maintaining a high-quality control feedback signal in most case becomes a matter of life and death. Just like in [18] and [19] in SAR imagery high resolution signal as always, the target and [21] is trying to achieve the same objective with 1 bit/multi-level quantization stage.

B. Artificial Neural Network Analog to Digital Converter (ADC) Models

A 3-stage neural network nonlinear ADC was designed and implemented in Matlab Simulink in [22], 16-bit quantization high resolution was demonstrated in the simulation results. A design like [22] is presented in [23] but it is not clear whether its linear or non-linear. Analog-to-Digital Converter acceleration using deep learning activation function, the function circuitry caters for both under sampling and oversampling [24].

C. Electronic Warfare (EW) Signal Processing

In EW processing the ADC stage is usually followed by enveloped detector stage a mathematical model coherent envelope detector for ambient backscatter is presented [25]. Dynamic range quantization bit resolution complexities are corrected by using the envelope detector stage

[26]. Glow plasma is used to detect electromagnetic wave, full digital RF chain is also implemented [27].

After the envelope detector usually phase or frequency detector stage follows. Phase detector with feedforward noise cancellation architecture, which uses sub-sampling for phase noise detection [28]. To implement an XOR phase detector an FPGA architecture was design and implemented in [29]. Digital phase locked loop for Internet-of-Things application is presented [30]. Like [30] a sampling phase detector with ultra-low phase noise is design for microwave synthesizers applications [31]. Simple Bang Band phase detector with 1-bit third-order single feedback loop delta-sigma ADC pre-processing stage for FMCW wave synthesis [32]. Like [31] a pulse phase-frequency detector for high-speed frequency synthesizers applications [33]. A capacitive power sensor is used to design a large dynamic range phase detector [34].

D. Adaptive Compute Acceleration Platform (ACAP)

For decade Xilinx has been working towards a fully programmable heterogeneous computing platform with Scalar and Vector Processing units optimized for Artificial Intelligence (AI) plus Digital Signal Processing (DSP) [35]. Such a platform is presented as System on Chip ACAP with Scalar processing being implemented on two ARM CPU's, one of these runs a LINUX operating system. The ACAP with Vector processing being implemented on GPU optimized for AI, and digital logic fabric optimized for DSP. The ACAP also has adaptable hardware suitable for custom input-output interface and custom memory design.

This paper contributes to the body of knowledge of Signal Processing in a niche field of Electronic Warfare mixed signal processing through the following contributions:

1. An introduction of mathematical model for odd/even sampling with memory considerations.
2. A simulation performance investigation of the novel odd/even order sampling.
3. An empirical experimental sampling frequency and memory performance investigation of the novel odd/even order sampling I/Q demodulator.
4. A Field Programmable Gate Array (FPGA) implementation of the novel odd/even sampling architecture. The paper is arranged as follow:

Section II presented the proposed architecture, Section III dives straight to the derivation of mathematical model of the proposed odd/even order sampling I/Q demodulator with memory considerations, and later presents the complete mathematical form of odd/even order sampling I/Q demodulator with memory considerations. Section IV develops a simulation model to investigate the performance of the proposed odd/even order sampling ADC to that of first order Delta-Sigma ADC. Section V develops an experimental setup with results using hardware I/Q demodulator with an aim to investigate the performance of sample frequency and memory design. Section VI implements the proposed architecture on FPGA platform to investigate the validity of the simulation and experimental results. The paper is then concluded in Section VII.

II. PROPOSED SYSTEM - SOFT-CORE ARCHITECTURE FOR ODD/EVEN ORDER SAMPLING I/Q DEMODULATOR WITH MEMORY CONSIDERATIONS

This paper proposes a soft-core architecture for odd/even order sampling with memory considerations. High level architectural overview is presented in Figure 1 with both odd/even algorithm and memory access implemented in a soft-core platform such as an FPGA or Embedded.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 1 September 2019 doi:10.20944/preprints201909.0014.v1

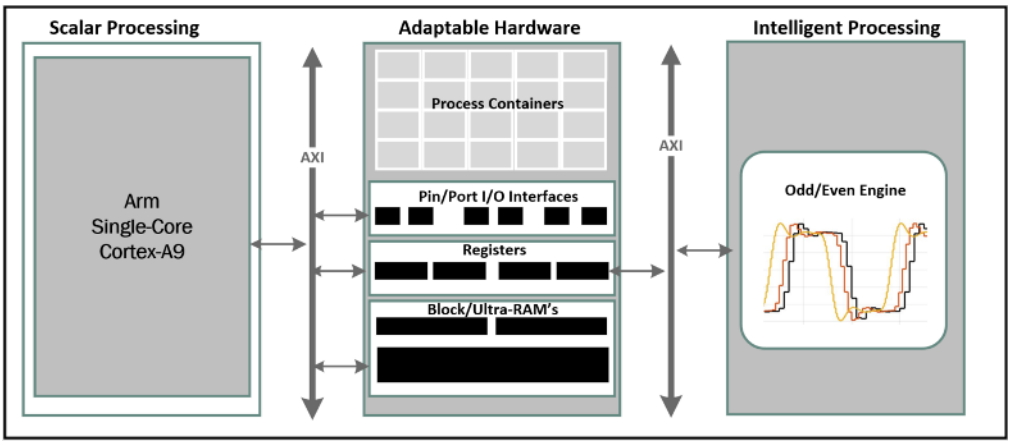

Figure 1. The proposed soft-score architecture for odd/even order sampling I/Q demodulator

The proposed soft-core architecture ready for implementation consist of programmable component with Zynq-Arm processor integrated as shown in Figure 1. The Zynq-Arm processor can access control registers through AXI data bus. The second component of the proposed soft-core architecture is the low latency digital logic circuit which implements odd/even sampling. The digital logic circuit is also controlled by the programmed registers as shown in Figure 1. The ARM processor component introduces flexibility that originally didn't exist odd/even sampling. Programmable capability of ARM processor allows for circuit control parameters to be changed at will. The results presented in this paper were collected from investigations collected from Matlab simulation, laboratory experimental setup and FPGA implementation. 8 bits addressing, storage of I_{even} and Q_{odd} for even order sampling and guard gaps are presented in in Table 3.

III. METHODOLOGY - DERIVATION OF ODD/EVEN ORDER SAMPLING I/Q DEMODULATOR WITH MEMORY CONSIDERATIONS

The design of I/Q demodulator that can flexibly select between odd and even order modes at will is considered. Further consideration is that, signal complications must also be assumed as nonexistent. This assumption is valid as the I/Q hardware has improved drastically over the years. This improvement in I/Q demodulator hardware has reached a level where such devices can be bought with operational specifications such as amplitude and phase imbalance of 0.07 dB and 0.2° respectively.

Let's also consider the dual port ram modelling term $dRM_{wr_s}^{rd^s}$ where rd^s is the read memory command, wr_s is the write memory command and s is the strobe command that selects between even or odd order. Let's further consider two terms that directly tune ADC sampling, such terms are $odd\_even\_adc\_tunning$ and $even\_odd\_adc\_tunning$ as shown in Figure 1.

A. I/Q DEMODULATOR

The design of soft-core architecture depends largely on the I/Q demodulator and Analogue to Digital Converter (ADC), traditionally the design of I/Q demodulator ADC interface for Radar and Electronic Warfare (REW) applications follows five different options as depicted in [2]. J.-E. Eklund and R. Arvidsson et al [2] modifies the traditional I/Q demodulator and ADC interface to include an odd/even selection switch and digital filter to smooth the digital ADC output [2], this modification kicks off by declaring the complex signal and I and Q as shown in equation 1, 2 and 3 below.

$$(t) = a_m(t) * (w_{IF} * t + \varphi_M(t)) \quad (1)$$

$$s(t) = I(t) * \cos(w_{IF} * t) - Q(t) * \sin(w_{IF} * t)$$

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 1 September 2019 doi:10.20944/preprints201909.0014.v1

$$I_{raw}(t) = a_M(t) * \cos(\varphi_M(t)) \quad (2)$$

$$Q_{raw}(t) = a_M(t) * \sin(\varphi_M(t)) \quad (3)$$

B. ODD ORDER SAMPLING

J.-E. Eklund and R. Arvidsson et al [2] and V. I. Slyusar et al [1] applied a FIR filter to the digital firmware mixer to obtain the final form of the presented I/Q digital mixer, it should be noted that [1] implements a 4 order FIR filter instead of a 7 order FIR filter.

Table 1. I/Q demodulator odd order digital mixing coefficients of 4 samples [2]

sample no: n	0	1	2	3	4
I-coefficients	0	1	0	-1	0
Q-coefficients	0	0	-1	0	1

$$I_{odd} = cos(w_{IF} * (T_1 + \Delta) + \varphi_{IF})) * C_1 - cos(w_{IF} * (T_3 + \Delta) + \varphi_{IF}) * C_3 \quad (4)$$

$$Q_{even} = -sin(w_{IF} * (T_2 + \Delta) + \varphi_{IF})) * C_3 + sin(w_{IF} * (T_4 + \Delta) + \varphi_{IF}) * C_1 \quad (5)$$

The I/Q modulator of the odd order presented in [1] did not clearly derived the odd order 3rd odder characterization equation presented in the paper and equation 8 and 9 below. The derivations from 6 to 7 paves the way for the proposed odd/even algorithm that considers of memory.

Table 2. I/Q demodulator FIR filtered for odd order digital mixing coefficients of 4 samples [2]

sample no: n	0	1	2	3	4
I-coefficients	0	1	0	-3	0
Q-coefficients	0	0	-3	0	1

$$I = u_1 - 3u_3 \; where \; u_1 = cos(w_{IF} * (T_1 + \Delta) + \varphi_{IF})) * C_1 \; is \; the \; ADC \; samples \quad (6)$$

$$Q = -(3u_2 - u_4) \; where \; u_2 = cos(w_{IF} * (T_2 + \Delta) + \varphi_{IF})) * C_3 \; is \; the \; ADC \; samples \quad (7)$$

C. EVEN ORDER SAMPLING

J.-E. Eklund and R. Arvidsson et al [2] and V. I. Slyusar et al [1] applied a FIR filter to the digital firmware mixer to obtain the final form of the presented I/Q digital mixer, it should be noted that [1] implements a 4 order FIR filter instead of a 7 order FIR filter. V. I. Slyusar et al [1] also introduces us to the idea of odd order sampling which is developed from even order sampling in [2], although limited theory derivation of odd order sampling he was able to apply it to single channel ADC I/Q sampling which uses 3rd order FIR filtering.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 1 September 2019 doi:10.20944/preprints201909.0014.v1

Table 3. I/Q demodulator even order digital mixing coefficients of 7 samples [2]

sample no: n	0	1	2	3	4	5	6	7
I-coefficients	1	0	-1	0	1	0	-1	0
Q-coefficients	0	1	0	-1	0	1	0	-1

$$I_{even} = cos(w_{IF} * (T_0 + \Delta) + \varphi_{IF})) * C_1 - cos(w_{IF} * (T_2 + \Delta) + \varphi_{IF}) * C_{11}$$

$$+ cos(w_{IF} * (T_4 + \Delta) + \varphi_{IF}) * C_{15} - cos(w_{IF} * (T_6 + \Delta) + \varphi_{IF}) * C_5 \quad (8)$$

$$Q_{odd} = sin(w_{IF} * (T_1 + \Delta) + \varphi_{IF})) * C_5 - sin(w_{IF} * (T_3 + \Delta) + \varphi_{IF}) * C_{15}$$

$$+ cos(w_{IF} * (T_5 + \Delta) + \varphi_{IF}) * C_{11} - cos(w_{IF} * (T_7 + \Delta) + \varphi_{IF}) * C_1 \quad (9)$$

Table 4. I/Q demodulator FIR filtered for odd order digital mixing coefficients of 7 samples

sample no: n	0	1	2	3	4	5	6	7
I-coefficients	1	0	-11	0	15	0	-5	0
Q-coefficients	0	5	0	-15	0	11	0	-1

Before we dive down to the derivation of memory mapping model and odd/even sampling, we need to develop the theory of odd sampling further by deriving the odd sampling expressions.

IV. METHODOLOGY ODD/EVEN ORDER SAMPLING WITH MEMORY

Since the proposed algorithm excludes the signal filtering stage, the filter phase Δ and coefficients C_n terms in equation 4 to 7 fall away. When we apply the ADC tuning terms which are controlled by the memory strobe the form presented in equation 4 becomes the new equation 10 below:

$$I_{odd} = \{(odd\_even\_adc\_sampling = 1)|\{cos(w_{IF} * T_1 + \varphi_{IF}) - cos(w_{IF} * T_3 + \varphi_{IF}) + cos(w_{IF} * T_5 + \varphi_{IF}) - cos(w_{IF} * T_7 + \varphi_{IF})\}\} \quad (10)$$

$$I_{odd} = \sum_{S_i=0}^{N} \{(odd\_even\_adc\_sampling = 1)|I_{raw}(S_i)\} \quad (11)$$

$$Q_{even} = \{(odd\_even\_adc\_sampling = 1)|\{sin(w_{IF} * T_2 + \varphi_{IF}) - sin(w_{IF} * T_4 + \varphi_{IF}) + sin(w_{IF} * T_6 + \varphi_{IF})\}\} \quad (12)$$

$$Q_{even} = \sum_{S_i=0}^{N} \{(odd\_even\_adc\_sampling = 1)|Q_{raw}(S_i)\} \quad (12)$$

Assuming sampling window of N samples as shown in equation 11, to store such a window a 2-bit strobe is used to tune the ADC in such a way that either the combination I_{odd}, Q_{even} or I_{even}, Q_{odd} are memory mapped as shown in Table 2. The memory is mapped in such a way that 8 bits addressing is achieved, furthermore memory data leak has been accounted for by introducing guard gaps. 8 bits addressing, storage of I_{odd} and Q_{even} for odd order sampling and guard gaps are presented in in Table 5.

$$dRM_{wr_s}^{rd^s} = \sum_{s_i=0}^{N} \left\{ \{(wr_s = 1 \; And \; s = 00)?\} | \left\{ \left\{ (s_i \; Mod \; 2 = 1)?| \sum_{i_s=0}^{256} I_{odd}(S_i), \right\} | \left\{ (s_i \; Mod \; 2 = 0)?| \sum_{q_s=269}^{525} Q_{even}(S_i), \right\} \right\} \right\} \quad (13)$$

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 1 September 2019 doi:10.20944/preprints201909.0014.v1

Equations 6, 7, 8 and 9 built up the derivation to the final form of the proposed odd order sampling with memory consideration. The full form of the proposed odd order sampling is presented in 13. The full form of this algorithm selects odd sampling by using s which controls the ADC sampling and dual port memory write location.

Table 5. Odd order sampling memory mapping

Input Addr	Dual Port Memory	Output Addr
0x00	I_odd_Sample_0	0x00
...	...	...
0xFF	I_odd_Sample_i	0xFF
data leak guard		
0x109	Q_even_Sample_0	0x109
...	...	...
0x208	Q_even_Sample_i	0x208
data leak guard		

V. METHOLOGY - SIMULATION OF ODD/EVEN ORDER SAMPLING

On the previous section a mathematical model for odd/even order ADC with internal tuning of sampling in such a way a selection between odd and even sampling is achieved with ease. In this section a simulation model that aims to compare performance of the odd/even order sampling model to first order delta-sigma model.

Simulation results for the Delta-Sigma sampling are shown in Figure 2 with quantization step size clearly defined. Quantization step size measurement attributes for the same Delta-Sigma sampling are given Figure 3 and table 7 below. These are compared to Figure 9 and Table 8. It can be clearly seen that the sampling frequency is reduced from approximately 8 kHz to 2 kHz.

Table 6. 1st Order Delta-Sigma quantization step size measurement results

Quantization Step Parameters	Value
ΔT	$124.687us$
ΔY	$0.1477\ volts$
ΔF	$8.020\ kHz$
$^{\Delta Y}/_{\Delta T}$	$1.185\ (^{volts}/_{ms})$

Simulation results for the odd/even order sampling are shown in Figure 4 and 5 with quantization step size clearly defined also. The architecture for even order sampling is like odd order sampling switch the difference being the selection of even samples instead of odd samples

Table 7. Even order quantization step size results

Quantization Step Parameters	Value
ΔT	$378.747us$

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 1 September 2019 doi:10.20944/preprints201909.0014.v1

ΔY	0.4120 $volts$
ΔF	2.640 kHz
$^{\Delta Y}/_{\Delta T}$	1.088 $(^{volts}/_{ms})$

Figure 7 to 9 compares performance of the different sampling techniques odd/even order registering a higher error rate due to big quantization step size.

VI. PERFORMANCE OF ODD/EVEN SAMPLING IN COMPARISON TO OTHER SCHEMES

We have performed experiments for quantization resolution from 2 to 12 bits. The results are depicted in Figure 2 and Table 9 respectively. The results are based on Realtime implementation on Xilinx FPGA development board with a clock frequency of 100MHz.

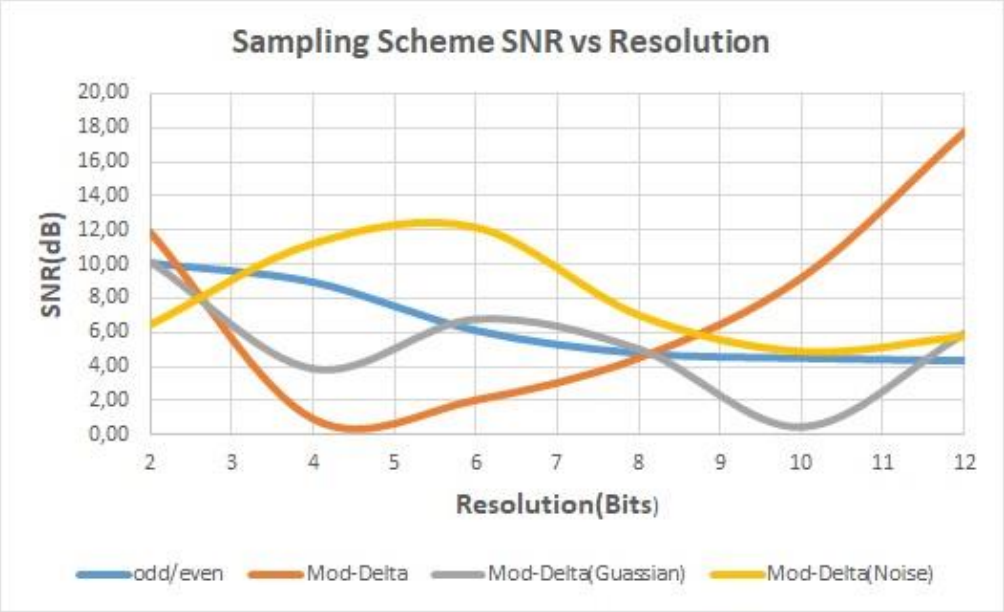

Figure 2. Performance of odd/even sampling to modulo ADC presented in [13]. We plot SNR vs quantization resolution rate for ideal modulo-delta process, gaussian process and field gathered noise process.

Figure 2 gives results for odd/even, Mod-Δ, Mod-Δ(Gaussian) and Mod-Δ(Noise) sampling schemes implemented on a Xilinx FPGA Platform. Below 3 bits resolution Mod-Δ has the worst performance than the other sampling schemes with 12 dB. Between 3 bits and 8 bits Mod-Δ has the best performance with SNR performance of below 6 dB, Mod-Δ(Noise) has the worst performance and odd/even has average performance. Above 8 bits odd/even and Mod-Δ(Gaussian) give the best performance compared to other sampling schemes recording performance of below 6 dB, while Mod-Δ has the worst recorded performance of 18 dB. This study shows that average best performance for sampling schemes below 6 dB SNR performance.

The implemented on a Xilinx FPGA platform with the waveform generated and stored in the FPGA DDR memory. Resource utilization for the proposed soft-core architecture for odd/even order sampling is presented in Table 18 with total resource utilization seating at below 50%.

Preprints (www.preprints.org) | NOT PEER-REVIEWED | Posted: 1 September 2019 doi:10.20944/preprints201909.0014.v1

Table 8. Resource Utilization for odd/even order sampling

	Used	Available	Utilization
SliceUtilization			
Slice LUTs	2044	14400	14.19%
LUT as Logic	1828	14400	12.69%
LUT as Memory	216	6000	3.60%
SliceRegUtilization			
Reg as Flip Flop	3158	28800	10.97%
Reg as Latch	0	28800	0.00%
MultiplexerUtilization			
F7 Muxes	52	8800	0.59%
F8 Muxes	5	4400	0.11%
MemoryUtilization			
Block RAM	1.5	50	3.00%
DSPUtilization			
DSPs	0	66	0.00%
SpecificFeatureUtilization			
XADC	0	1	0.00%
Total Utilization			45,15%

VII. CONCLUSIONS

This paper presented a novel odd/even order sampling I/Q modulator system. The system was used in a development of prototype Electronic Warfare system. In Electronic Warfare mixed signal processing is a necessity since the received Radar is analogue in nature while Electronic Counter Measure (ECM) and Electronic Support Measure (ESM) processing is digital in nature. Simulink model and empirical experimental design were used to investigate design elements such as sampling frequency and memory mapping. The impact of sampling frequency on memory mapping optimization was investigated on the empirical experimental setup. Simulation results comparing the proposed odd/even order sampling to first order delta-sigma sampling showed a reduced sampling frequency from 8kHz to 2kHz, that's sample reduction frequency of quarter without losing signal integrity such as phase and dynamic range. Experimental comparing odd/even order sampling to standard ADC sampling showed an improved memory storage requirement from 512 bytes to 256 bytes, and improved sample frequency by half with only the phase being compromised while amplitude remained unaffected. Future work includes the development of Electronic Warfare (EW) System on Chip (EWSoC), the work proposed in this paper accompanied by Versal: Adaptive Compute Acceleration Platform (ACAP) and Radio Frequency System on Chip (RFSoC) from Xilinx are positive efforts towards EWSoC.

References

[1] V. I. Slyusar, "I/Q-DEMODULATION OF THE ODD ORDER," in International Conference on Antenna Theory and Techniques,, Kharkiv, Ukraine, 2015.

[2] J.-E. Eklund and R. Arvidsson, "A Multiple Sampling, Single A/D Conversion Technique for I/Q Demodulation in CMOS," in IEEE JOURNAL OF SOLID-STATE CIRCUITS, DECEMBER 1996.

[3] I. Mashkin, A. Nikolaev and N. Nikitin, "Assessing the Impact of Analog-to-digital Converter Resolution

on the Phase Difference Measurement Error in a Digital Receiver," in International Scientific & Technical Conference "Dynamics of Systems, Machanisms and Machines", Omsk, Russia, 13-15 November 2018.

[4] D. Budanov, M. Pilipko and D. Morozov, "Encoders for flash analog-to-digital converters," in 2018 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering, Moscow, Russia, 29 Jan - 1 Feb 2018.

[5] A. Mohammadi and M. Chahardori, "A Low-power, Bootstrapped Sample and Hold Circuit with Extended Input Range for Analog-to-Digital Converters in CMOS 0.18 μm," in 2018 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Prague, Czech Republic, 2-5 July 2018.

[6] V. N. Ashanin and A. Korotkov, "Realisation of Integrating Analog-Digital Converter with Intermediate Time-Impulse Modulation Using NI Multisim," in 2018 Moscow Workshop on Electronic and Networking Technologies (MWENT), Moscow, Russia, 14-16 March 2018.

[7] M. Abdelkader, A. Ali, A. Abdelaziz, M. W. Ismail, M. A. Refky and Y. Ismail, "A 200MS/s, 8-bit Time-based Analog to Digital Converter (TADC) in 65nm CMOS technology," in 2016 Fourth International Japan-Egypt Conference on Electronics, Communications and Computers (JEC-ECC), Cairo, Egypt, 31 May-2 June 2016.

[8] A. Glascott-Jones, M. Wingender, F. Bore, M. Stackler, N. Chantier, K. Salmi, P. Coquille, M. Martin, V. Monier, G. Wagner, E. Savasta, D. Bellin, R. Pilard and J. Duvernay , "Results from a Prototype 6GSps Digital to Analogue Converter with greater than 7 GHz Analogue Bandwidth.," in 2016 11th European Microwave Integrated Circuits Conference (EuMIC), London, UK, 3-4 Oct. 2016.

[9] T. Waho, "Analog-to-Digital Converters Using Not Multi-level But Multi-bit Feedback Paths," in 2017 IEEE 47th International Symposium on Multiple-Valued Logic (ISMVL), Novi Sad, Serbia, 22-24 May 2017.

[10] M.-K. JEON, W.-J. YOO, C.-G. KIM and C. YOO, "A Stochastic Flash Analog-to-Digital Converter Linearized by Reference Swapping," in 2017 IEEE. Translations and content mining are permitted for academic research, 26 October 2017.

[11] S. Jia, . L. Weng, W. Wang and Y. Wang, "A highly linear 5GS/s voltage-to-time converter for time-based analog-to-digital converters," in 2017 IEEE Asia Pacific Microwave Conference (APMC), Kuala Lumpar, Malaysia, 11 January 2018.

[12] P. Dhage and P. Jadhav , "Design of Power Efficient Hybrid FlashSuccessive Approximation Register Analog to Digital Converter," in 2017 International Conference on Communication and Signal Processing (ICCSP), Chennai, India, 08 February 2018.

[13] O. Ordentlich, G. Tabak, P. K. Hanumolu, A. C. Singer and G. W. Wornell, "A Modula-Based Architecture for Analog-to-Digital Conversion," IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, vol. 12, no. 5, pp. 825 - 840, October 2018.

[14] D. Behera,, R. S. Kumar and N. Krishnapura, "Reset-Free Memoryless Delta–Sigma Analog-to-Digital Conversion," in 2018 IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I, NOVEMBER 2018.

[15] X. Ding, K. Hofmann, L. Zhang, D. Yi and Y. Ma, "Redundant Double Conversion based Digital Background Calibration of SAR ADC with Convergence Acceleration and Assistance," in Proceedings of the 25th International Conference "Mixed Design of Integrated Circuits and Systems", Gdynia, Poland, June 21-23, 2018.

[16] P. Cruz, T. Alves and A. Cartaxo, "Relaxing the ADC Sampling Rate in High-Resolution Radar Systems Through Photonic Analogue-to-Digital Conversion," in 2018 20th International Conference on Transparent Optical Networks (ICTON), Bucharest, Romania, 1-5 July 2018.

[17] D. Budanov, D. Morozov and M. Pilipko, "An 8-bit Analog-to-Digital Converter With a Novel Encoder Using 90 nm CMOS," in 2018 IEEE International Conference on Electrical Engineering and Photonics (EExPolytech), St. Petersburg, Russia, 22-23 Oct. 2018.

[18] P. Yang, Y.-J. Cen, Y.-K. Li and D.-G. Li, "The Design of High Resolution Capacitance Array in SAR ADC," in 2018 IEEE 18th International Conference on Communication Technology (ICCT), Chongqing, China, 8-11 Oct. 2018.

[19] M. Pilipko and M. Manokhin, "Design of a Low-Power 12-bit SAR ADC," in 2019 IEEE Conference of

Russian Young Researchers in Electrical and Electronic Engineering (EIConRus), Saint Petersburg and Moscow, Russia, Russia, 28-31 Jan. 2019.

[20] B. Rahrovi, "A Review and Comparison of the DSP-Based Resolver to Digital Conversion Methods," in 2019 IEEE Texas Power and Energy Conference (TPEC), College Station, TX, USA, USA, 7-8 Feb. 2019.

[21] X. GUO, G. MEHDI, M. ASIF, A. HU and J. MIAO, "1-Bit/2-Level Analog-to-Digital Conversion Based on Comparator and FPGA for Aperture Synthesis Passive Millimeter-Wave Imager," IEEE Access, vol. 7, pp. 51933 - 51939, 12 April 2019.

[22] M. A. Bensenouci, H. Escid and M. Attari, "Neural network-based non-linear A/D conversion," in 2015 IEEE International Circuits and Systems Symposium (ICSyS), Langkawi, Malaysia, 28 January 2016.

[23] H. Xu, L. Wang, R. Yuan and Y. Chang, "A/D converter background calibration algorithm based on neural network," in 2018 International Conference on Electronics Technology (ICET), Chengdu, China, 23-27 May 2018.

[24] M. Giordano, G. Cristiano, K. Ishibashi, S. Ambrogio, H. Tsai, G. W. BGurr and P. Narayanan, "Analog-to-Digital Conversion With Reconfigurable Function Mapping for Neural Networks Activation Function Acceleration," IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 9, no. 2, pp. 367 - 376, June 2019.

[25] G. Vougioukas, P. N. Alevizos and A. Bletsas, "Coherent Detector for Pseudo-FSK Backscatter Under Ambient Constant Envelope Illumination," in 2018 IEEE 19th International Workshop on Signal Processing Advances in Wireless Communications (SPAWC), Kalamata, Greece, 27 August 2018.

[26] X. Ma, L. Li, S. Ming, X. F. I. You and J. Lin, "Envelope Detection for an ADC-Relaxed Double-Sideband Low-IF CW Doppler Radar," IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 12, pp. 5833 - 5841, 20 September 2018.

[27] A. Golan, A. Etinger, M. Einat and Y. Pinhasi, "Digital Signal Detection by a Glow Discharge Detector," IEEE Transactions on Plasma Science, vol. 47, no. 1, pp. 95 - 99, Jan. 2019.

[28] B. Thijssen, E. Klumperink, P. Quinlan and B. Nauta, "Feedforward Phase Noise Cancellation Exploiting a Sub-Sampling Phase Detector," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 11, pp. 1574 - 1578, Nov. 2018.

[29] J. Mitra, and T. K. Nayak, "An FPGA-Based Phase Measurement System," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 1, pp. 133 - 142, Jan. 2018.

[30] I. L. Syllaios, "Hybrid ΔΣ Programmable Phase/Frequency Detector for IoT Chipsets," in 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 04 May 2018.

[31] B. Ga¸sowski, S. Hanasz, K. Czuba and Ł. Zembala, "Influence of step recovery diode DC bias on AM/P conversion in sampling phase detectors," in 2018 22nd International Microwave and Radar Conference (MIKON), Poznan, Poland, 09 July 2018.

[32] J. Lin, Z. Song, N. Qi, W. Rhee, Z. Wang, and B. Chi , "A 77-GHz mixed-mode FMCW signal generator based on bang-bang phase detector," in 2017 IEEE Asian Solid-State Circuits Conference (A-SSCC), Seoul, South Korea, 28 December 2017.

[33] E. G. Kacharmina, A. A. Timofeev, V. V. Chudnikov and B. I. Shakhtarin, "Pulse phase-frequency detectors in high-speed frequency synthesizers," in 2018Systems of Signal Synchronization, Generating and Processing in Telecommunications (SYNCHROINFO), Minsk, Belarus, 10 September 2018.

[34] J. Han and R. Chen, "RF MEMS In-Line Type Phase Detector With Large Dynamic Range," IEEE Electron Device Letters, vol. 40, no. 5, pp. 792 - 795, May 2019.

[35] Xilinx, "Versal: The First Adaptive Compute Acceleration Platfrom(ACAP)," Xilinx, October 2018.