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Sol–gel deposited ceria thin films as gate dielectric for CMOS technology

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Abstract. **In this work, cerium oxide thin films were prepared using cerium chloride heptahydrate, ethanol and citric acid as an additive by sol–gel spin-coating technique and further characterized to study the various properties. Chemical composition of deposited films has been analysed by FTIR which shows existence of CeO_2. The samples have been optically characterized using ellipsometry to find refractive index of 2·18 and physical thickness which is measured to be 5·56 nm. MOS capacitors were fabricated by depositing aluminum (Al) metal using the thermal evaporation technique on the top of CeO_2 thin films. Capacitance–voltage measurement was carried out to calculate the dielectric constant, flat-band voltage shift of 18·92, 0·3–0·5 V, respectively and conductance–voltage study was carried out to determine the D_{it} of $1{\cdot}40 \times 10^{13}$ eV^{-1} cm^{-2} at 1 MHz.**

Keywords. **High-k; CeO_2; gate dielectric; sol–gel; FTIR; XRD; CV.**

1. Introduction

In the current era of nanotechnology, the semiconductor device industries require high dielectric (high-k) materials for gate dielectric applications in advance CMOS circuits. The different dielectric layers are being used as gate oxide in MOSFETs, as capacitor to store charge in memory devices and as an insulator in back-end interconnects (Rathee *et al* 2010). Earlier, the SiO_2 was the most promising dielectric material of choice for all these applications (Houssa *et al* 2006). The semiconductor roadmap following Moore's law is responsible for an exponential decrease of minimum feature size of devices. But, in order to follow Moore's law, the current trends are use of nanoelectronics and technological research towards the scaling down of devices to smaller physical dimensions (Guha and Narayanan 2009). The decrease in device feature size offers increased speed, low power consumption and low cost because of the increased density of devices per wafer as per ITRS. This size reduction presents challenges for the various SiO_2 applications due to the quantum mechanical effects as the thickness of conventional SiO_2 gate insulators is reduced just to a few atomic layers, electrons can tunnel directly through the films and cause leakage currents resulting in increase of power dissipation to unacceptable levels, heat becomes critical issue and reduces device reliability (Gusev 2006).

In order to maintain low power consumption performance of CMOS transistors, high-k gate dielectrics must be employed to replace conventional SiO_2/SiON as the scale of the channel length goes down to sub-100 nm feature size. Alternative gate dielectric needs the stringent requirements including high permittivity, thermal stability, high level film and interface quality, processing and materials compatibility with fabrication of CMOS devices and long-term reliability for practical replacement of SiO_2/SiON (Wilk *et al* 2001). Many materials have been investigated as candidates for this replacement. Among all the high-k dielectrics, amorphous metal oxides, such as unary metal oxide of Al_2O_3 (Gusev *et al* 2000), CeO_2 (Kang *et al* 1998; Inoue *et al* 1999), HfO_2 (Lee *et al* 2000; Wilk *et al* 2000) and ZrO_2 (Zhong *et al* 2001) and binary systems of $(Y_2O_3)_x(ZrO_2)_{1-x}$ (yttria-stabilized ZrO_2) (Wang *et al* 2000), $LaAlO_3$ (Xiang *et al* 2003) and $(HfO_2)_x(Al_2O_3)_{1-x}$ (Yu *et al* 2002), have been shown to be the most promising high-k gate dielectrics due to their high dielectric constant, excellent thermal stability and good compatibility with modern electronics processing techniques.

Recently, the rare earth cerium oxide (CeO_2) has been reported to be a potentially promising alternative gate dielectric to replace the conventional SiO_2 with a lot of potential advantages (Quah *et al* 2010, 2011; Lim *et al* 2011) for CMOS applications such as: high-dielectric constant ($k \sim 26$), large bandgap (~5·5 eV), fluorite structure with very small lattice mismatch of ~0·35%, high thermodynamic stability and good interface with Si substrate. The film's structure and interface properties depend upon deposition processes. Several deposition techniques have been reported in literature for the preparation of CeO_2 films on Si for CMOS devices, including sputtering (Wang *et al* 2001), vacuum evaporation (Inoue *et al* 1990), MBE (Joumori *et al* 2004), PLD (Karakaya *et al* 2006), MOCVD (Ami and Suzuki 1998), and E-beam evaporation (Inoue *et al* 1999), etc. All these techniques require high temperature treatments which usually induces a deterioration of the device performance and reliability. Therefore, for silicon-based nanoelectronics device fabrication, low temperature processes are strongly desired.

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The present paper is concerned with the deposition of spin-coated CeO_2 films prepared using an ethanolic precursor sol containing citric acid as an additive. The deposited CeO_2 films have been characterized by XRD, FTIR and ellipsometer for microstructural, chemical and optical properties and also capacitance–voltage (C–V) measurement is carried out for studying some of the electrical properties. This work attempts to explore the properties of ceria for gate dielectric applications in CMOS devices. Experimental details are presented in the second section and the results are discussed in the third section of the paper whereas the fourth section concludes the paper.

2. Experimental

Sol–gel derived CeO_2 films were deposited on commercially available p-type Si (1 0 0) wafers with resistivity ~10–20 Ω-cm. The silicon substrates were cleaned using trichloro-ethylene (Himedia), acetone and methanol with 5 min heat treatment, respectively, followed by rinse in deionized water (DI). Ceria sol was prepared by dissolving 2·5 g cerium chloride heptahydrate ($CeCl_3 \cdot 7H_2O$, make-Himedia) as source of ceria in 30 ml ethanol, followed by the addition of citric acid (Fisher Scientific) precursor in 1:1·0 mole ratio. Then solution was spin coated (Milman-2000S) at a spinning speed of 6000 rpm for 30 s on Si. These spin-coated films were heat treated for 5 min in air in an electric furnace at 400 °C. The metal and substrate contacts were formed by depositing aluminum metal using the thermal evaporation (Hind-HIVAC) system for MOS capacitor fabrication. The native oxide at the backside of Si was removed by the hydrofluoric acid followed by rinsing in deionized water and then the bulk contact of Al was formed by using thermal evaporation system at the backside of Si. The electrical connections are taken from top metal electrode and backside substrate contact. The deposited films were characterized by ellipsometer (Philips SD-1000), Fourier transform infrared spectroscopy (FTIR) and X-ray diffraction. Capacitance–voltage (C–V) and conductance–voltage (G–V) measurements have been carried out using (Agilent 4284 A) LCR meter. Electrical dielectric constant and density of interface traps (D_{it}) have been determined with the help of C–V and G–V curves.

2.1 *MOS structure*

The MOS capacitor structure is shown in figure 1(a), it consists of metal–oxide–semiconductor regions. Electrical contacts are made to the metal gate and the back contact to the semiconductor. Accumulation occurs typically for negative voltages (p-Si substrate), where the negative charge on the gate attracts holes from the substrate to the oxide–semiconductor interface. Depletion occurs for positive voltages; the positive charge on the gate pushes the mobile holes into the substrate, thereby depleting the semiconductor of the mobile carriers and leaving a negative charge in the space

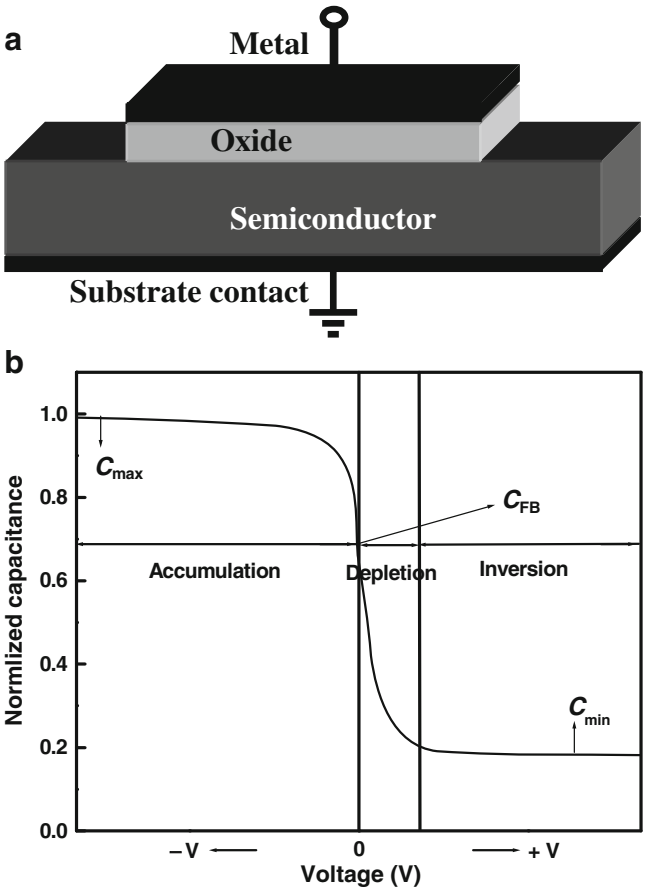

Figure 1. **a.** Cross section of MOS capacitor structure and **b.** C–V characteristics of MOS structure at high frequencies.

charge region which is due to the ionized acceptor ions. The voltage separating the accumulation and depletion regime is referred to as the flatband voltage as shown in figure 1(b). Inversion occurs at more positive voltages which are larger than the threshold voltage. In addition to the depletion layer charge, a negatively charged inversion layer forms at the oxide–semiconductor interface.

2.2 *Concept of equivalent oxide thickness (EOT)*

The gate oxide thickness required for good MOSFET control actually depends on the capacitance of the film. Capacitance is given by

$$C = k\varepsilon_0 A/t_{ox}, \tag{1}$$

where k is the dielectric constant, A the area and t_{ox} the thickness.

Silicon dioxide (SiO_2) has a k value of 3·9, if an alternate material could be found with a higher k value, then the same capacitance per unit area A could be achieved with a physically thicker film and potentially lower leakage. Comparison

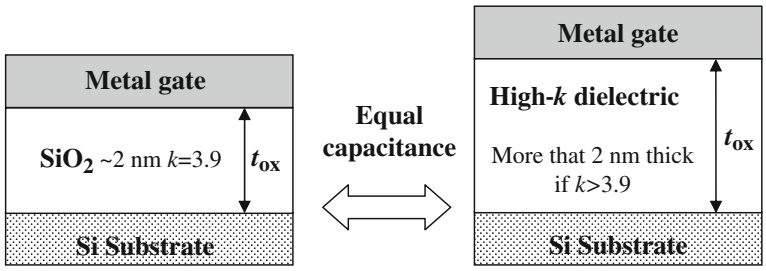

Figure 2. Comparison of gate dielectrics used in transistor gate stacks. Both structures result in same gate stack capacitance.

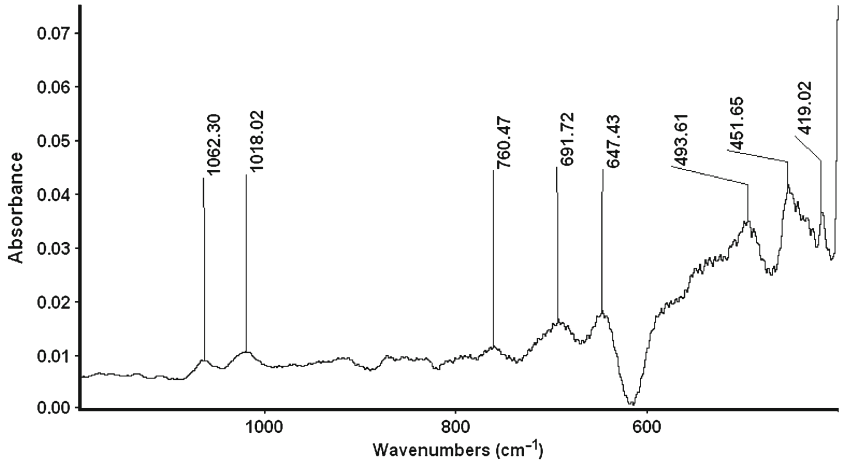

Figure 3. FTIR spectra of CeO_2 film annealed at 400 °C.

of various films and thickness that would result is done using the concept of equivalent oxide thickness (EOT) (figure 2). EOT is given by:

$$\text{EOT} = \left(k_{\text{SiO}_2} t_{\text{ox}}\right)/k_{\text{x}}, \tag{2}$$

where k_{x} is the k value for the film of interest, t_{ox} the physical thickness of the film of interest and k_{SiO_2} the k value of silicon dioxide. From (2), a film with a k value of 7 could be almost twice as thick as a silicon dioxide film with a k of 3·9 and still have the same control over MOSFET.

3. Results and discussion

3.1 *Ellipsometer*

Thickness and refractive index of the cerium dioxide thin film are measured with ellipsometer (Philips SD1000) at the visible wavelength of 632·8 nm using single point measurement technique. The measured average value of physical thickness is 5·56 nm and refractive index is 2·18. The EOT determined for deposited film is 1·14 nm. The measured value of refractive index is comparable to the (2·13–2·33) reported by Quah *et al* (2010) for CeO_2 deposited by the metal–organic decomposition method (MOD).

3.2 *Fourier transform infrared spectroscopy (FTIR)*

Figure 3 shows FTIR spectra of the deposited cerium oxide thin film. The FTIR analysis was carried out to obtain information about chemical bonding characteristics. The spectrum is shown in the range of 400–1200 cm^{-1}. The spectrum shows the existence of both Ce- and Si-oxide phases. The peaks from 500–800 cm^{-1} are due to the presence of Ce–O bond (Wang *et al* 2001). In the present spectra of the film, peak at 647·43 cm^{-1} is corresponding to Ce–O bond, the Si–O bond appears at 1062·30 cm^{-1} and the broad O–H bond has been detected at 3381 cm^{-1} (not shown) which may be due to the presence of moisture, however, it can be reduced by annealing the deposited CeO_2 films at higher annealing temperatures. The presence of Si–O bond shows existence of interfacial SiO_2 between Si substrate and CeO_2.

3.3 *XRD*

The crystal structure of the film is verified with X-ray diffraction (XRD). Figure 4 shows XRD spectra of CeO_2 film annealed at 400 °C. Mixed phase of CeO_2 peaks with JCPDS card no. 034-0394 and 44-1001 were detected. Three diffraction peaks, which were ascribed to cubic phases of CeO_2, were detected at (2 0 0), (2 2 0) and (3 1 1) and one

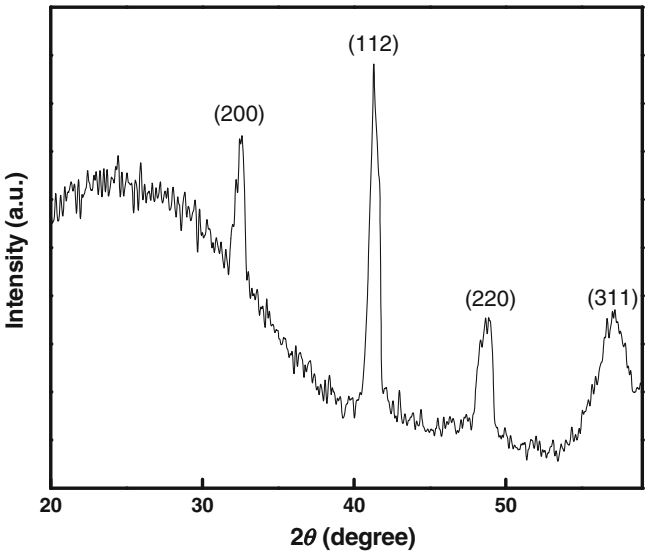

Figure 4. XRD spectra of CeO_2 film annealed at 400 °C.

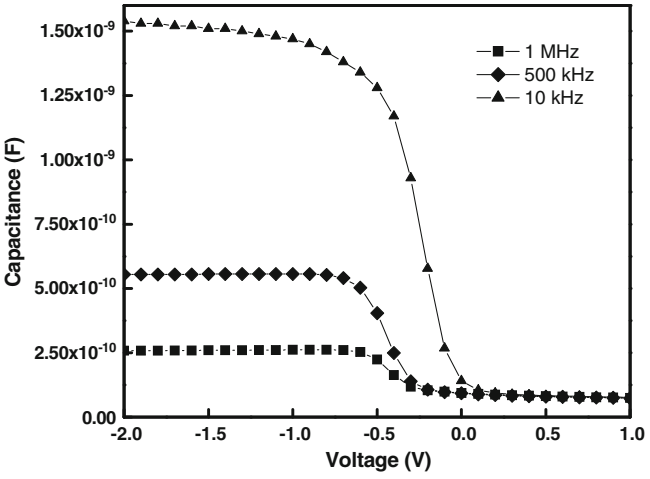

Figure 5. C–V characteristics of Al/CeO_2/Si MOS capacitor.

diffraction peak which was ascribed to hexagonal phase of CeO_2 was detected at (1 1 2). These peaks are in well agreement with the CeO_2 films deposited by MOD (Quah *et al* 2010). Diffraction plane of (1 1 2) reveals the maximum peak intensity as compared to other peaks. Hence it is considered that a preferred oriented (1 1 2) plane is produced.

3.4 *C–V and G–V characteristics*

Al/CeO_2/p-Si MOS capacitor was characterized by the Agilent 4284A LCR meter for the measurements of electrical properties of the fabricated MOS structure at different frequencies. A typical C–V characteristics curve of MOS structure is shown in figure 5. The dispersion observed in the accumulation region is due to the substrate series resistance, R_s, which mainly affects the high-frequency C–V curve. The C–V curves are corrected for the

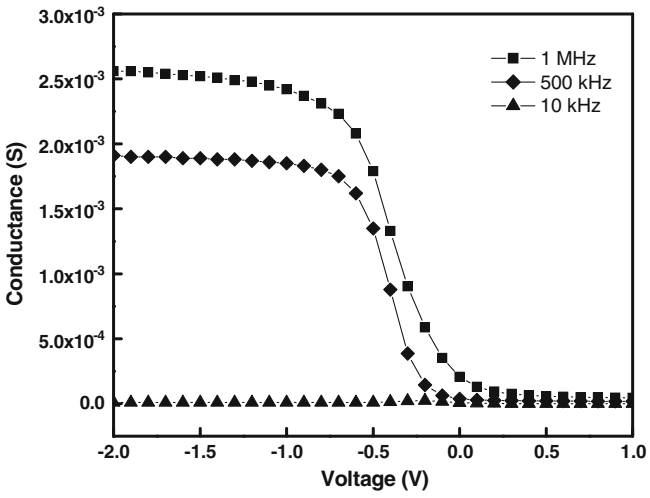

Figure 6. G–V characteristics of Al/CeO_2/Si MOS capacitor.

determination of the dielectric constant (Wu *et al* 2006). The dielectric constant determined from accumulation capacitance of C–V curve obtained at measurement frequency of 1 MHz is 18·92. The determined k value appears to be lower than the expected may be due to the growth of undesired SiO_x interface layer at the CeO_2/p-Si interface upon high temperature treatment in an open air as observed in the FTIR spectra. The value of equivalent oxide thickness using dielectric constant of 18·92 and electrode area of $3{\cdot}14 \times 10^{-4}$ cm^2 is calculated as 1·14 nm. There is a slightly negative shift (0·3–0·5 V) in the flat-band voltage (V_{FB}) observed from figure 5 due to the presence of positive effective oxide charges (Q_{eff}) located in CeO_2 thin film. The Q_{eff} is found by using (3) and thus calculated as $7{\cdot}69 \times 10^{12}$ cm^{-2} (Cheong *et al* 2008). The conductance–voltage (G–V) measurement as shown in figure 6, was employed to investigate the density of trapped charges at the CeO_2/Si interface. The density of trapped charges (D_{it}) calculated from the Hill–Coleman method (Oulachgar *et al* 2007) using (4). The obtained values of D_{it} at 1 MHz, 500 and 10 kHz are $1{\cdot}40 \times 10^{13}$ eV^{-1} cm^{-2}, $2{\cdot}00 \times 10^{13}$ eV^{-1} cm^{-2} and $7{\cdot}37 \times 10^{12}$ eV^{-1} cm^{-2}, respectively which can be further minimized by annealing the films in different ambient at higher temperatures. The obtained D_{it} value appears to be higher as compared with others (Quah *et al* 2010, $\sim 2{\cdot}5 \times 10^{12}$ eV^{-1} cm^{-2}) which may be due to the trapping of charges in SiO_x interfacial layer observed in the FTIR spectra.

$$Q_{eff} = \frac{\Delta V_{FB} C_{ox}}{qA}, \tag{3}$$

where C_{ox} is the oxide capacitance, q the electronic charge, A the electrode area and ΔV_{FB} the flat band voltage shift.

$$D_{it} = \frac{2\omega C_{ox}^2 G_{max}}{qA\left\{G_{max}^2 + \omega^2 [C_{ox} - C_m(G_{max})]^2\right\}}, \tag{4}$$

where C_m is the maximum capacitance, G_{max} the maximum conductance and ω the frequency.

4. Conclusions

In this work, CeO_2 thin film having a thickness of 5·56 nm was successfully deposited by the sol–gel technique on *p*-Si substrate. The dielectric constant value of the deposited CeO_2 film is 18·92 and an equivalent oxide thickness is 1·14 nm. The dielectric constant is observed to be lower than its ideal (∼26) value due to the growth of low-*k* interfacial layer of SiO_x as seen in FTIR spectra. The FTIR spectra confirms the deposition of CeO_2 film. CV measurement showed negative shift in flat-band voltage and positive effective oxide charges. The value of Q_{eff} determined to be $7{\cdot}69 \times 10^{12}$ cm^{-2}. From the aforementioned observations, deposited CeO_2 thin films on *p*-Si can be promising alternative gate dielectric candidate for application in CMOS technology due to its higher dielectric constant and lower EOT.

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References

Ami T and Suzuki M 1998 *Mater. Sci. Eng.* **B54** 84

Cheong K Y, Moon J H, Kim H J, Bahng W and Kim N-K 2008 *J. Appl. Phys.* **103** 084113

Guha S and Narayanan V 2009 *Annu. Rev. Mater. Res.* **39** 181

Gusev E P 2006 *IBM J. Res. & Dev.* **50** 387

Gusev E P, Copel M, Cartier E, Baumvol I J R, Krug C and Gribelyuk M A 2000 *Appl. Phys. Lett.* **76** 176

Houssa M *et al* 2006 *Mater. Sci. Eng.* **R51** 37

Inoue T, Yamamoto Y, Koyama S, Suzuki S and Ueda Y 1990 *Appl. Phys. Lett.* **56** 1332

Inoue T, Yamamoto Y and Satoh M 1999 *Thin Solid Films* **343** 594

Joumori S, Nakajima K, Suzuki M, Kimura K, Nishikawa Y, Matsushita D, Amaguchi T and Satou N 2004 *Jpn J. Appl. Phys.* **43** 7881

Kang J F, Ziong G C, Lian G J and Han R Q 1998 *Solid State Commun.* **108** 225

Karakaya K, Zinine A, van Berkum J G M, Verheijen M A, Rittersma Z M, Rijnders G and Blank D H A 2006 *J. Electrochem. Soc.* **153** F233

Lee B H, Kang L, Nieh R, Qi W J and Lee C J 2000 *Appl. Phys. Lett.* **76** 1926

Lim W F, Cheong K Y and Lockman Z 2011 *Appl. Phys.* **A103** 1067

Oulachgar E H, Aktik C, Scarlete M, Dostie S, Sowerby R and Gujrathi S 2007 *Appl. Phys. Lett.* **101** 084107

Quah H J, Cheong K Y, Hassan Z, Lockman Z, Jasni F A and Lim W F 2010 *J. Electrochem. Soc.* **157** H6

Quah H J, Lim W F, Cheong K Y, Hassan Z and Lockman Z 2011 *J. Crystal Growth* **326** 2

Rathee D, Kumar M and Arya S K 2010 *Int. J. Comp. Appl.* **8** 10

Wang S J, Xu S Y, You L P, Lim S L and Ong C K 2000 *Semicond. Sci. Technol.* **13** 362

Wang L P, Tang B Y, Huang N, Tian X B and Chiu P K 2001 *Mater. Sci. Eng.* **A308** 176

Wei-Hao W, Tsui B-Y, Chen M-C, Hou Y-T, Jin Y and Jao H-J 2006 *Appl. Phys. Lett.* **89** 162911

Wilk G D, Wallace R M and Anthony J M 2000 *J. Appl. Phys.* **87** 484

Wilk G D, Wallace R M and Anthony J M 2001 *J. Appl. Phys.* **89** 5243

Xiang W F, Lu H B, Yan L, Guo H L and Yang G Z 2003 *J. Appl. Phys.* **93** 533

Yu H Y, Li M F, Cho B J, Yeo C C, Joo M S, Zheng J Z and Ramanathan S 2002 *Appl. Phys. Lett.* **81** 376

Zhong H C, Heuss G, Misra V, Luan H, Lee C and Kwong D L 2001 *Appl. Phys. Lett.* **78** 1134