This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2017.Doi Number

Solar PV-fed Multilevel Inverter with Series Compensator for Power Quality Improvement in Grid-Connected Systems

Devalraju Prasad[1], Graduate Student Member, IEEE, Dhanamjayulu C[1], Senior Member, IEEE.

[1]School of Electrical Engineering, Vellore Institute of Technology, Vellore, Tamilnadu, India.

Corresponding author: C. Dhanamjayulu (e-mail: dhanamjayulu.c@vit.ac.in)

"This work was supported by Vellore Institute of Technology, Vellore, Tamilnadu, India through the research fund RGEMS under VIT SEED GRANT/12439."

ABSTRACT Power quality difficulties arise as a result of Renewable Energy Sources (RES) integrating with the grid. Voltage swell, sag, and harmonic distortion occur on the grid due to power quality issues, which have an impact on customers. An inexpensive series compensator, like the Dynamic Voltage Restorer (DVR), is the best solution for overcoming the aforementioned problems. In this article, a solar PV integrated DVR with a novel multilevel inverter is introduced to address the power quality issues in the grid. The main objective of the proposed work is to develop a DVR integrated with a 23-level multilevel inverter to enhance the power quality. In addition, an improved INC-MPPT technique is designed for the boost converter for maximum energy extraction from the solar PV modules. Despite numerous benefits of multilevel inverters, there exist several reliability challenges such as fewer component counts and reduced THD. The suggested topology can able to generate 23 levels of output voltage with asymmetrical DC sources. The MLI has several advantages such as a reduction in the overall component count, cost and size of the inverter. Additionally, a detailed mathematical analysis is presented for the rotating dq reference frame control. The dynamic performance of the DVR is evaluated with a balanced load and implemented experimentally. Simulation results of the proposed system are carried out using MATLAB/Simulink. The proposed system is implemented using a dSPACE controller with a laboratory hardware prototype and OPAL-RT real-time simulator setup as well. The results show that the design of the proposed system is more effective at compensating for voltage sag and improves the power quality significantly. The THD obtained at the grid side is lower, which is under IEEE standards.

INDEX TERMS Enhanced INC MPPT technique, Photovoltaic array, Dynamic voltage restorer, Power quality, multilevel inverter.

ABBREVIATIONS AND NOMENCLATURE

CPD	: Custom Power Devices
DVR	: Dynamic Voltage Restorer
PQ	: Power Quality
RES	: Renewable Energy Sources
INC MPPT	: Incremental Conductance MPPT
EINC	: Enhanced Incremental Conductance
MLI	: Multilevel Inverter
THD	: Total Harmonic Distortion
MV	: Medium Voltage
MBV	: Maximum Blocking Voltage
TSV	: Total Standing Voltage
SIMO	: Single-Input Multi-Output
PSC	: Pre-Sag Compensation
VSI	: Voltage Source Inverter
NLC	: Nearest Level Control
N_{DC}	: Number of DC sources
N_{Lev}	: Number of Levels
N_{SW}	: Number of Switches
N_{GDK}	: Number of Gate Driver Circuits
V_T	: Thermal Voltage
γ	: Ideality Constant
I_o	: Saturation Current
T_c	: Cell Temperature
β	: Coefficient of Temperature
G_n	: Normal Value of Irradiation
α	: Duty Ratio
f_s	: switching frequency
ϕ	: phase angle

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and
content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

δ : phase angle jump
V_G^{Sag} : Grid voltage at sag
e_r : Error signal
ΔI_L and ΔV_{dc} : Current and Voltage ripple factors

I. INTRODUCTION

In the smart era, microprocessor-controlled devices, or digital, electronic, and non-linear devices, are extensively used in all sectors of the industry. Nearly all of these devices are sensitive to electrical supply disruptions at any minute and cannot be operated properly. Problems that happen because of inadequate power quality are data errors, automatic resets, memory loss, UPS alarms, equipment failure, software corruption, circuit board failure, power supply problems, and overheating of electrical distribution systems. Considering these realities, PQ has become progressively more critical [1]. The use of sensitive loads such as diagnostic apparatus in health centers, educational institutions, detention centers, etc. over several years has been fourfold, which has led to a concern with the quality of power of sensitive loads [2]. The essential power quality issues include voltage swells, sags, harmonics, transients, flickers, fluctuations, and interruptions [3]. The sensitive and critical loads must prevent these issues in terms of power quality and voltage disturbances. In this regard, a wide range of solutions has been introduced, including the best and most efficient solution for the compensation and mitigation of voltage disturbances known as Custom Power Devices (CPDs). The DVR is the best CPD since it has low cost, is small in size, and can respond quickly to voltage disturbances [4], [5].

In grid-connected networks, dynamic voltage restorers (DVR) play a significant role in minimizing voltage disruptions. The grid voltage changes are controlled in grid systems by an energy-efficient photovoltaic (PV)-based DVR with a proportional controller and a new boost converter [6]. Renewable energy sources, as well as DC-DC converters in various topologies accessible today, are very essential for energizing electronics [7]. PV integration helps to generate clean, renewable energy while also lowering pollution levels. It can support important loads in the event of a grid outage, boosting reliability while simultaneously addressing energy issues. Furthermore, integrating PV and DVR while fulfilling energy demands reduces harmonics, voltage dips, and improves power factor.

In many industrial applications, MLIs have found their extensive influence such as UPFC, drives with high power and medium voltage, DSTATCOM, electric vehicles (EV), active power filters, DVR, micro-grid, grid integrated or stand-alone PV systems, and other fields [8]. Half-bridge inverter [9] and H-Bridge (full-Bridge) inverter [10] are familiar inverter topologies in single-phase DVR. Besides that numerous multilevel inverters, matrix converters, and Impedance-fed inverters [11] are used for both single and three-phase DVRs. AC-AC converter-based DVRs [12] are used to enhance the power quality in the absence of a dc-link capacitor. However, during voltage sag AC-AC converters draw huge current from the grid. Thus, these are not suitable for long-duration voltage sag mitigation in weak grids. For deep voltage sag, Z-source converter-based DVR with less dc-link voltage was presented [13], though it needs storage as well as a risk of shoot-through. Typical three-phase DVR inverter topologies include the full-bridge, four-leg six-switch, and six-switch split capacitor configurations.

However for higher power voltage source inverters with two-level are not suitable because the switches will block large voltage, and more dv/dt creates electromagnetic interference to overcome these problems multilevel inverter (MLI) is the best solution. The benefits of MLIs are lower output voltage step, high power quality, fewer switching losses, minimum harmonics, and better electromagnetic compatibility. Capacitor voltage balancing is difficult when the voltage level increases in the case of diode-clamped MLI, hence these are restricted to three levels. Even though most of the industries are used three-level NPC Inverter. Flying Capacitor MLI requires more dc capacitors for higher voltage levels. However, there is flexibility to set the switching combinations and feasible for DC capacitor voltage balance [14]. Due to its modularity characteristic, CHB MLI topology becomes more reliable and popular. However, each bridge needs an isolated DC source and for higher levels, the requirement for switches also increases [15]. Hybrid topologies, most of which are developed from conventional topologies, have been proposed by researchers as a cost-effective means of addressing power quality issues and achieving high grid code standards [8]. Analysis and comparison of the 49-level modular asymmetrical 49-level inverter were proposed in [16].

The authors in [17] Presented a new DVR topology based on a buck-boost ac/ac converter. It contains an inductor, capacitor, and five switches, and the most prominent characteristic of the topology is the lack of an injection transformer, which allows for a direct connection to the grid without the use of storage devices. As a result, this topology has less physical volume, mass, and cost than traditional topologies. A DVR with a cascaded H-Bridge multilevel converter [15] was connected directly to the MV network without the use of an injection transformer. The voltage restoration is achieved by the capacitors as energy storage using the zero active power compensation technique.

DVR with five-level reduced power components TCHB inverter [18] was used to mitigate the voltage sag using two voltage compensation schemes. In [19] proposed an S4L inverter-based DVR with a single DC power source and reduced switch count, thus it is cost-effective, furthermore, it generates seven levels, which significantly supports in reduction of the system harmonic problem. Interline DVR with CHB multilevel inverter was proposed in [20] to mitigate the voltage sag with better THD. An adjustable dc-link connected MLI-based DVR [21] is suitable for compensation of both long and short period sag. DVR with an open-end winding transformer having reduced inverter loss and lower

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and
content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

harmonics was proposed in [22]. Cascaded OEW transformer-based DVR was reported in [23] with better voltage levels, and reduced THD even though it does not require extra clamping diodes. T- type MLI-based DVR was proposed for medium and high-power applications [24]. A new asymmetrical multilevel inverter that combines an E-type clamped X-type DVR with a reliable fractional-order super-twisting sliding mode control was proposed. In [25] for a definite voltage level, these topologies require a high number of switches thus, the required driver circuits, size, and cost are increased. It was suggested in [26] to use an "odd-nary" cascading asymmetric multi-level inverter, which produces staircase output at higher levels while using fewer switches. To compensate for any voltage disturbances, a novel HCMLI coupled to a photovoltaic power source is proposed as an AC-voltage synthesizer for DVR [27]. A selective harmonic feedback control strategy was proposed in [28] and is implemented in MV DVR to provide voltage harmonic compensation without affecting sag compensation. H infinity voltage controller-based DVR proposed in [29] is effectively compensated the voltage sags in MV applications.

In this work, asymmetrical 23-level MLI is proposed to overcome all the limitations. The recommended 23-level MLI is implemented in a PV-fed DVR using a rotating dq reference frame controller. From the comparative analysis, the recommended 23-level MLI requires less component count factor and is cost-effective. The proposed PV-fed MLI-DVR efficiently minimizes the voltage sags, and swells and improves the power quality. The following are the most crucial features of the proposed topology:

- The recommended 23-level MLI uses only three DC sources and twelve switches among them seven are unidirectional switches and five bidirectional switches.
- Most switches have reduced voltage stress, allowing them to operate at medium voltages.
- The proposed PV-fed MLI-DVR efficiently minimizes the voltage sags, and swells and improves the power quality.
- The proposed PV-fed MLI-DVR harmonic profile is superior to traditional VSIDVR, and under the IEEE standard.

The remainder of the article is prepared accordingly. Section 2 describes the proposed solar PV integrated MLI-DVR. Section 3 describes the functioning and control of a PV-fed MLI-DVR. The proposed solar PV-fed MLI-DVR results were reported in Section 4 and the conclusions were made in Section 5.

II. Solar PV Fed MLI - DVR Configuration

The system is configured using a 3-phase, 3-wire DVR, solar PV, a boost converter, and a load as shown in Figure. 1. DVR is the primary part, made up of a voltage source MLI, a DC link capacitor, an LC filter, and a coupling transformer. The solar PV system is the second part, which includes a PV array, an MPPT controller, and a boost converter.

The equivalent circuit of DVR is obtained by connecting a voltage source (V_{Comp}) in between source (V_S) and load (V_L) with their respective impedances, Z_S and Z_L, as shown in Figure 2. At the PCC source, current I_S is divided into I_L and I_{OT}. Where I_L is sensitive load current and I_{OT} is another load current. The voltage at PCC is represented by V_G and the voltage compensated by DVR is V_{DVR}. Resistance R and inductance L are obtained from the impedance Z of the filter and injection transformer, the values of R_{DVR} and X_{DVR} are related to V_{DVR}. The impedance of the source, load, and DVR are Z_S, Z_L, and Z_{DVR} respectively.

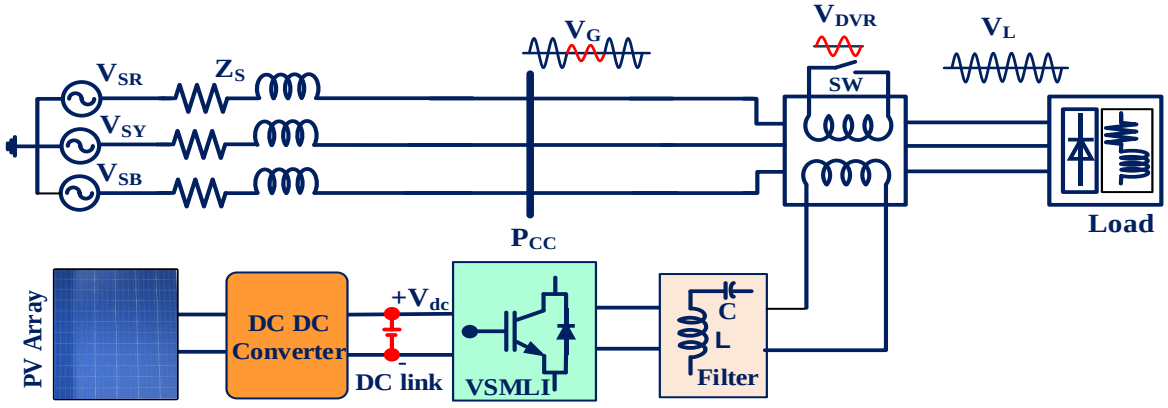


Figure 1. PV fed MLI-DVR configuration

P_S is real power and Q_S is reactive power of supply. P_L is real power and Q_L is the reactive power of the load. P_{DVR} is real power and Q_{DVR} is reactive power supplied by the DVR.

The voltage across sensitive load V_L is given by

$$V_L(t) = V_G(t) + V_{DVR}(t) + Ri_L(t) + L\frac{di_L}{dt} \quad (1)$$

For higher power applications, voltage source inverters with two-level are not suitable because the switches will block large voltage, more dv/dt creates electromagnetic interference, and hence recently MLIs are used in DVR configuration. The article proposed a 23-level multilevel inverter supplied by a solar PV array.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

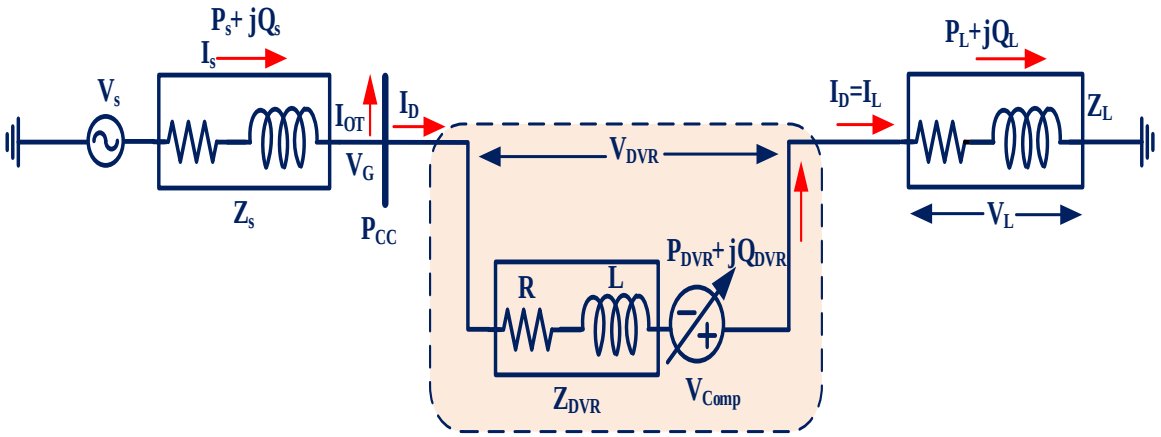


Figure 2. Equivalent model of DVR

A. *Proposed 23-level Inverter*

The proposed configuration comprises three dc sources namely V_a, V_b, and V_c, and seven unidirectional switches and five bidirectional switches. Four bidirectional switches are connected in a crisscross structure [30] as depicted in Figure 3.

For asymmetric operation, the magnitudes of DC voltage sources are fixed as

$$V_a = 1V_{dc};\ V_b = 3V_{dc};\ V_c = 7V_{dc} \tag{2}$$

The required DC sources N_{DC} in terms of levels N_{Lev} is given by:

$$N_{DC}^{Asym} = \frac{(N_{Lev}-5)}{6} \tag{3}$$

The number of switches N_{SW} required in terms of levels N_{Lev} is given by:

$$N_{SW}^{Asym} = \frac{(N_{Lev}+1)}{2} \tag{4}$$

The suggested topology uses unidirectional power switches for all of the switches. As a result, the required gate driver circuits N_{GDK} equals the number of N_{SW}, and is written as:

$$N_{GDK}^{Asym} = N_{SW}^{Asym} = \frac{(N_{Lev}+1)}{2} \tag{5}$$

$V_{L,\,max}$ is the maximum voltage output and is given by:

$$V_{L,max}^{Asym} = \frac{(N_{Lev}-1)}{2} \tag{6}$$

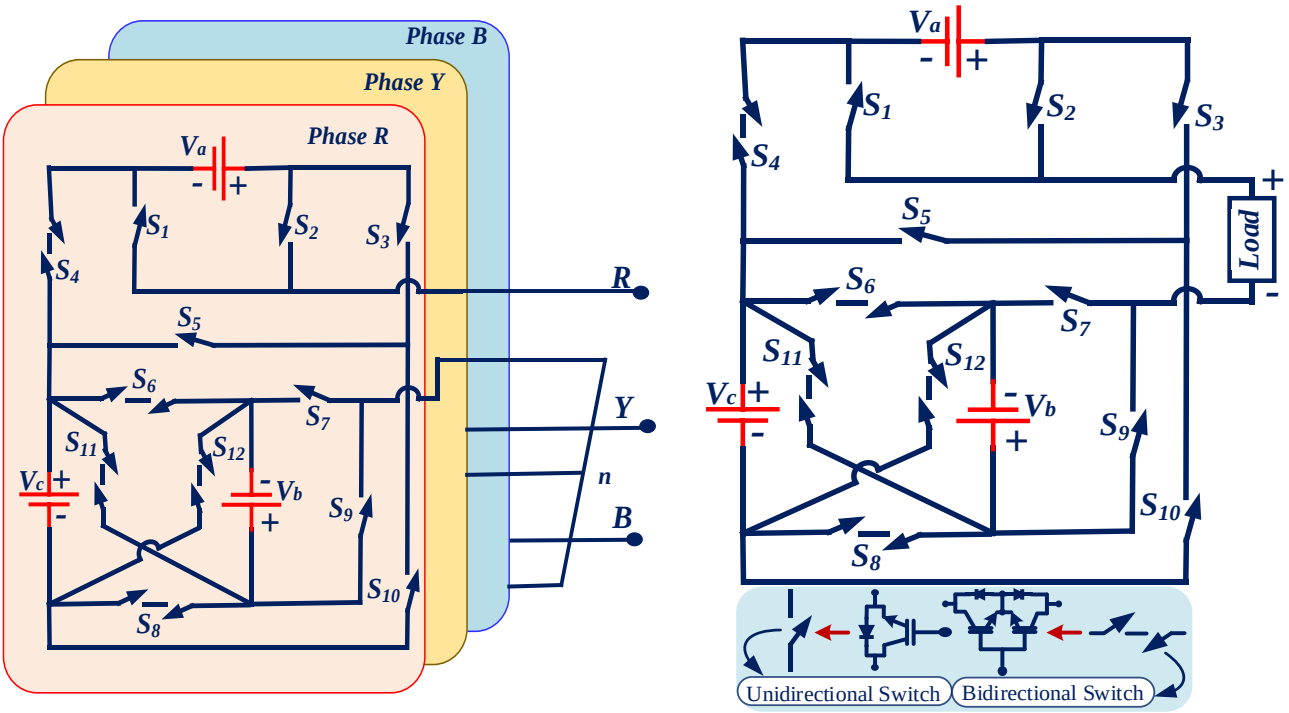


Figure 3. Twenty-three-level MLI topology (a) Three-phase (b) single-phase configuration

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

The proposed configuration produces an output voltage of 23 levels with magnitudes of zero, positive (+V_{dc} to +11 V_{dc}), and negative (-V_{dc} to -11V_{dc}). TABLE I shows the 23-level MLI switching states in both positive and negative levels.

Total maximum blocking voltage is one of the most important qualitative characteristics, which is referred to as the algebraic sum of the maximum voltage stress on each switch. MBV of particular switches are calculated as follows:

$$MBV_{S1} = MBV_{S2} = MBV_{S3} = V_a = 1V_{dc}$$

$$MBV_{S7} = MBV_{S9} = V_b = 3V_{dc}$$

$$MBV_{S5} = MBV_{S10} = V_c = 7V_{dc}$$

$$MBV_{S4} = \frac{1}{2}(V_c + V_a) = 4V_{dc.}$$

$$MBV_{S6} = MBV_{S11} = MBV_{S8} = MBV_{S12} = \frac{1}{2}(V_c + V_b) = 5V_{dc.}$$

TABLE I
SWITCHING CONDITIONS OF THE PROPOSED THE MLI

Positive levels												Output Voltage (Volts)	Negative levels											
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
0	1	0	1	0	0	1	1	0	0	0	0	11V_{dc}	1	0	1	0	0	1	0	0	1	1	0	0
1	0	0	1	0	0	1	1	0	0	0	0	10V_{dc}	0	1	1	0	0	1	0	0	1	1	0	0
1	0	1	0	1	0	1	1	0	0	0	0	9V_{dc}	1	0	1	0	1	0	1	1	0	0	0	0
0	1	0	1	0	0	0	1	1	0	0	0	8V_{dc}	1	0	1	0	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	1	1	0	0	0	7V_{dc}	0	1	1	0	0	1	1	0	0	1	0	0
1	0	1	0	1	0	0	1	1	0	0	0	6V_{dc}	1	0	1	0	1	0	0	1	1	0	0	0
0	1	0	1	0	0	0	0	1	0	0	1	5V_{dc}	1	0	1	0	0	0	1	0	0	1	1	0
0	1	0	1	0	0	1	0	0	0	1	0	4V_{dc}	1	0	1	0	1	1	0	0	1	0	0	0
1	0	0	1	0	0	1	0	0	0	1	0	3V_{dc}	1	0	0	1	0	1	0	0	1	0	0	0
1	0	1	0	1	0	1	0	0	0	1	0	2V_{dc}	0	1	0	1	0	1	0	0	1	0	0	0
0	1	0	1	0	1	1	0	0	0	0	0	1V_{dc}	1	0	1	0	0	0	0	1	1	1	0	0
1	0	0	1	0	1	1	0	0	0	0	0	0V_{dc}	1	0	0	1	0	1	1	0	0	0	0	0

TABLE II
SWITCHING CONDITIONS OF THE PROPOSED THE MLI

Levels	Current conducting path	Active sources	Stress on switches	Maximum Stress across switches		Output Voltage (Volts)
L_1	V_c-S_4-V_a-S_2-L-S_7-V_b-S_8-V_c	V_c+V_a+V_b	S_1, S_6, S_9, S_{11}, S_{12}	S_6 = S_{11}= S_{12}	5V_{dc}	+11V_{dc}
L_2	V_c-S_4-S_1-L-S_7-V_b-S_8-V_c	V_c+V_b	S_6, S_9, S_{11}, S_{12}	S_6 = S_{11}= S_{12}	5V_{dc}	+10V_{dc}
L_3	V_c-S_5-S_3-V_a-S_1-L-S_7-V_b-S_8-V_c	V_c+V_b-V_a	S_2, S_4, S_6, S_9, S_{10}, S_{11}, S_{12}	S_{10}	7V_{dc}	+9V_{dc}
L_4	V_c-S_4-V_a-S_2-L-S_9-S_8-V_c	V_c+V_a	S_1, S_{11}	S_{11}	5V_{dc}	+8V_{dc}
L_5	V_c-S_4-S_1-L-S_9-S_8-V_c	V_c	S_{11}	S_{11}	5V_{dc}	+7V_{dc}
L_6	V_c-S_5-S_3-V_a-S_1-L-S_9-S_8-V_c	V_c-V_a	S_2, S_4,S_{10}, S_{11}, S_{12}	S_{11} = S_{12}	5V_{dc}	+6V_{dc}
L_7	V_c-S_4-V_a-S_2-L-S_9-V_b-S_{12}-V_c	V_c-V_b+V_a	S_1,S_6, S_7, S_8,S_{11}	S_6 = S_8= S_{11}	5V_{dc}	+5V_{dc}
L_8	V_b-S_{11}-S_4-V_a-S_2-L-S_7-V_b	V_b+V_a	S_1,S_6, S_9	S_9	3V_{dc}	+4V_{dc}
L_9	V_b-S_{11}-S_4-S_1-L-S_7-V_b	V_b	S_6, S_9	S_6 = S_9	3V_{dc}	+3V_{dc}
L_{10}	V_b-S_{11}-S_5-S_3-V_a-S_1-L-S_7-V_b	V_b-V_a	S_2, S_4, S_6, S_9	S_9	3V_{dc}	+2V_{dc}
L_{11}	V_a-S_2-L-S_7-S_6-S_4-V_a	V_a	S_1	S_1	1V_{dc}	+1V_{dc}
L_{12}	L-S_7-S_6-S_4-S_1-L	-	-	-	0	0V_{dc}
L_{13}	V_a-S_3-S_{10}-S_8-S_9-L-S_1-V_a	-(V_a)	S_2	S_2	1V_{dc}	-1V_{dc}
L_{14}	V_b-S_9-L-S_2-V_a-S_4-S_6-V_b	-(V_b-V_a)	S_1, S_7	S_7	3V_{dc}	-2V_{dc}
L_{15}	V_b-S_9-L-S_1-S_4-S_6-V_b	-(V_b)	S_7	S_7	3V_{dc}	-3V_{dc}
L_{16}	V_b-S_9-L-S_1-V_a-S_3-S_5-S_6-V_b	-(V_b+V_a)	S_2, S_4, S_7	S_4	4V_{dc}	-4V_{dc}
L_{17}	V_c-S_{11}-V_b-S_7-L-S_1-V_a-S_3-S_{10}-V_c	-(V_c-V_b+V_a)	S_2, S_4, S_5, S_6, S_8, S_9, S_{12}	S_5	7V_{dc}	-5V_{dc}
L_{18}	V_a-S_3-S_5-V_c-S_8-S_9-L-S_1-V_a	-(V_c-V_a)	S_2, S_4, S_{10}	S_{10}	7V_{dc}	-6V_{dc}
L_{19}	V_c-S_6-S_7-L-S_2-S_3-S_{10}-V_c	-(V_c)	S_5, S_{12}	S_5	7V_{dc}	-7V_{dc}
L_{20}	V_c-S_6-S_7-L-S_1-V_a-S_3-S_{10}-V_c	-(V_c+V_a)	S_2, S_4, S_5,S_{12}	S_5	7V_{dc}	-8V_{dc}
L_{21}	V_a-S_3-S_5-V_c-S_8-V_b-S_7-L-S_1-V_a	-(V_c-V_a+V_b)	S_2, S_4, S_6,S_9, S_{10}, S_{11}, S_{12}	S_{10}	7V_{dc}	-9V_{dc}
L_{22}	V_c-S_6-V_b-S_9-L-S_2-S_3-S_{10}-V_c	-(V_c+V_b)	S_5, S_7, S_8,S_{11}, S_{12}	S_5	7V_{dc}	-10V_{dc}
L_{23}	V_c-S_6-V_b-S_9-L-S_1-V_a-S_3-S_{10}-V_c	-(V_c+V_b+V_a)	S_2, S_4, S_5, S_7, S_8, S_{11}, S_{12}	S_5	7V_{dc}	-11V_{dc}

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

The term TSV is stated as the algebraic sum of MBV across individual switches and is expressed in equation 7, equation 8 provides the TSV_{PU}.

$$TSV = MBV_{S1} + MBV_{S2} + MBV_{S3} + - - - + MBV_{Sn} \quad (7)$$

$$TSV_{PU} = \frac{TSV}{V_{L,max}} \quad (8)$$

For the proposed topology TSV^{Prop} is calculated as

$$TSV^{Prop} = 4[5V_{dc}] + 2[3V_{dc}] + 2[7V_{dc}] + 3[V_{dc}] + 4V_{dc}$$

$$TSV^{Prop} = 47V_{dc} \quad (9)$$

And $$TSV_{PU}^{Prop} = \frac{47V_{dc}}{11V_{dc}} = 4.27 \quad (10)$$

As a consequence, the recommended MLI topology optimizes the utilization of DC sources with minimum TSV and switches, hence the volume and price will be reduced.

TABLE II shows the current path to the load, as well as the maximum blocking voltage (MBV) and the voltage stress on the switches. It has been found that some operating voltage levels include redundant switches.

A comparison is made between the recommended topology and other recent topologies to evaluate the benefits and capabilities of the recommended 23-level MLI topology. Table III shows a comparison of the required driver circuits, DC sources, switches, component count factor (CCF), the maximum number of conducting devices per level, TSV_{PU}, and the cost factor [31] for each level.

TABLE III
COMPARISONS OF THE PROPOSED 23-LEVEL MLI WITH RECENT TOPOLOGIES

Topologies	*Quantitative analysis*						*Qualitative analysis*				
Ref	N_{lev}	N_{DC}	N_{SW}	N_{GDK}	*MCD*	N_{Var}	*CCF*	*%THD*	TSV_{PU}	CF/N_{Lev}	
										$\alpha = 0.5$	$\alpha = 1.5$
[32]	23	6	12	12	6	0	1.30	2.59	5.81	1.43	1.68
[33]	23	5	10	10	4	2	1.17	-	6.09	1.39	1.65
[34]	23	5	14	14	7	0	1.43	5.47	-	-	-
[35]	23	5	12	9	3	5	1.34	4.17	-	-	-
[36]	23	5	12	12	4	0	1.26	3.6	4.4	1.35	1.54
[37]	23	3	12	12	5	0	1.17	-	5.27	1.28	1.52
Proposed	23	3	12	12	7	0	1.17	3.23	4.27	1.27	1.45

B. Analysis of Boost Converters for Solar PV.

The current and voltage of the PV array are, controlled by temperature, irradiance, and the number of parallel and series strings hence, it is essential to pick the correct PV panel. Trina Solar TSM-200 DC/DA01A panel with 3 parallel and 2 series modules per string is selected. An ideal equivalent model of solar PV is shown in Figure 4. D is the diode and R_P, R_S are the resistances of parallel n_p and series n_s connected cells, respectively.

From an ideal PV circuit, the diode current is

$$i_d = I_0\left(e^{\frac{V_D}{\gamma V_T}} - 1\right) \quad (11)$$

Where γ is the ideality constant, saturation current is I_o and thermal voltage $V_T = (\frac{kT_c}{q})$ is depends on the charge of electron q, cell temperature T_c, and Boltzmann's constant k.

Output power $$P_{PV} = V_{PV} * I_{PV} \quad (12)$$

Output current is

$$I_{PV} = I_S - I_d - I_p = I_S - I_0\left(e^{\frac{V_D}{\gamma V_T}} - 1\right) - I_p \quad (13)$$

$$I_{PV} = n_p I_S - n_p I_0\left(e^{\left(\frac{1}{\gamma V_T}\right)\left(\frac{V_{PV}}{n_s} + \frac{R_S I_{PV}}{n_p}\right)} - 1\right) - \frac{n_p}{R_p}\left(\frac{V_{PV}}{n_s} + \frac{R_S I_{PV}}{n_p}\right) \quad (14)$$

Short circuit current I_S

$$I_{s(T)} = I_{s(TR)}[\beta(T - T_R) + 1] \quad (15)$$

The values of coefficient of temperature **β**, reference temperature T_R, and corresponding short circuit current $I_{S(TR)}$ are provided in PV datasheets.

Considering the intensity of irradiance then

$$I_{s(G)} = I_{s(Gn)}\frac{G}{G_n} \quad (16)$$

G_n is the normal value of irradiation

Saturation current I_0 is calculated at $I_{PV} = 0$, then I_0 at T_R is given by

$$I_O = \frac{I_S}{\left(e^{\frac{V_D}{\gamma V_T}} - 1\right)} \quad (17)$$

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

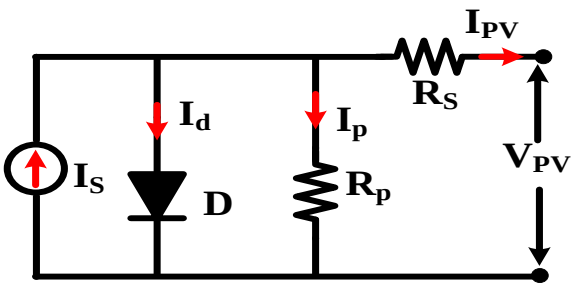


Figure 4. Equivalent model of Solar PV

The fundamental problem of employing renewable energy sources to generate electricity is low voltage output. To enhance the voltage level, the RES output is sent to a DC-DC boost converter.

The boost converter output voltage is regulated by the duty cycle of the control switch. Hence, by adjusting the switch-ON time, one can alter the output voltage. The formula used to calculate the average output voltage over the duty cycle 'α' is

$$V_{dc} = V_{PV}\left(\frac{1}{1-\alpha}\right) \quad (18)$$

The value of inductor and capacitors are calculated using

$$L = \frac{V_{PV}\alpha}{(f_s * \Delta I_L)} \quad (19)$$

$$C = \frac{I_0\alpha}{(f_s * \Delta V_{dc})} \quad (20)$$

The input current and output voltage ripple factors are ΔI_L and ΔV_{dc}, respectively, and the switching frequency is f_s. For a realistic estimation of inductor and capacitor values, ΔI_L should be restricted to 30%, and ΔV_{dc} is commonly assumed at 5%. TABLE IV lists the features of the solar PV boost converter.

TABLE IV
SPECIFICATIONS OF PV BOOST CONVERTER

200W PV Module		Boost converter.	
P_{PV}	200W	L	1.28 mH
I_{PV}	5.32A	C	1.31μF
V_{PV}	37.6V	$V_{in} = V_{PV}$	112.8V
I_{sc}	5.60A	α	0.718
V_{oc}	46.0V	V_{dc}	400 V

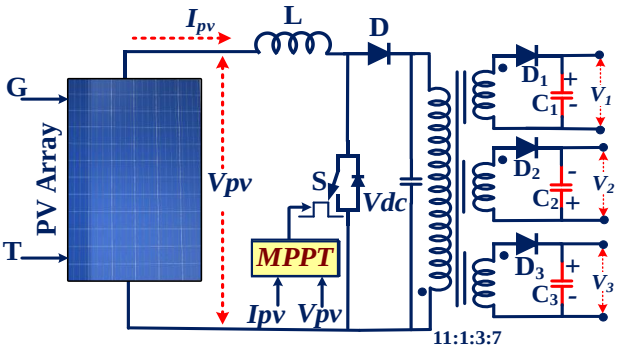


Figure 5. SIMO isolated DC-DC converter

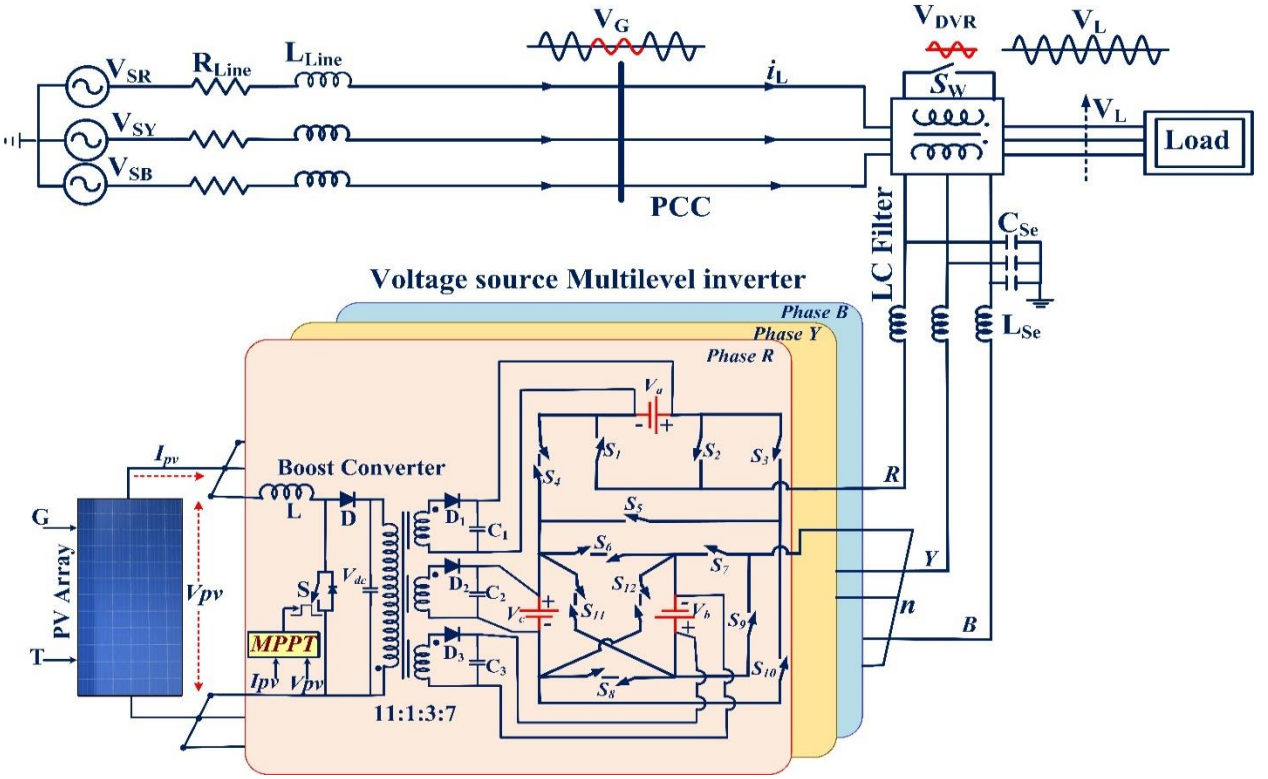


Figure 6. Proposed solar PV-fed MLI-DVR configuration

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and
content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

Figure 5 shows a single-input multi-output (SIMO) circuit that receives the output of the DC-DC boost converter [38]. Boost converter output is fed into the primary winding of a transformer and secondary of multi winding transformer gives three output ports with turn's ratio of 11:1:3:7. At the output terminal of each DC-DC converter output port, a diode and a capacitor are connected. The diode is positioned to prevent the capacitor's reverse current from flowing into the transformer windings. The operation of the boost converter is regulated by the MPPT controller depending on inputs such as environmental parameters (solar radiation and temperature), PV array parameters (V_{oc} and I_{sc}), and outputs like DC link voltage. The operational performance of traditional incremental and conductance MPPT algorithms is lower if the operating point is fluctuating around the MPP and under rapidly changing irradiance conditions. To address these issues, an enhanced INC MPPT is employed [39]. The circuit diagram of the PV-fed MLI-DVR connected to the grid is shown in Figure 6.

III. Operation and Control of PV-fed MLI-DVR

Depending on the type of load and voltage sag, the DVR compensating technique differs. This is because only a few loads respond to fluctuations in voltage magnitude, while others are sensitive to deviations in phase angle, and still, others are sensitive to both. As a result, the load characteristics dictate which control approach to employ. The pre-sag compensation (PSC) method is used to compensate for both the magnitude and phase angle of the voltage sag [40].

In this strategy load voltage is maintained with the pre-sag voltage, therefore no voltage disturbance is sensed by the load because the load voltage is having the same magnitude and phase angle, hence it is also known as the voltage quality optimized technique. The vector representation of PSC is shown in Figure. 7. During sag, the DVR is controlled by adding more real power, which affects the rating of direct energy storage or energy received from the grid hence the requirement of energy source to supply active power will increase apart from reactive power injected by the inverter. It is acceptable for both balanced and unbalanced sensitive loads heaving phase jump or not.

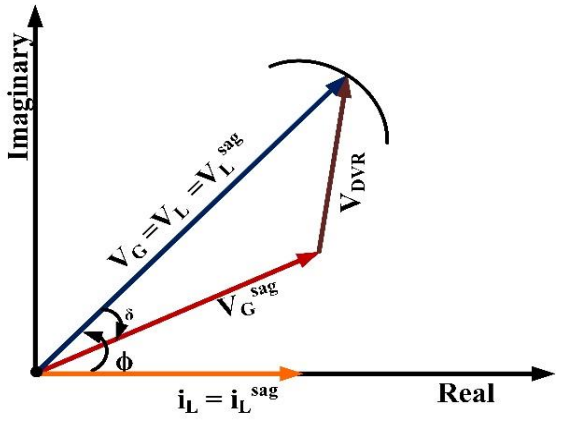


Figure 7. Pre sag voltage injection technique for DVR

Equation 21 gives the magnitude of V_{DVR} and the phase angle of V_{DVR} is obtained from equation 22.

$$V_{DVR,p} = \sqrt{2}\sqrt{(V_L)^2 + (V_G^{Sag})^2 - (2V_L V_{G,p}^{Sag}\cos(\delta_p))} \quad (21)$$

$$\angle V_{DVR,p} = \tan^{-1}\left(\frac{V_L \sin\phi - V_{G,p}^{Sag}\sin(\phi-\delta_p)}{V_L\cos\phi - V_{G,p}^{Sag}\cos(\phi-\delta_p)}\right) \quad (22)$$

Where V_{DVR} is the DVR injected voltage, ϕ is the phase angle between V_L and I_L, V_G^{Sag} is the grid voltage at sag, δ is the corresponding angle of phase jump to V_G^{Sag}, p is the corresponding phase of the supply voltage (R, Y, or B).

A. Control scheme of the DVR

A voltage disturbance duration (both start and end), phase jump, and depth depend on the type of voltage disturbance. Various methods for sensing voltage disturbances are presented in [41]. The Park transformation is utilized to transform the three-phase load voltages $V_{L\,RYB}$ and reference voltages $V_{ref,\,RYB}$ into vectorized dq0 voltage components $V_{L,dq0}$, and $V_{ref,dq0}$. The following formula is used to compute the three-phase reference voltage:

$$\begin{bmatrix} V_{R\,ref} \\ V_{Y\,ref} \\ V_{B\,ref} \end{bmatrix} = V_{L\,max}\begin{bmatrix} sin\omega t \\ sin(\omega t - 120^0) \\ sin(\omega t + 120^0) \end{bmatrix} \quad (23)$$

Then, using the Park transformation, it is changed from RYB to dq0 components

$$\begin{bmatrix} V_d \\ V_q \\ V_O \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos(\omega t) & cos(\omega t - 120^0) & cos(\omega t + 120^0) \\ -sin(\omega t) & -sin(\omega t - 120^0) & -sin(\omega t + 120^0) \\ 0.5 & 0.5 & 0.5 \end{bmatrix} \times \begin{bmatrix} V_R \\ V_Y \\ V_B \end{bmatrix} \quad (24)$$

Once the load and reference voltages change into the dq0 frame, the error signal e_r will be obtained in terms of magnitude and phase shift of voltage, as shown in figure 8b.

$$|e_{r\,dq0}| = \sqrt{(V_{dref} - V_{di})^2 + (V_{qref} - V_{qi})^2 + (V_{0ref} - V_{0i})^2} \quad (25)$$

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

The change in the dq0 components will result from variations in magnitude and phase shift of voltage. Changes in the state of the supply are detected and responded to swiftly by the suggested control. In this work, the synchronous reference frame the phase-locked loop (PLL) is used as a synchronization method. It maintains frequency and phase synchronization between the controller output signal and a reference input signal.

The DVR control presented in this article is a PI controller driven by an error signal, resulting in a low level of complexity. The controller function is to reduce the error signal on the distribution grid as much as possible. In the time domain, the contribution signal of the PWM in dq0 frame for the PI controller is Vp, given as

$$V_{P\,dq0} = K_P e_{r\,dq0} + K_i \int_0^1 e_{r\,dq0} dt \tag{26}$$

Finally, the output of PI control is fed back into abc frame to regulate the PWM that generates the VSI gating pulses, given as

$$\begin{bmatrix} V_R \\ V_Y \\ V_B \end{bmatrix} = \begin{bmatrix} sin(\omega t) & cos(\omega t) & 1 \\ sin(\omega t - 120^0) & cos(\omega t - 120^0) & 1 \\ sin(\omega t + 120^0) & cos(\omega t + 120^0) & 1 \end{bmatrix} \times \begin{bmatrix} V_{d\,P} \\ V_{q\,P} \\ V_{0\,P} \end{bmatrix} \tag{27}$$

According to Equation (25), the error signals e_r of dq voltages are given to the PI controller, as

$$e_{rd}(t) = V_{dref} - V_d \tag{28}$$

$$e_{rq}(t) = V_{qref} - V_q \tag{39}$$

The error e_{rd} signal is fed into the D-axis of the PI controller, whereas the error e_{rq} is fed into the Q-axis of the PI controller, as shown in Figure 8. The signal provided to the controller is the change in voltage between V_{ref} and V_d. The error equation is given as

$$e_r = V_{ref} - V_d \tag{30}$$

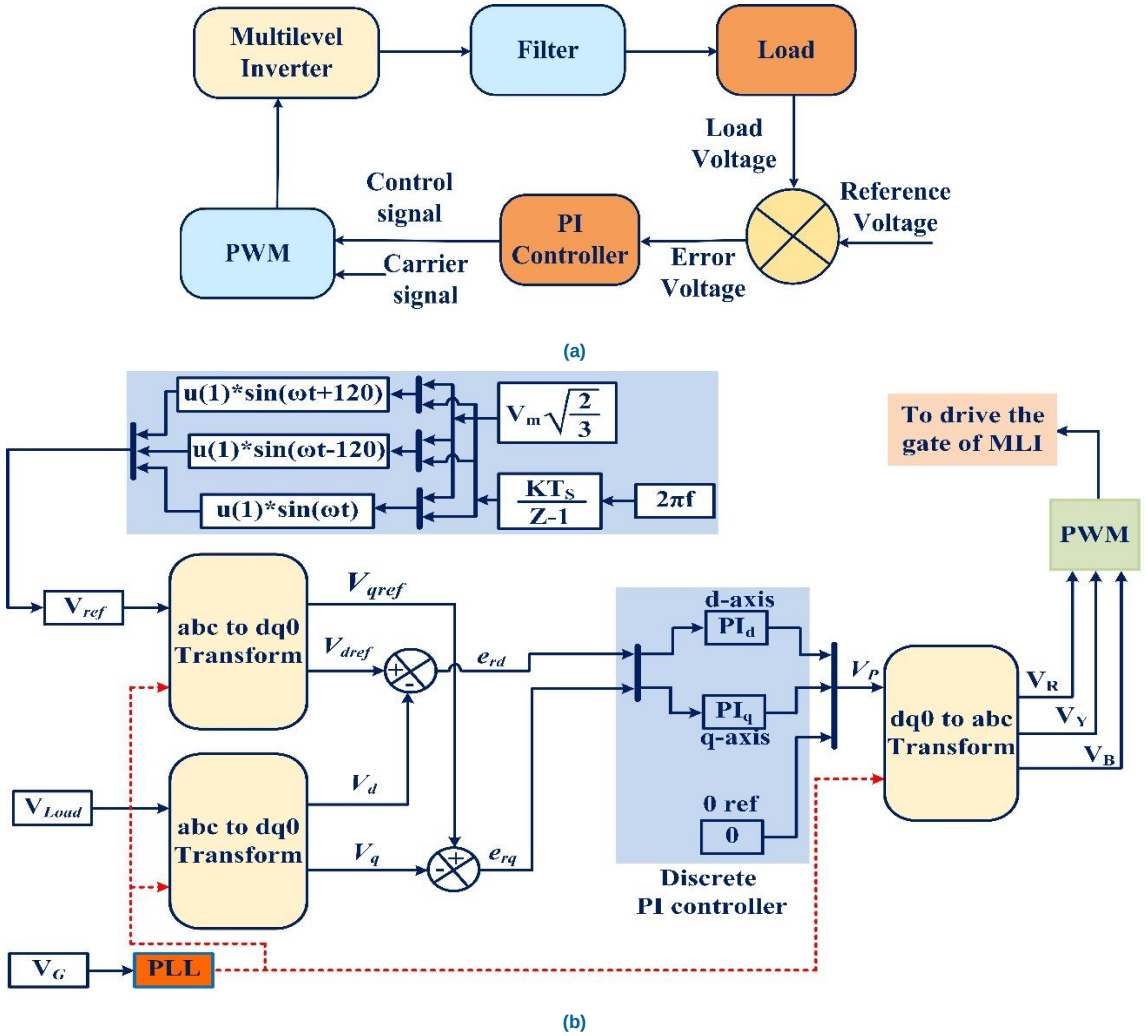


Figure 8. DVR PI controller

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and
content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

Figure 8 represents the control strategy of the proposed MLI-based DVR. A rotating dq reference frame controller is used to generate the reference signal shown in Figure 8b. The error signal and error rate drives the PI controller, it analyzes the input and produces controller output. The controller output is given as a reference voltage to the PWM. The pulses generated by the PWM pulse generator control the operation of the multilevel inverter. The systematic procedure of the control system is presented in Figure 8a. The magnitude and phase angle of the reference voltage is produced by using the pre-sag compensation technique and injected through the multilevel inverter. This information is computed by using the synchronous reference frame Phase-Locked Loops (PLL). The parameters of PI controller are obtained as K_{pd} = 7.401, K_{id} = 189.014 in case of D-axis, K_{pq} = 69.31, K_{iq} = 192.412 in case of Q-axis.

B. Pulse width modulation

The nearest level control (NLC) or round method [20] is a low switching frequency control technique used to generate the nearest voltage level by converting it to the desired reference output voltage. Using the switching table, the closest level of voltage to the reference voltage is chosen by selecting the switching combination that corresponds to that level as depicted in Figure 9. The nearest output voltage level for voltage reference V_{ref} and the modulation index 'm' is

$$V_{ref} = m\left(\frac{N-1}{2}\right)Vsin(\omega t) = V_m \sin(\omega t) \quad (31)$$

$$m = \frac{V_m}{\left(\frac{N-1}{2}\right)V} \quad (32)$$

$$V_L = V\ round\ \left(\frac{V_{ref}}{V}\right) \quad (33)$$

The limits of the reference voltage and active switches of the selected voltage level of the NLC technique are represented in Table V. The switching angles are calculated from equation (34) and tabulated in Table VI

$$\theta = sin^{-1}\left(\frac{x-0.5}{\frac{N-1}{2}}\right) \quad (34)$$

TABLE V

LIMITS OF THE REFERENCE VOLTAGE AND ACTIVE SWITCHES OF THE SELECTED VOLTAGE LEVEL OF PV BOOST CONVERTER

Positive levels			Negative levels		
Limits of the reference voltage	Level selected	Active switches	Limits of the reference voltage	Level selected	Active switches
$0 \le V_{ref} < 0.5$	$0V_{dc}$	$S_2, S_3, S_6, S_8, S_9, S_{11}$	$-0.5 \le V_{ref} < 0$	$0V_{dc}$	$S_1, S_4, S_5, S_7, S_{10}, S_{12}$
$0.5 \le V_{ref} < 1.5$	$1V_{dc}$	$S_2, S_4, S_5, S_7, S_9, S_{11}$	$-1.5 \le V_{ref} < -0.5$	$-1V_{dc}$	$S_1, S_3, S_6, S_8, S_{10}, S_{12}$
$1.5 \le V_{ref} < 2.5$	$2V_{dc}$	$S_1, S_3, S_6, S_7, S_9, S_{11}$	$-2.5 \le V_{ref} < -1.5$	$-2V_{dc}$	$S_2, S_4, S_5, S_8, S_{10}, S_{12}$
$2.5 \le V_{ref} < 3.5$	$3V_{dc}$	$S_2, S_3, S_6, S_7, S_9, S_{11}$	$-3.5 \le V_{ref} < -2.5$	$-3V_{dc}$	$S_1, S_4, S_5, S_8, S_{10}, S_{12}$
$3.5 \le V_{ref} < 4.5$	$4V_{dc}$	$S_2, S_4, S_6, S_7, S_9, S_{11}$	$-4.5 \le V_{ref} < -3.5$	$-4V_{dc}$	$S_1, S_3, S_5, S_8, S_{10}, S_{12}$
$4.5 \le V_{ref} < 5.5$	$5V_{dc}$	$S_2, S_4, S_5, S_8, S_9, S_{12}$	$-5.5 \le V_{ref} < -4.5$	$-5V_{dc}$	$S_1, S_3, S_6, S_7, S_{10}, S_{11}$
$5.5 \le V_{ref} < 6.5$	$6V_{dc}$	$S_1, S_3, S_6, S_8, S_9, S_{12}$	$-6.5 \le V_{ref} < -5.5$	$-6V_{dc}$	$S_2, S_4, S_5, S_7, S_{10}, S_{11}$
$6.5 \le V_{ref} < 7.5$	$7V_{dc}$	$S_2, S_3, S_5, S_7, S_9, S_{12}$	$-7.5 \le V_{ref} < -6.5$	$-7V_{dc}$	$S_1, S_4, S_6, S_8, S_{10}, S_{11}$
$7.5 \le V_{ref} < 8.5$	$8V_{dc}$	$S_2, S_4, S_5, S_7, S_9, S_{12}$	$-8.5 \le V_{ref} < -7.5$	$-8V_{dc}$	$S_1, S_3, S_6, S_8, S_{10}, S_{11}$
$8.5 \le V_{ref} < 9.5$	$9V_{dc}$	$S_1, S_3, S_6, S_7, S_9, S_{12}$	$-9.5 \le V_{ref} < -8.5$	$-9V_{dc}$	$S_2, S_4, S_5, S_8, S_{10}, S_{11}$
$9.5 \le V_{ref} < 10.5$	$10V_{dc}$	$S_2, S_3, S_6, S_7, S_9, S_{12}$	$-10.5 \le V_{ref} < -9.5$	$-10V_{dc}$	$S_1, S_4, S_5, S_8, S_{10}, S_{11}$
$10.5 \le V_{ref}$	$11V_{dc}$	$S_2, S_4, S_6, S_7, S_9, S_{12}$	$V_{ref} < -10.5$	$-11V_{dc}$	$S_1, S_3, S_5, S_8, S_{10}, S_{11}$

TABLE VI

SWITCHING ANGLES AND THE CORRESPONDING VOLTAGE LEVELS

Positive Interval	Voltage	Negative Interval
$0^0 \le \boldsymbol{\theta} < 2.6^0$, $177.4^0 \le \boldsymbol{\theta} < 180^0$	$0V_{dc}$	$180^0 \le \boldsymbol{\theta} < 182.6^0$, $357.4^0 \le \boldsymbol{\theta} < 360^0$
$2.6^0 \le \boldsymbol{\theta} < 7.83^0$, $172.2^0 \le \boldsymbol{\theta} < 177.4^0$	$1V_{dc}$	$182.6^0 \le \boldsymbol{\theta} < 187.83^0$, $352.17^0 \le \boldsymbol{\theta} < 357.4^0$
$7.83^0 \le \boldsymbol{\theta} < 13.13^0$, $166.87^0 \le \boldsymbol{\theta} < 172.2^0$	$2V_{dc}$	$187.83^0 \le \boldsymbol{\theta} < 193.13^0$, $346.87^0 \le \boldsymbol{\theta} < 352.17^0$
$13.13^0 \le \boldsymbol{\theta} < 18.55^0$, $161.45^0 \le \boldsymbol{\theta} < 166.87^0$	$3V_{dc}$	$193.13^0 \le \boldsymbol{\theta} < 198.55^0$, $341.45^0 \le \boldsymbol{\theta} < 346.87^0$
$18.55^0 \le \boldsymbol{\theta} < 24.14^0$, $155.86^0 \le \boldsymbol{\theta} < 161.45^0$	$4V_{dc}$	$198.55^0 \le \boldsymbol{\theta} < 204.14^0$, $335.86^0 \le \boldsymbol{\theta} < 341.45^0$
$24.14^0 \le \boldsymbol{\theta} < 30^0$, $150^0 \le \boldsymbol{\theta} < 155.86^0$	$5V_{dc}$	$204.14^0 \le \boldsymbol{\theta} < 210^0$, $330^0 \le \boldsymbol{\theta} < 335.86^0$
$30^0 \le \boldsymbol{\theta} < 36.22^0$, $143.78^0 \le \boldsymbol{\theta} < 150^0$	$6V_{dc}$	$210^0 \le \boldsymbol{\theta} < 216.22^0$, $323.78^0 \le \boldsymbol{\theta} < 330^0$
$36.22^0 \le \boldsymbol{\theta} < 42.98^0$, $137^0 \le \boldsymbol{\theta} < 143.78^0$	$7V_{dc}$	$216.22^0 \le \boldsymbol{\theta} < 223^0$, $317^0 \le \boldsymbol{\theta} < 323.78^0$
$42.98^0 \le \boldsymbol{\theta} < 50.6^0$, $129.4^0 \le \boldsymbol{\theta} < 137^0$	$8V_{dc}$	$223^0 \le \boldsymbol{\theta} < 230.6^0$, $309.4^0 \le \boldsymbol{\theta} < 317^0$
$50.6^0 \le \boldsymbol{\theta} < 59.72^0$, $120.8^0 \le \boldsymbol{\theta} < 129.4^0$	$9V_{dc}$	$230.6^0 \le \boldsymbol{\theta} < 239.72^0$, $300.28^0 \le \boldsymbol{\theta} < 309.4^0$
$59.72^0 \le \boldsymbol{\theta} < 72.65^0$, $107.35^0 \le \boldsymbol{\theta} < 120.8^0$	$10V_{dc}$	$239.72^0 \le \boldsymbol{\theta} < 252.65^0$, $287.65^0 \le \boldsymbol{\theta} < 300.28^0$
$72.65^0 \le \boldsymbol{\theta} < 107.35^0$	$11V_{dc}$	$252.65^0 \le \boldsymbol{\theta} < 287.65^0$

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

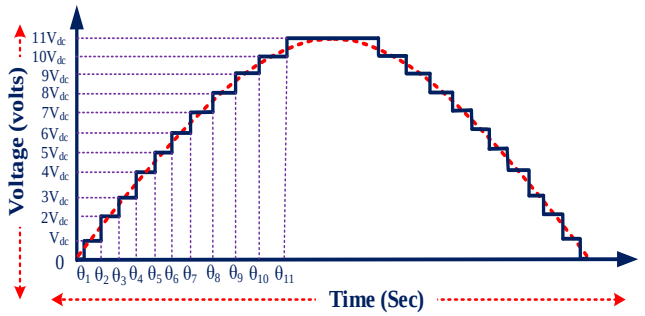


Figure 9. Nearest level control technique waveform of 23 levels

IV. RESULTS AND DISCUSSION

A. Simulation results

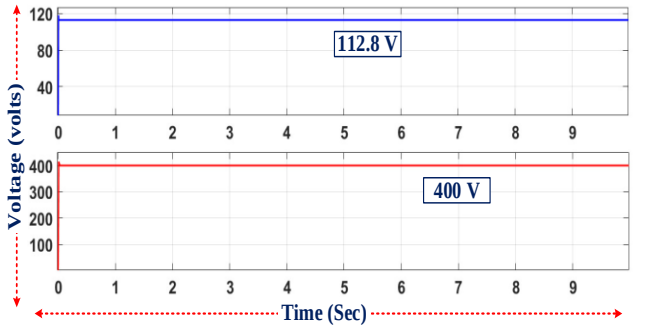
The proposed multilevel inverter solar PV fed DVR is evaluated in terms of improving voltage profile. The results are shown using the MATLAB/Simulink platform. Table VII lists the parameters of DVR.

TABLE VII
DVR PARAMETERS AND RATINGS.

Source (AC grid)	400V, 50 Hz
DC-link voltage	400V
Filter	L=5 mH, C=80 µF, R=1.5Ω
Switching frequency	5kHz
Transformer ratio	1:1

The simulation results of PV and boost converter with EINC MPPT are shown in Figure. 10. PV at MPP generates 112.8 volts and by using a boost converter it is boosted to 400 volts which are appeared at the DC link. Figure 11 represents the R phase voltage waveform of an asymmetrical 23-level MLI. Voltage sag mode is created by applying overload at time intervals ranging from 0.2 sec to 0.285 sec.

Figure 10. Simulation results of PV and boost converter



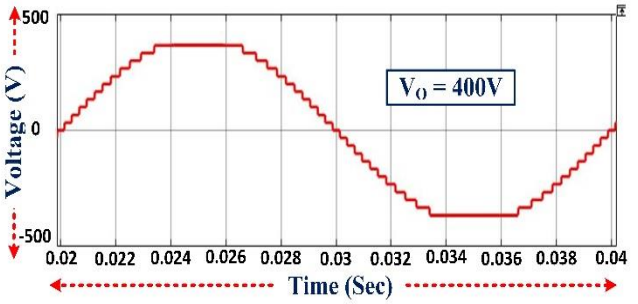


Figure 11. Simulation phase voltage of proposed 23-level MLI topology

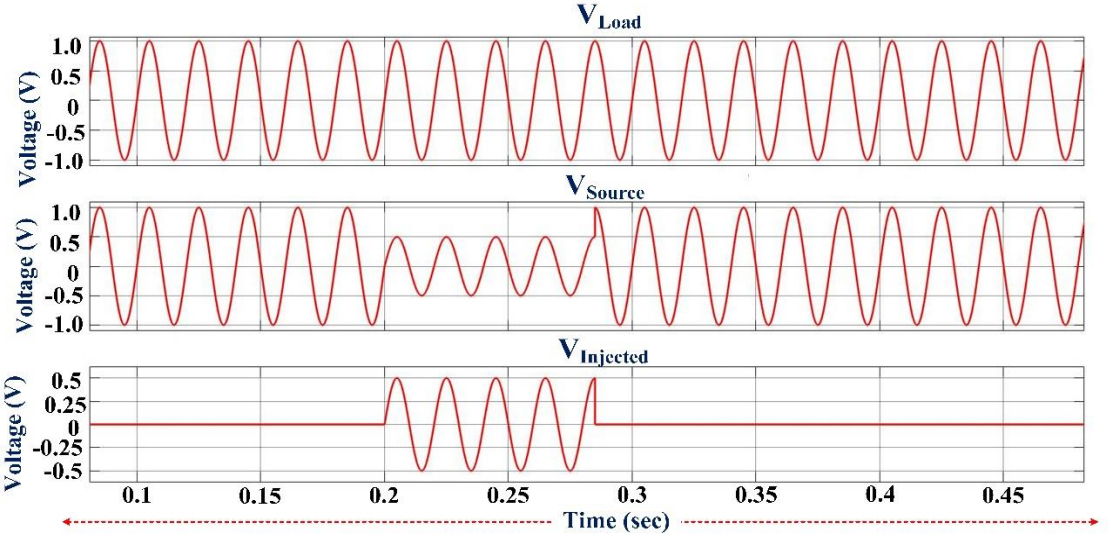


Figure 12. Simulation results of Source, Injected, and Load voltages at sag condition.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and
content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

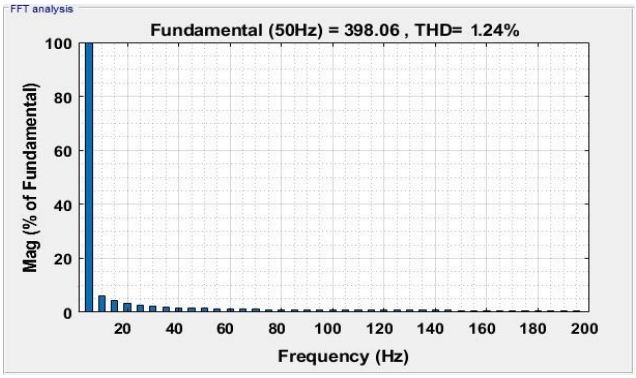


Figure 13. THD at V_{Load} with DVR during sag mode

In this test, 0.5pu of sag is applied in comparison to load point reference voltage. The proposed DVR injects the appropriate voltage and maintains the load voltage profile, and is shown in Figure 12 and Figure 14. Figure 12 represents the voltage profile of DVR at 0.5pu of sag condition only in one phase, whereas Figure 14 shows a three-phase voltage profile of DVR. Figure 13 depicts the voltage THD at the load side with DVR in sag mode. A double voltage sag mode is created by applying overload at time intervals ranging from 0.2 sec to 0.285 sec with 0.7pu and from 0.315 sec to 0.385 sec with 0.5pu of sag is applied in comparison to load point reference voltage. The proposed DVR injects the appropriate voltages and maintains the load voltage profile, as shown in Figure 15. In this test, a swell mode is created at time intervals from 0.3 sec to 0.365 sec. 1.2 pu of swell is applied in comparison to load point reference voltage. The proposed DVR compensates for the appropriate voltage and maintains the load voltage profile, and is shown in Figure 16.

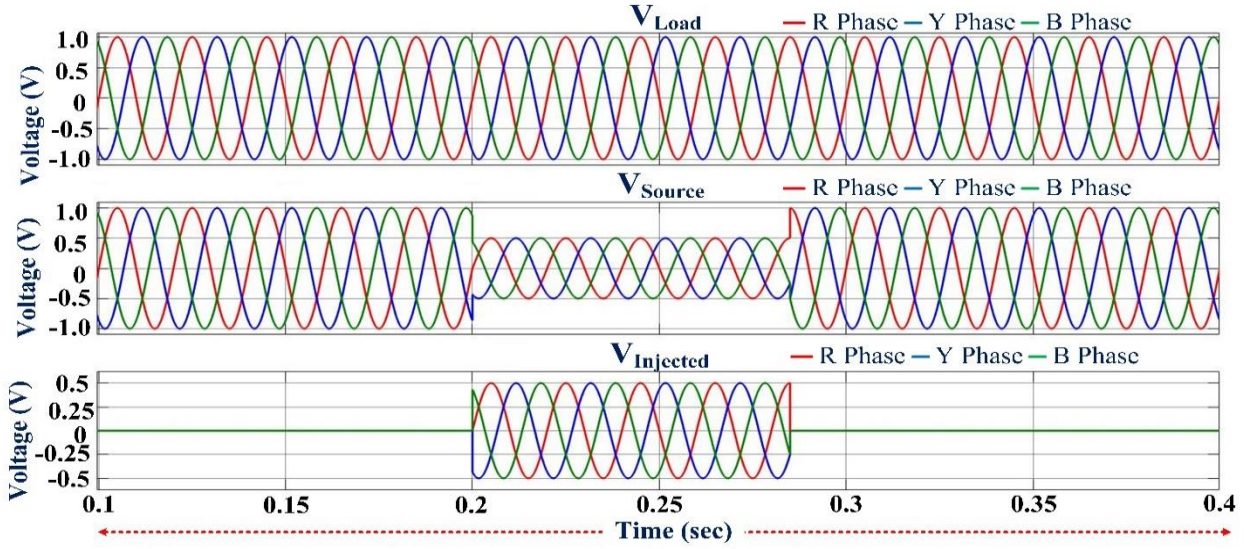


Figure 14. Simulation results of Source, Injected, and Load voltages at 0.5pu of sag condition.

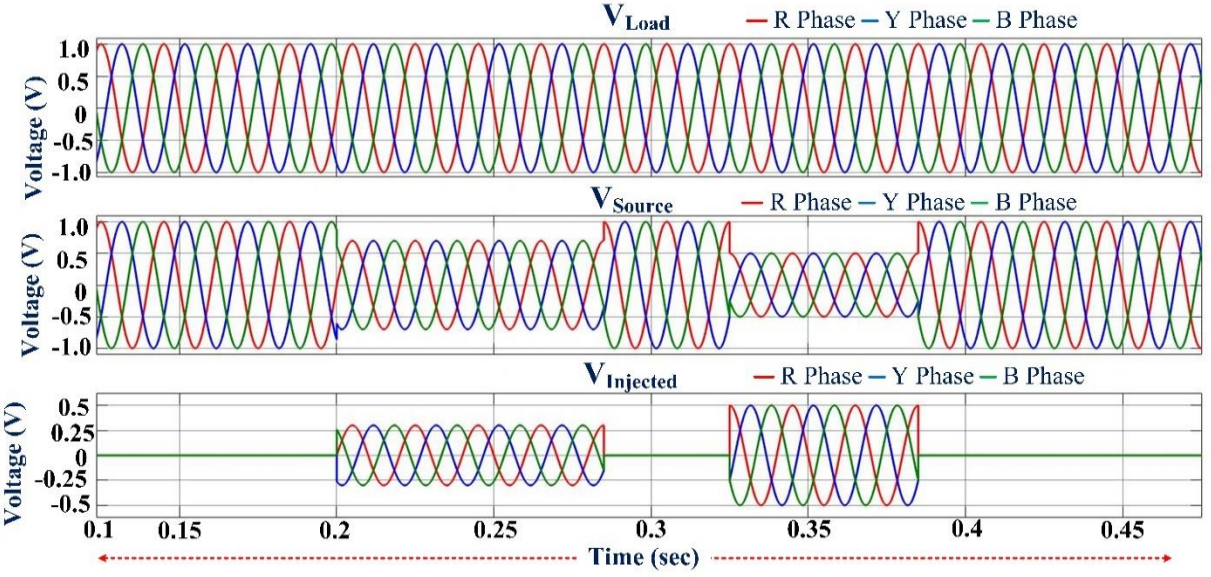


Figure 15. Simulation results of Source, Injected, and Load voltages at 0.7pu and 0.5pu sag mode

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and
content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

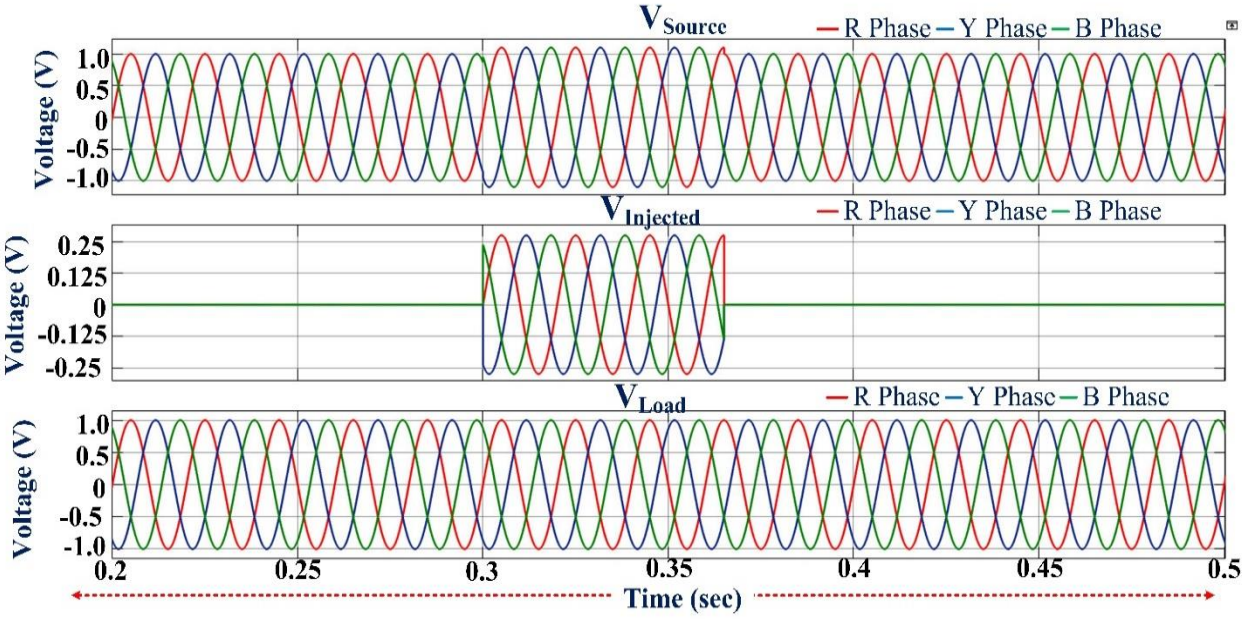


Figure 16. Simulation results of Source, Injected, and Load voltages at 1.2pu swell mode

B. Experimental Results

The suggested topology of 23-level MLI is tested using a single-phase prototype built in the lab. A dual dc supply supplies the input dc sources and a 100-ohm resistive load is used. The prototype consists of 12 IGBT switches that are activated by using optocouplers (MCT2E). The real-time controller dSPACE1104 is used to build the switching control system, and DSO is used to monitor the voltage and current waveforms. The experimental setup is shown in Figure 17 and the findings with a resistive load are shown in Figure 18, at steady-state output voltages of 400V (282.84 V_{rms}) and the load current of 4A (2.82 I_{rms}).

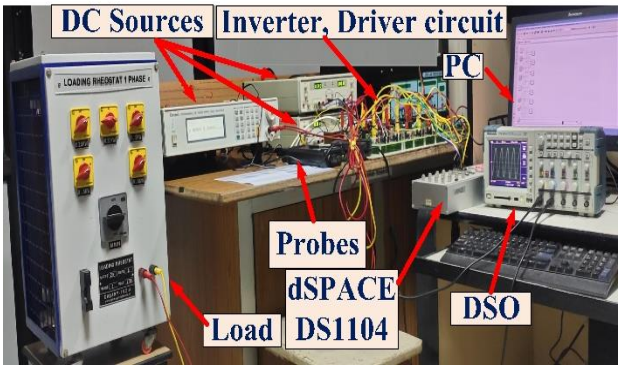


Figure 17. Experimental set-up of 23-level MLI

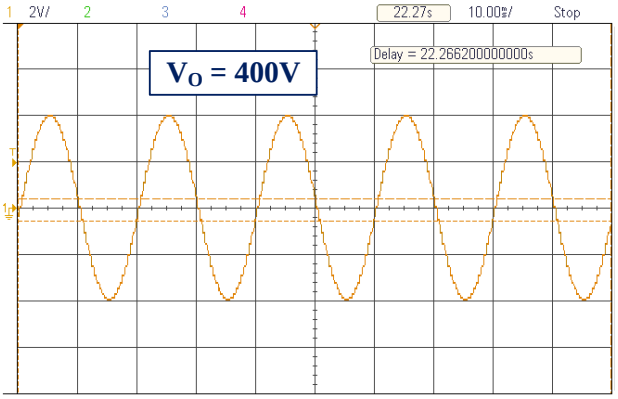


Figure 18. Experimental output voltage of 23-level MLI

C. Real-time Analysis

For high-power applications, it is not feasible to test experimentally the simulation results achieved with MATLAB/Simulink. To verify their accuracy hardware in-loop testing (HIL) was developed. This platform scales down testing time, cost and also provides test features in any situation and enables test system change. The setup of the HIL simulator is shown in Figure 19. It consists of an Opal-RT OP5600 simulator, as well as a host computer and a digital storage oscilloscope. It is entirely digital, supported by an FPGA processor, a real-time simulator that runs Simulink in real-time using a fixed-step solver. For viewing and editing the block diagram graphical model in the frontend, it uses MATLAB/Simulink, from which real-time simulation code is generated, updated, and downloaded.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and
content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

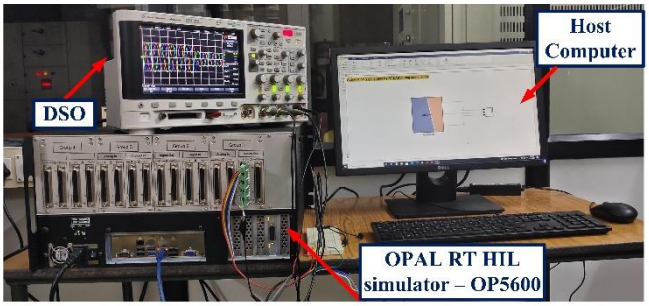


Figure 19. HIL simulator set-up

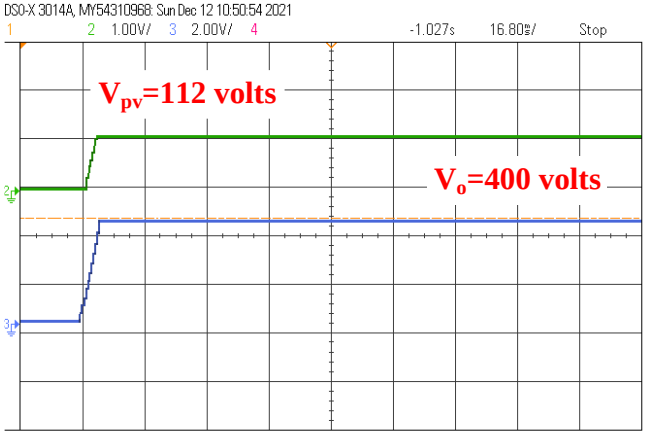


Figure 20. PV and boost converter output in real-time

Figure 20 illustrates the performance of an EINC MPPT controlled boost converter using OPAL-RT and Figure 21 shows the output of PV fed MLI-DVR at 0.5pu sag condition of one phase, which includes source voltage, compensation voltage, and load voltage information.

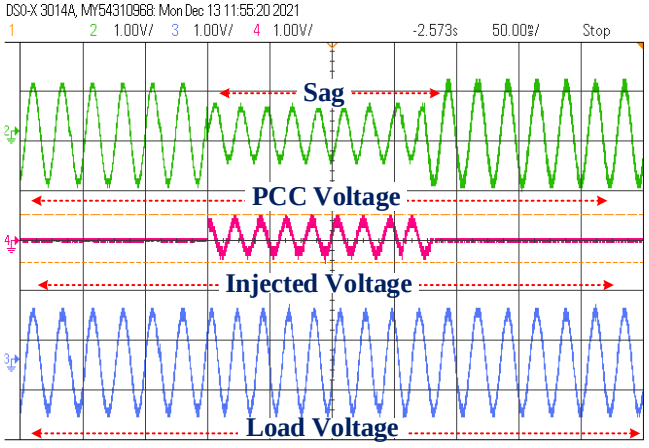
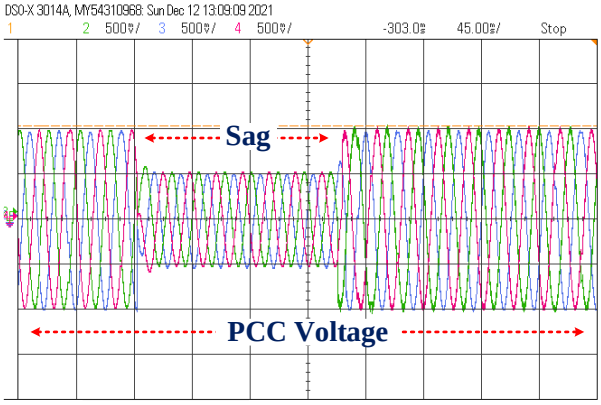


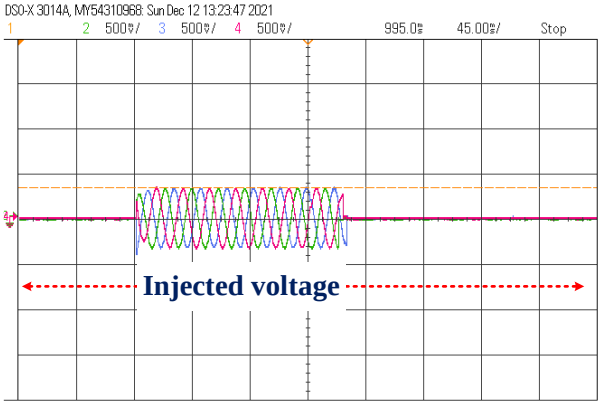
Figure 21. HIL single-phase Voltage profiles at sag condition.

Figure 22 shows the output voltage profile of PV fed MLI-DVR at 0.5pu sag condition, which includes source voltage, compensation voltage, and load voltage information. Figure 23 shows the real-time output details of the proposed DVR source voltage, compensated voltage, and load voltages at 0.7pu and 0.25pu sag conditions.

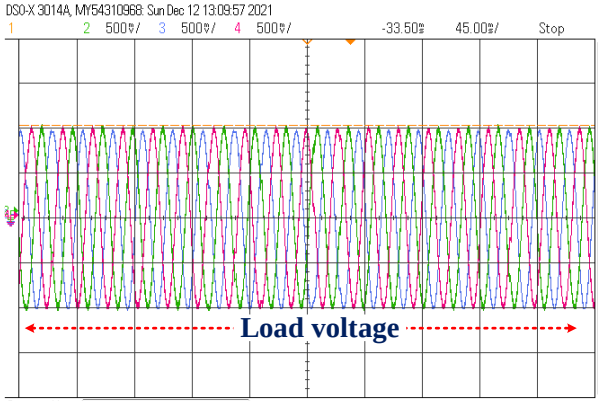
The THD of the proposed PV-fed DVR is reduced from 17.09 percent (without DVR) to 1.28 percent (with MLI-DVR) at sag condition and is represented in Figure 24. The proposed DVR architectures are compared with existing MLI DVR architectures in terms of switches required, output voltage levels and THD and are tabulated in Table VIII



(a)



(b)



(c)

Figure 22. HIL three-phase output of (a) Source, (b) Injected, and (c) Load voltages at 0.5pu sag condition.

Figure 25 represents the comparison of the required number of switches per phase to produce expected levels in the output voltage waveform from this the proposed MLI-DVR topology produces higher voltage levels with reduced switches hence the sag voltage is effectively compensated by implementing this topology with lesser THD.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

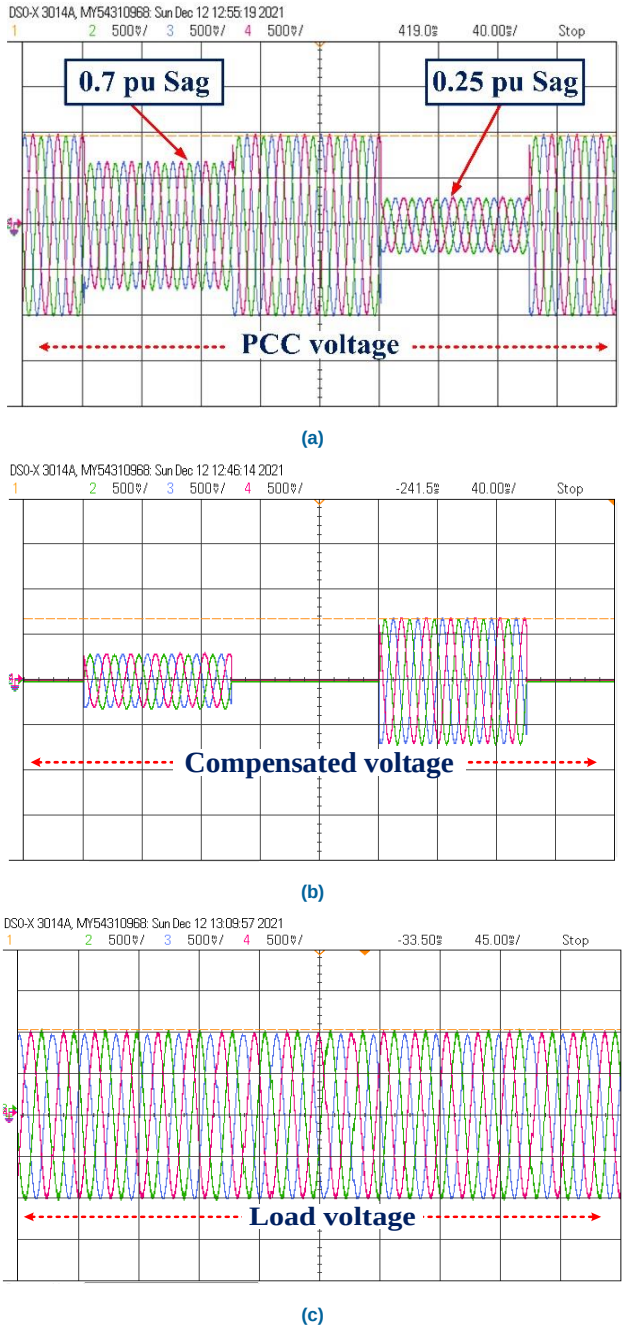


Figure 23. HIL three-phase output of (a) Source, (b) Injected, and (c) Load voltages at 0.7pu and 0.5pu sag conditions.

Figure 24. Real-time load THD at sag condition

TABLE VIII
COMPARISON OF PROPOSED MLI-DVR WITH OTHER TOPOLOGIES

Ref.	Inverter Topology	Switches /Phase	No of Levels	THD
[41]	Diode Clamped	24	5	-
[24]	T-Type MLI	8	5	2.77
[18]	TCHB MLI	5	5	4.78
[20]	CHB MLI	8	7	-
[42]	CHB MLI	12	7	-
[19]	Simplified Four Level Inverter	8	7	1.23
[43]	CHB MLI	12	7	1.73
[44]	CHB MLI	16	9	-
[21]	CHB MLI	16	9	2.8
[45]	CHB MLI	20	11	-
[15]	CHB MLI	24	13	-
[46]	CHB MLI	32	17	-
Proposed	RCMLI	12	23	1.28

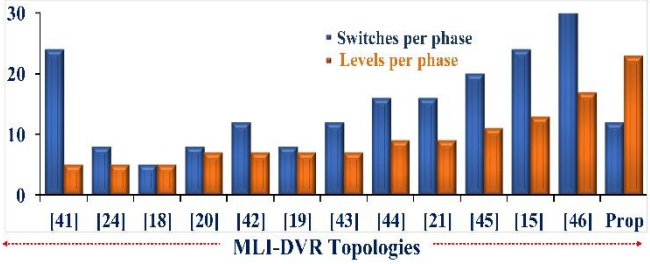


Figure 25. Comparison of proposed MLI-DVR with other topologies

VII. CONCLUSION

A PV-fed MLI-DVR using a rotating dq reference frame controller with an asymmetrical 23-level MLI is proposed in this article. A novel multilevel inverter is designed and implemented experimentally with a laboratory prototype. A synthesized output voltage of the proposed MLI is obtained with a low THD utilizing fewer circuit components. There exits various outstanding features of the proposed MLI such as the TSV_{PU} is 2.4 whereas the cost function (CF/L) values for 'α' are 1.07 and 1.15 respectively, therefore the proposed MLI is cost-effective and superior than the existing topologies. The results of the proposed PV-fed MLI-DVR are verified with the OPAL-RT real time simulator testing platform. The proposed system efficiently minimizes the voltage sag and preserves the DC link voltage to be stable. The maximum power can be extracted from the PV modules using INC MPPT technique. A detailed comparison of the proposed MLI-DVR is presented with the existing topologies and it is found that the proposed system performs efficiently during the compensation of voltage sag. A lower THD of 1.28 % is obtained in the process of compensation of voltage at the grid and satisfies the IEEE standards. The proposed system is significantly performs well henceforth it can be further implemented in HVDC and FACTS devices.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and
content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

ACKNOWLEDGMENT

The authors are grateful to the Vellore Institute of Technology in Vellore, India, for granting a SEED grant to fund this research.

REFERENCE

[1] M. K. Saini and R. Kapoor, "Classification of power quality events - A review," Int. J. Electr. Power Energy Syst., vol. 43, no. 1, pp. 11–19, 2012, doi: 10.1016/j.ijepes.2012.04.045.

[2] J. Gong, D. Li, T. Wang, W. Pan, and X. Ding, "A comprehensive review of improving power quality using active power filters," Electr. Power Syst. Res., vol. 199, no. June, 2021, doi: 10.1016/j.epsr.2021.107389.

[3] R. Sepehrzad, A. Mahmoodi, S. Y. Ghalebi, A. R. Moridi, and A. R. Seifi, "Intelligent hierarchical energy and power management to control the voltage and frequency of micro-grids based on power uncertainties and communication latency," Electr. Power Syst. Res., vol. 202, no. August 2021, 2022, doi: 10.1016/j.epsr.2021.107567.

[4] F. Kleber de Araújo Lima, J. M. Guerrero, F. L. Tofoli, C. G. C. Branco, and J. L. Dantas, "Fast and accurate voltage sag detection algorithm," Int. J. Electr. Power Energy Syst., vol. 135, no. August 2021, 2022, doi: 10.1016/j.ijepes.2021.107516.

[5] Dhanamjayulu, C., and S. Meikandasivam. "Fuzzy controller based design of 125 level asymmetric cascaded multilevel inverter for power quality improvement." *Analog Integrated Circuits and Signal Processing* 101, no. 3 (2019): 533-542.

[6] M. Bajaj, "Design and Simulation of Hybrid DG System Fed Single-Phase Dynamic Voltage Restorer for Smart Grid Application," Smart Sci., vol. 8, no. 1, pp. 24–38, 2020, doi: 10.1080/23080477.2020.1748928.

[7] A. B. Kanase-Patil, A. P. Kaldate, S. D. Lokhande, H. Panchal, M. Suresh, and V. Priya, "A review of artificial intelligence-based optimization techniques for the sizing of integrated renewable energy systems in smart cities," Environ. Technol. Rev., vol. 9, no. 1, pp. 111–136, 2020, doi: 10.1080/21622515.2020.1836035.

[8] P. Kala and S. Arora, "A comprehensive study of classical and hybrid multilevel inverter topologies for renewable energy applications," Renew. Sustain. Energy Rev., vol. 76, no. February, pp. 905–931, 2017, doi: 10.1016/j.rser.2017.02.008.

[9] S. M. Silva, S. É. da Silveira, A. de Souza Reis, and B. J. Cardoso Filho, "Analysis of a dynamic voltage compensator with reduced switch-count and absence of energy storage system," IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1255–1262, 2005, doi: 10.1109/TIA.2005.853382.

[10] M. Fang, A. I. Gardiner, A. MacDougall, and G. A. Mathieson, "A novel series dynamic voltage restorer for distribution systems," POWERCON 1998 - 1998 Int. Conf. Power Syst. Technol. Proc., vol. 1, pp. 38–42, 1998, doi: 10.1109/ICPST.1998.728702.

[11] M. R. Banaei and A. R. Dehghanzadeh, "DVR based cascaded multilevel Z-source inverter," PECon2010 - 2010 IEEE Int. Conf. Power Energy, pp. 51–56, 2010, doi: 10.1109/PECON.2010.5697556.

[12] S. Jothibasu and M. K. Mishra, "An improved direct AC-AC converter for voltage sag mitigation," IEEE Trans. Ind. Electron., vol. 62, no. 1, pp. 21–29, 2015, doi: 10.1109/TIE.2014.2334668.

[13] M. Balamurugan, T. S. Sivakumaran, and M. Aishwariya, "Voltage sag/swell compensation using Z-source inverter DVR based on FUZZY controller," 2013 IEEE Int. Conf. Emerg. Trends Comput. Commun. Nanotechnology, ICE-CCN 2013, no. ICECCN, pp. 648–653, 2013, doi: 10.1109/ICE-CCN.2013.6528580.

[14] Salary, Ebrahim, Mohamad Reza Banaei, and Ali Ajami. "Analysis of Hybrid Multilevel Inverters Using a Reduced Voltage Stress Switch." *Cankaya University Journal of Science and Engineering* 13, no. 2 (2016).

[15] S. Galeshi and H. Iman-Eini, "Dynamic voltage restorer employing multilevel cascaded H-bridge inverter," IET Power Electron., vol. 9, no. 11, pp. 2196–2204, 2016, doi: 10.1049/iet-pel.2015.0335.

[16] Salari, Ebrahim, and Ali Darvish Falehi. "A novel 49-level asymmetrical modular multilevel inverter: analysis, comparison and validation." Analog Integrated Circuits and Signal Processing 101, no. 3 (2019): 611-622.

[17] B. H. Kwon, G. Y. Jeong, S. H. Han, and D. H. Lee, "Novel line conditioner with voltage up/down capability," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1110–1119, 2002, doi: 10.1109/TIE.2002.803236.

[18] R. J. Satputaley and V. B. Borghate, "Performance analysis of DVR using 'new reduced component' multilevel inverter," Int. Trans. Electr. Energy Syst., vol. 27, no. 4, pp. 1–11, 2017, doi: 10.1002/etep.2288.

[19] J. Ye, H. B. Gooi, X. Zhang, B. Wang, and J. Pou, "Simplified four-level inverter-based dynamic voltage restorer with single DC power source," IEEE Access, vol. 7, pp. 137461–137471, 2019, doi: 10.1109/ACCESS.2019.2941999.

[20] M. Shahabadini and H. Iman-Eini, "Improving the Performance of a Cascaded H-Bridge-Based Interline Dynamic Voltage Restorer," IEEE Trans. Power Deliv., vol. 31, no. 3, pp. 1160–1167, 2016, doi: 10.1109/TPWRD.2015.2480967.

[21] E. Babaei, M. F. Kangarlu, and M. Sabahi, "Dynamic voltage restorer based on multilevel inverter with adjustable dc-link voltage," IET Power Electronics, vol. 7, no. 3. pp. 576–590, 2014, doi: 10.1049/iet-pel.2013.0179.

[22] G. A. De Almeida Carlos, E. C. Dos Santos, C. B. Jacobina, and J. P. R. A. Mello, "Dynamic Voltage Restorer Based on Three-Phase Inverters Cascaded Through an Open-End Winding Transformer," IEEE Trans. Power Electron., vol. 31, no. 1, pp. 188–199, 2016, doi: 10.1109/TPEL.2015.2404798.

[23] G. A. De Almeida Carlos, C. B. Jacobina, J. P. R. A. Méllo, and E. C. Dos Santos, "Cascaded Open-End Winding Transformer Based DVR," IEEE Trans. Ind. Appl., vol. 54, no. 2, pp. 1490–1501, 2018, doi: 10.1109/TIA.2017.2768531.

[24] K. Rajkumar, P. Parthiban, and N. Lokesh, "Real-time implementation of transformerless dynamic voltage restorer based on T-type multilevel inverter with reduced switch count," International Transactions on Electrical Energy

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and
content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

Systems, vol. 30, no. 4. 2020, doi: 10.1002/2050-7038.12301.

[25] Falehi, Ali Darvish, and Hossein Torkaman. "Promoted supercapacitor control scheme based on robust fractional-order super-twisting sliding mode control for dynamic voltage restorer to enhance FRT and PQ capabilities of DFIG-based wind turbine." Journal of Energy Storage 42 (2021): 102983.

[26] Darvish Falehi, Ali. "Half-cascaded multilevel inverter coupled to photovoltaic power source for AC-voltage synthesizer of dynamic voltage restorer to enhance voltage quality." International Journal of Numerical Modelling: Electronic Networks, Devices and Fields 34, no. 5 (2021): e2883.

[27] Falehi, A. D., and M. Rafiee. "Enhancement of DFIG-wind turbine's LVRT capability using novel DVR based odd-nary cascaded asymmetric multi-level inverter." Engineering science and technology, an international journal 20, no. 3 (2017): 805-824.

[28] Newman, Michael John, Donald Grahame Holmes, John Godsk Nielsen, and Frede Blaabjerg. "A dynamic voltage restorer (DVR) with selective harmonic compensation at medium voltage level." In 38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003., vol. 2, pp. 1228-1235. IEEE, 2003.

[29] Li, Yun Wei, D. Mahinda Vilathgamuwa, Frede Blaabjerg, and Poh Chiang Loh. "A robust control scheme for medium-voltage-level DVR implementation." IEEE Transactions on Industrial Electronics 54, no. 4 (2007): 2249-2261.

[30] Toupchi Khosroshahi, Mahdi. "Crisscross cascade multilevel inverter with reduction in number of components." IET Power Electronics 7, no. 12 (2014): 2914-2924.

[31] Devalraju, Prasad, and C. Dhanamjayulu. "A Novel 19-level Asymmetrical Multilevel Inverter for Dynamic Voltage Restorer Applications." In 2021 Innovations in Power and Advanced Computing Technologies (i-PACT), pp. 1-7. IEEE, 2021.

[32] Thakre, Kishor, Kanungo Barada Mohanty, Aditi Chatterjee, and Vinaya Sagar Kommukuri. "A modified circuit for symmetric and asymmetric multilevel inverter with reduced components count." International Transactions on Electrical Energy Systems 29, no. 6 (2019): e12011.

[33] Hosseinzadeh, Mohammad Ali, Maryam Sarbanzadeh, Elham Sarbanzadeh, Marco Rivera, and Patrick Wheeler. "New Asymmetric Cascaded Multi-level Converter with Reduced Components." In 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), pp. 1-6. IEEE, 2018.

[34] Khosroshahi, Mahdi Toopchi, Ali Ajami, Ata Ollah Mokhberdoran, and Mohammadreza Jannati OsKuee. "Multilevel hybrid cascade-stack inverter with substantial reduction in switches number and power losses." Turkish Journal of Electrical Engineering & Computer Sciences 23, no. 4 (2015): 987-1000.

[35] Thiruvengadam, Annamalai. "An enhanced H-bridge multilevel inverter with reduced THD, conduction, and switching losses using sinusoidal tracking algorithm." Energies 12, no. 1 (2019): 81

[36] Meraj, Sheikh Tanzim, Nor Zaihar Yahaya, Kamrul Hasan, and Ammar Masaoud. "A hybrid T-type (HT- type) multilevel inverter with reduced components." Ain Shams Engineering Journal (2021)

[37] Gupta, K.K. and Jain, S., 2012. Topology for multilevel inverters to attain maximum number of levels from given DC sources. *IET Power Electronics*, *5*(4), pp.435-446.

[38] S. N. Rao, D. V. A. Kumar, and C. S. Babu, "Grid Connected Distributed Generation System with High Voltage Gain Cascaded DC-DC Converter Fed Asymmetric Multilevel Inverter Topology," Int. J. Electr. Comput. Eng., vol. 8, no. 6, p. 4047, 2018, doi: 10.11591/ijece.v8i6.pp4047-4059.

[39] A. Belkaid, I. Colak, and O. Isik, "Photovoltaic maximum power point tracking under fast varying of solar radiation," Appl. Energy, vol. 179, pp. 523–530, 2016, doi: 10.1016/j.apenergy.2016.07.034.

[40] J. G. Nielsen, F. Blaabjerg, and N. Mohan, "Control strategies for dynamic voltage restorer compensating voltage sags with phase jump," Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC, vol. 2, pp. 1267–1273, 2001, doi: 10.1109/apec.2001.912528.

[41] P. Boonchiam and N. Mithulananthan, "Diode-clamped Multilevel Voltage Source Converter Based on Medium Voltage DVR," pp. 590–595, 2008.

[42] B. Wang, G. Venkataramanan, and M. Illindala, "Operation and control of a dynamic voltage restorer using transformer coupled H-Bridge converters," IEEE Trans. Power Electron., vol. 21, no. 4, pp. 1053–1061, 2006, doi: 10.1109/TPEL.2006.876836.

[43] K. Chandrasekaran and V. K. Ramachandaramurthy, "An improved Dynamic Voltage Restorer for power quality improvement," Int. J. Electr. Power Energy Syst., vol. 82, pp. 354–362, 2016, doi: 10.1016/j.ijepes.2016.02.036.

[44] M. I. Marei, A. B. Eltantawy, and A. A. El-Sattar, "An energy optimized control scheme for a transformerless DVR," Electr. Power Syst. Res., vol. 83, no. 1, pp. 110–118, 2012, doi: 10.1016/j.epsr.2011.09.015.

[45] A. J. Visser, J. H. R. Enslin, and H. D. T. Mouton, "Transformerless series sag compensation with a cascaded multilevel inverter," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 824–831, 2002, doi: 10.1109/TIE.2002.801067.

[46] A. M. Massoud, S. Ahmed, P. N. Enjeti, and B. W. Williams, "Evaluation of a multilevel cascaded-type dynamic voltage restorer employing discontinuous space vector modulation," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2398–2410, 2010, doi: 10.1109/TIE.2010.2041732.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

This article has been accepted for publication in IEEE Access. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/ACCESS.2022.3196174

Devalraju Prasad received the B.Tech. Degree in electrical and electronics engineering from JNTUA, Andhra Pradesh, India, in 2009, the M.Tech. Degree in electrical power systems from JNTUA, Andhra Pradesh, India, in 2015. He is perusing Ph.D. degree in the field of Power Electronics at Vellore Institute of Technology, Vellore, India. His research activities are in the area of multilevel inverters, power converters, and active power filters and power quality.

Dhanamjayulu C (Senior Member, IEEE) received the B.Tech. Degree in electronics and communication engineering from JNTU University, Hyderabad, India, the M.Tech. Degree in control and instrumentation systems from the Indian Institute of Technology Madras, Chennai, India, and the Ph.D. degree in power electronics from the Vellore Institute of Technology, Vellore, India. He was invited as a Visiting Researcher with the Department of Energy Technology, Aalborg University, Esbjerg, Denmark, funded by the Danida Mobility Grant, Ministry of Foreign Affairs of Denmark on Denmark's International Development Cooperation. He was a Postdoctoral Fellow with the Department of Energy Technology, Aalborg University, from October 2019 to January 2021. Since 2010, he has been a Senior Assistant Professor with the Vellore Institute of Technology. His research interests include multilevel inverters, power converters, active power filters, power quality, grid connected systems, smart grid, electric vehicle, electric spring, and tuning of memory elements and controller parameters using soft switching techniques for power converters, average modelling, steady-state modelling, and small-signal modelling stability analysis of the converters and inverters. He is an Academic Editor of the journal International Transactions on Electrical Energy Systems (Wiley-Hindawi).

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/