SOLARCAP: Super Capacitor Buffering of Solar Energy for Self-Sustainable Field Systems

Amal Fahad[†], Tolga Soyata[*], Tai Wang[*], Gaurav Sharma[*], Wendi Heinzelman[*], Kai Shen[†]
[*]Dept. of Electrical and Computer Engineering
University of Rochester
Rochester, NY 14627
{soyata, twang33, sharma, wheinzel}@ece.rochester.edu
[†]Dept. of Computer Science
University of Rochester
Rochester, NY 14627
{fahad, kshen}@cs.rochester.edu

***Abstract*—Intelligent systems like automatic highway traffic management, area surveillance, and geological activity monitoring require substantial data collection and processing in the field. Energy self-sustainability is a critical foundation for successful field systems that are away from the power grid infrastructure. Instead of the conventional battery-based energy storage, this paper argues that the super capacitor buffering of solar energy (*SOLARCAP*) has the advantages of precise energy lifetime awareness, low maintenance, and operational robustness. By designing and developing a prototype implementation of the circuitry required for management and harvesting of energy, we demonstrate a SOLARCAP system that ensures safe device operation within the permitted voltage range.**

I. Introduction

Industrial and societal systems in the physical world have recognized the value of data-driven intelligence. For example, in intelligent transportation systems [1], high-speed cameras and sensors capture a large volume of data on traffic and road conditions. Online processing and action on such data enables a new level of accountability (vehicle license plate identification [2]), safety (automatic speed monitoring and integrated weather/traffic signaling), and efficiency (congestion-aware vehicular traffic routing). Similarly, detection and analysis of imagery changes [3] can help identify moving objects and activity patterns in area surveillance and security (such as the million-plus cameras in London [4]).

In these systems, data processing *in the field*, where data sources and control signals reside, has several key advantages. First, intelligent feature recognition and filtering at the data sources allows the systems to operate at much larger scales than centralized systems for which the network bandwidth bottlenecks restrict the ability to grow. Second, by relying less on the unreliable (often wireless) communications in the field, the overall system reliability is enhanced. Finally, local processing permits faster response to emergent events.

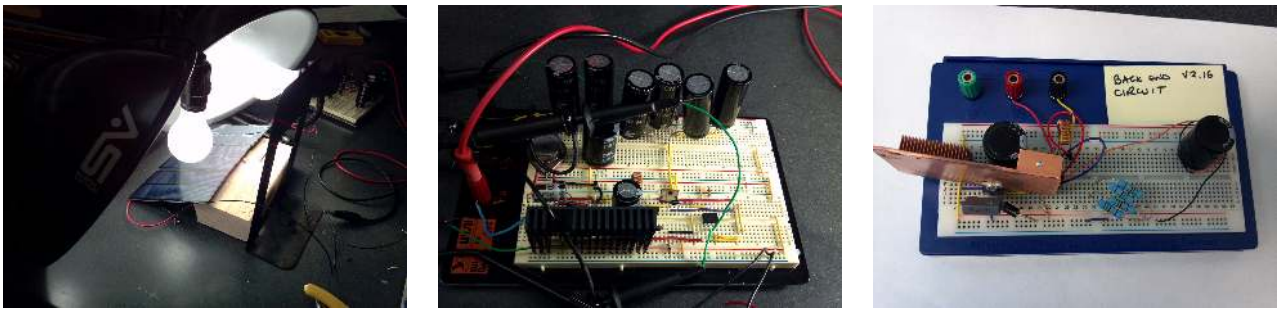
Self-sustainability is critical for successful data processing in the field. Complete wire-free field systems possess strong economic competitiveness due to their easy installation and maintenance. Self-sustainable systems are also environmentally friendly by not using the fossil-fuel based grid power. Specifically, a field node must live on ambient energy sources (e.g., solar cells) and energy storage. Conventional rechargeable battery-based energy storage has drawbacks of not allowing a precise estimate of remaining energy, requiring periodic maintenance, and having a negative environmental impact from the chemistry involved. To address these problems, we present a new approach to self-sustainable field systems through the use of the super-capacitor-based solar energy buffering, a system that we call *SOLARCAP*.

Using solar panels paired with super-capacitors presents unique opportunities and challenges: while rechargeable batteries can reach their peak voltage rather quickly, it is challenging to find an analytical relationship to their *stored energy* by observing their output voltage. The stored energy in a super-capacitor, on the other hand, is precisely calculated as $E = \frac{1}{2}CV^2$, where C and V are the capacitance and the voltage of the super-capacitor, respectively. This ease of assessing the stored energy, however, is countered with a disadvantage: the super-capacitor voltage (V) increases monotonically as it builds up energy, eventually reaching a maximum value (2.7 V for the Maxwell BCAP3000 series we used [5]). Therefore, the voltage output of a super-capacitor block may be much lower or much higher than the operation voltage of the circuit it is powering, which dictates a sophisticated circuit design to harness all of the stored energy.

In this paper, we argue that, with proper circuit design, super-capacitors hold the potential of being a disruptive technology within the embedded application environments we study. Although super-capacitors have been widely used in industry (e.g., automotive [6], [7], elevators [8]), to the best of our knowledge, this is the first paper that describes the usage of super-capacitors as the sole energy source for field embedded devices with a specific circuit and system design. The rest of this paper describes our SOLARCAP hardware platform, energy management circuit, and a prototype evaluation.

II. Self-Sustainable Hardware Platforms

Our energy harvesting and buffering mechanisms must support sufficient computing and data processing capacities for field applications. One example field system is an Alix embedded board based on the AMD Geode 500 MHz processor, running the Linux operating system and Open Source Computer Vision Library (OpenCV) image processing tasks. It consumes 3.2 W during full utilization, at the operation voltage of 8 V (400 mA). To create a self-sustainable system that can generate such power continuously, we describe the operational details of the solar panels and the super-capacitors.



(a) Emulated bright-day solar supply (b) Front-end circuit prototype (c) Back-end circuit prototype

Fig. 1. Prototype SOLARCAP hardware. The circuit has been developed in two different phases: 1) Front-end supply transfers the energy from the solar panels into the super-capacitors, 2) Back-end circuit is a DC-DC buck converter to produce a low-ripple voltage supply from the super-capacitor energy

A. Energy Generation Using Solar Panels

The Radio Shack Model 277052 solar panels we have employed in our experiments are shown in Figure 1a. Each panel is rated at 6 V, 1.5 W, which suggests an aggregate 4.5 W power output for the three panels connected in series. Unfortunately, this simple math does not hold true due to the non-linear I–V relationship of typical photovoltaic solar panels. Characterized by their open-circuit voltage (V_{OC}), and short-circuit current (I_{SC}), solar panel current decreases from I_{SC} down to zero while its output voltage increases from zero (@I=I_{SC}) to V_{OC} (@I=0). This behavior results in a non-linear concave power curve that has a maximum between these two extremes, referred to as the Maximum Power Point (MPP) in the literature [9].

To determine the specific values for the solar panels we have employed in our project, we varied the voltage output of the three-series-connected solar panels and plotted the resulting power output in Figure 2. While the V_{OC} of the three Radio Shack panels in series was 17.15 V (which is consistent with the advertised 6 V per panel), the maximum current attainable was 148 mA at short circuit (i.e., when the solar panel output is zero volts). The Maximum Power Point (denoted as MPP going forward) was approximately 1.8 W total, which is below the advertised 4.5 W, partially due to our lower-than-optimum irradiation level. The most important parameter to note is the voltage and current at MPP, which was reached when V = 13.3 V and I = 132.7 mA. From the standpoint of circuit design, the voltage at MPP will play a crucial role, as will be explained in the next section. Also note the sharp drop in the power output above the MPP and the smooth decrease below the MPP. These concepts will be the key points to consider during the circuit design.

B. Energy Storage—Super Capacitors

While rechargeable batteries are commonly used for energy storage, we have chosen super-capacitors to be the storage element due to their key advantages that make them better suited for self-sustainable, low-maintenance systems in the field as shown below:

1) Since super-capacitors are in fact capacitors, their energy levels and charge/discharge patterns are extremely predictable. Their stored energy, $E = \frac{1}{2}CV^2$, can be calculated by measuring their terminal voltage, V. A super-capacitor block consisting of four series 3000 F super-capacitors can operate a 3.2 W computing board for about four hours at full charge. The ability of precisely computing the remaining energy allows new lifetime-aware management on self-sustainable devices.
2) The porous material used to manufacture super-capacitors is free of environmentally-harmful acid and other corrosive chemicals and yields near-infinite life-time ($\approx 10^6$ charge cycles), implying lower maintenance costs and environmental-friendliness as compared to rechargeable batteries, supporting $\approx$ 5000 charge cycles.
3) Due to their extremely low ESR (Equivalent Series Resistance) of $\approx 1m\Omega$, super-capacitors have a $10\times$ higher power density, permitting them to charge/discharge quickly to absorb sudden peaks in the solar panel output, while supplying bursty power output (e.g., triggered by the sudden arrival of interesting data).
4) Super-capacitor capacitance drops only 2% between $-20°C$ and $60°C$, and 5% between $-40°C$ and $-20°C$, making them a perfect candidate for field deployment.

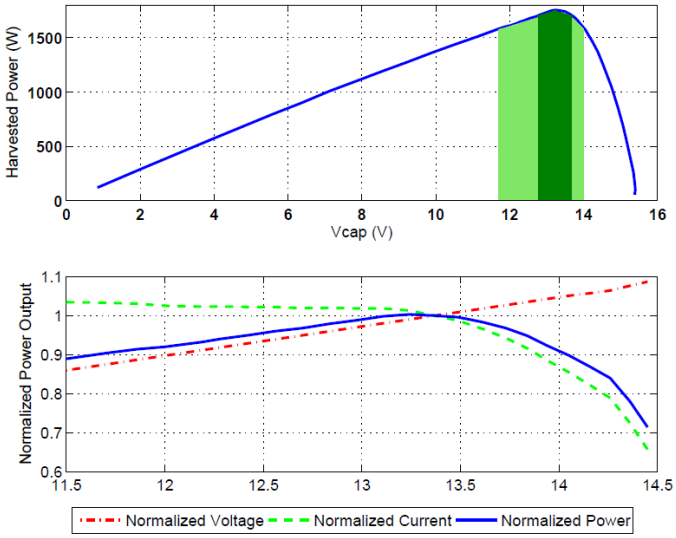


Fig. 2. Non-linear I-V curve of the three series solar panels. Maximum Power Point (MPP) is reached at 13.3V

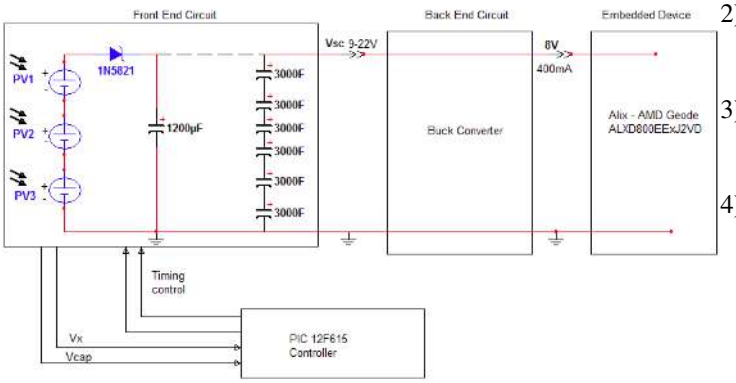


Fig. 3. Building blocks of the solar harvesting/storage system

Alternatively, the rechargeable batteries lose their storage capacity gradually at each charge cycle.

III. System Design

The high level outline of the circuit we have developed is shown in Figure 3, which consists of a *Front End Circuit* to transfer the harvested solar energy into the super-capacitors, a *Back End Circuit* that converts the energy inside the super-capacitors to a constant voltage and a PIC microcontroller to execute the control algorithm for the system. These components are explained in the following subsections.

A. Front End Circuit

As shown in Figure 2, the Maximum Power Point (MPP) of the solar panels is reached at $V_{CAP} = 13.3$ V, where V_{CAP} is the voltage of the *staging capacitor* that quickly absorbs the generated solar energy. The MPP of the solar panel block must be continously manipulated based on its irradiation levels by varying V_{CAP}. In Figure 2, the dark and light green areas signify efficiency boundaries of 95 - 98% and 98 - 100%, respectively. The goal of the Front End circuit is to keep the voltage of the staging capacitor contiously manipulated to stay within these most efficient regions.

Figure 4 shows the Front End circuit, which employs the CV (Constant Voltage) [9] method and directs the power generated by an array of three solar panels into the staging capacitor. A 1200 μF staging capacitor is selected, which can vary its voltage (i.e., V_{CAP}) within the dark green region (13.0 - 13.5 V) in 5 ms and within the entire green region (12.5 - 13.7 V) within 11 ms. This response time is low enough to quickly change V_{CAP} based on varying irradiation levels, yet slow enough to permit the energy transfer with a PIC 12F615 MCU containing a 35 μs-conversion-time SAR-ADC. The 1N5821 Shottky diode we used has a 320 mV voltage drop at the MPP of 130 mA. In our experiments, we contemplated using one or more series solar panels. We have observed that the advantages and disadvantages of using multiple panels are as follows:

1) Single and multiple solar panel configurations all have the same number of switching transistors and Shottky diodes, allowing the latter configuration to better amortize the energy losses of these components.
2) The overall efficiency is increased when the staging capacitor output is stored at a higher voltage, since step-down conversion is more efficient [10].
3) Higher voltages of multiple panels permit higher energy storage using smaller capacitors due to the quadratic dependence on voltage (i.e., $E = \frac{1}{2}CV^2$).
4) Different solar panels have mismatched I-V characteristics. We measured the MPP of three different panels to yield 715 mW (@169 mA), 698 mW (@155 mA), and 669 mW (@160 mA) at a specific irradiation level. When forced to work at a common current due to the series configuration, we observed them to yield $\approx 10\%$ lower aggregate power due to these mismatches.
5) Above $\approx$100 V, high voltage switching devices must be used, which are much less efficient at low power consumption levels, limiting the number of panels to ≈ 6 for efficient operation.

Based on these advantages and disadvantages, we employed the three-series solar panel configuration, which more than recoups its I-V mismatch-related losses due to the other advantages. The staging capacitor voltage V_{Cap} is controlled very precisely by transferring the accumulated energy into the super capacitor block in small amounts. This transfer is accomplished by the Front End circuit which works in Buck converter mode [10] when V_{Cap} is higher than the voltage across the super-capacitor storage unit (denoted as V_{SC}), and switches to Boost Mode when $V_{Cap} \leq V_{SC} + V_{Loss}$, where V_{Loss} is a term to account for the aggregate voltage drops across the PNP and the diode. Each energy transfer drops V_{Cap} by an amount of ΔV and transfers it to the 220 μH inductor. The energy loss/gain in the capacitor and inductor must be equal as shown below (ignoring the energy losses in the resistors, inductor, and the two transistors for simplicity)

$$\begin{aligned} \Delta E(C) &= \tfrac{1}{2} \times 1.2 \times 10^{-3} \times (13.305^2 - 13.300^2) \\ \Delta E(L) &= \tfrac{1}{2} \times 220 \times 10^{-6} \times (I_2^2 - I_1^2) \\ \Delta E(C) &\approx \Delta E(L) = 80\mu J \\ (I_1^2 - I_2^2) \approx 0.73A \implies & \boxed{I_2 \approx 1A \quad I_1 \approx 0.5A} \end{aligned} \tag{1}$$

where 13.30 V is the selected optimum V_{CAP} and is permitted to rise 5 mV before the energy is transferred by turning on the PNP transistor. PNP transistor is driven to saturation by applying 5 V to the GP4 input of the 2N2222 NPN transistor. This causes the energy to be transferred to the inductor in a period of Δt which can be calculated as follows

$$\begin{aligned} V_L = L \times \frac{dI}{dt} &\approx L \times \frac{\Delta I}{\Delta t} \\ V_{Cap} - V_{SC} - V_{CESat} &= 220 \times 10^{-6} \times \frac{0.5}{\Delta t} \\ 13.3 - 10 - 0.7 &= \frac{110 \times 10^{-6}}{\Delta t} = 2.6 \\ & \boxed{\Delta t = 42\mu s} \end{aligned} \tag{2}$$

where 42 μs is the time to transfer 80 μJ from the capacitor into the inductor when the voltage difference between V_{SC} and

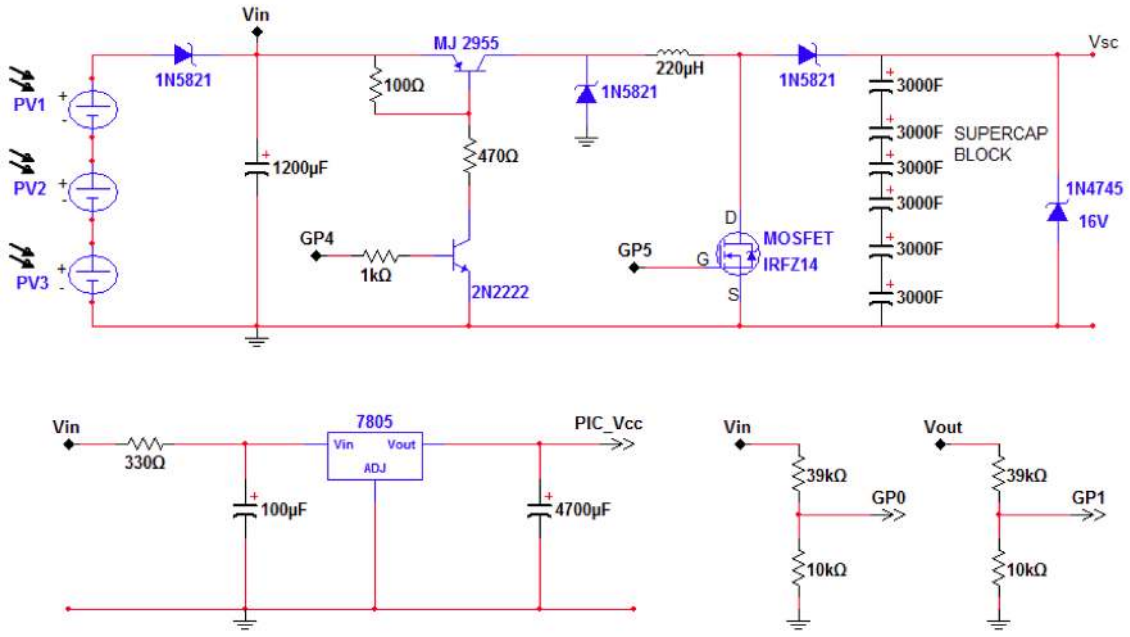


Fig. 4. Front End Circuit is used to transfer the energy generated by the solar panels into the super-capacitor block.

V_{CAP} is only 3.3 V. This time will get progressively higher when the voltage difference gets lower due to the rising V_{SC} as it builds up energy. In our circuit, the measurement of the V_{in} and V_{SC} nodes take approximately 35 μs which is the amount of time it takes the SAR ADC (inside the PIC) to finish its conversion. When the voltage difference is lower, we turn on the MOSFET by applying a logic 1 to the GP5 node to accelerate the transfer (i.e., Boost mode). In Boost mode, $\Delta t = \frac{110\times10^{-6}}{12.5} \approx 9\,\mu s$, since, based on Equation 2, V_{SC} is replaced with the saturation voltage of the MOSFET (0.1 V), resulting in a dramatically accelerated transfer. Enabling boost mode, however, causes the efficiency of the transfer to go down since the Boost circuits are less efficient by design.

A 1:5 resistor divider (i.e., 10 $k\Omega$ and 39 $k\Omega$) is used for both V_{In} and V_{SC} nodes to match the PIC V_{DD} (5 V) to these nodes' voltages (max $\approx$ 25 V). Front-end prototype is shown in Figure 1b which uses a standard 7805 voltage regulator. Despite its 60% efficiency of this regulator, since the PIC current is only in the few mA range, this inefficiency does not contribute more than 1% to the overall efficiency. The main contributor to the PIC power consumption is indeed the driving current of the 2N2222 transistor which is around 4 mA.

B. System Control Software

The primary function of the PIC control software is to continously sample the V_{In} and V_{SC} voltages applied to its input pins GP0 and GP1, respectively, and to control the energy flow from the 1200 μF energy-staging capacitor into the inductor by activating the PNP (GP4) and the MOSFET (GP5). When V_{in} reaches 13.305 V, the MJ 2955 transistor is turned on by applying a Logic 1 to GP4, allowing a current to flow through the inductor ranging in magnitude between 0.5 to 1A. This current increases the magnetically stored energy in the inductor, thereby reducing the voltage at V_{In}. This energy must be transferred at a precisely determined value, since 1) transferring too little energy will cause the MPP to shift to above the green area, thereby sharply reducing the power output 2) transferring too much energy will cause the operating voltage to fall below the green area, again, causing a less-than-optimum power energy generation.

While GP4 is used to control the flow of the energy from the solar panel staging capacitor into the super-capacitor side, GP5 is turned on when this energy transfer has to be accelerated. GP4 is used to operate the circuit in the *Buck converter* [10] mode, whereas switching GP5 will allow the circuit to switch to *Boost converter* mode. GP5 has to be activated for for two reasons: 1) if the energy transfer has to be accelerated during times when the solar panel output peaks and the energy has to be transferred faster, 2) if the voltage of the super-capacitor block exceeds $V_{In} + V_{Loss}$, where V_{Loss} is a term used in the program to represent the voltage drops due to V_{CESat} of the PNP ($\approx$ 500 - 800 mV), and V_F of the Shottky diodes ($\approx$ 500 mV at 1 A).

C. Back End Circuit

As shown in Figure 6, the Back End circuit is a typical buck converter which converts the super-capacitor voltage to a constant voltage output to operate the embedded board connected to the output. In our implementation, we have used a board that requires an $\approx$ 8 V input and draws 400 mA. The buck converter we have utilized is the ON-SEMI MC33167T switching regulator which is capable of providing a maximum of 5 A output. The 1.5 $k\Omega$ and 1 $k\Omega$ resistor divider keeps the output at $V_{out} = 5.05 \times \frac{2.5}{1.5} \approx 8.4\,V$. The prototype of the Back End Circuit is shown in Figure 1c.

IV. Performance Evaluation

The two prototypes we have built are shown in Figure 1 along with the setup we have utilized to simulate an artificial

```
const unsigned int BestVin=530;
const unsigned int Vloss=100;
const unsigned char FREQ=20;
unsigned int Vout,Vin,Voutctrl;
unsigned char ON_charge=1, ONC;

void Init()
{
     // Gp0 = Vin, Gp1 = Vout, Gp4 = Enable, Gp5=PWM
     TRISIO  = 0B00001011;
     // ADC FRC clock, set GP0 and Gp1 to analog
     ANSEL   = 0B01110011;
     GPIO.B4 = 0;                GPIO.B5 = 0;
}
void main(){
        Init();
        Vout=ADC_read(1);
    while(1)
    {
      Vin=ADC_read(0);
      //Spin until Vin reaches 13V
      while (Vin<BestVin){
          GPIO.B4 = 0;          GPIO.B5 = 0;
          Vin=ADC_read(0);
      }
        ///////// BUCK OPERATION  /////////
      if(Vin>Vout+Vloss){
          if (Vin>BestVin)  GPIO.B4 = 1;
          else              GPIO.B4 = 0;
          Voutctrl--;
          if (Voutctrl==0){
             Vout=ADC_read(1);
             Voutctrl=10;
          }
      } else {
        ///////// BOOST OPERATION  /////////
        GPIO.B4=1;          GPIO.B5=1;
        ONC=ON_Charge;  while (ONC--);
        GPIO.B5=0;
        GPIO.B4=0;
        Vin=ADC_read(0);
        /////   DUTY CYCLE ADJUSTMENT  /////
        if ((Vin>BestVin) &&(ON_charge<(FREQ-2))) {
          ON_charge++;
        }
        if ((Vin<BestVin) &&(ON_charge>2)) {
          ON_charge--;
        }
        Vout=ADC_read(1);
        Voutctrl=10;
        }
      }
  }
```

Fig. 5. Microchip mikroC PRO code used to control the Front End Circuit.

light source using a 100 W light bulb. A digital Tektronix oscilloscope is used to measure the switching activity throughout the energy transfer. We have used the Windows-based program provided by Tektronix to record the switching patterns as well as the voltage levels at V_{In} and V_{CAP}.

Initially, six 70 F, 2.7 V super-capacitor units are discharged. These lower-valued super-capacitors were used for testing to span the entire voltage range within a few minutes during the experiments, rather than the actual 3000 F block which would require almost a day to charge. Figure 7a shows snapshots of the oscilloscope output when the circuit is operating. The super-capacitor voltage (blue) started rising from 0 V to 16 V, eventually limited by the 16 V Zener protection diode. The PIC code allowed the V_{Cap} (yellow) to reach the MPP and started activating the PNP to transfer the energy to the inductor via 45 μs pulses on GP4 (purple). This continued until the super-

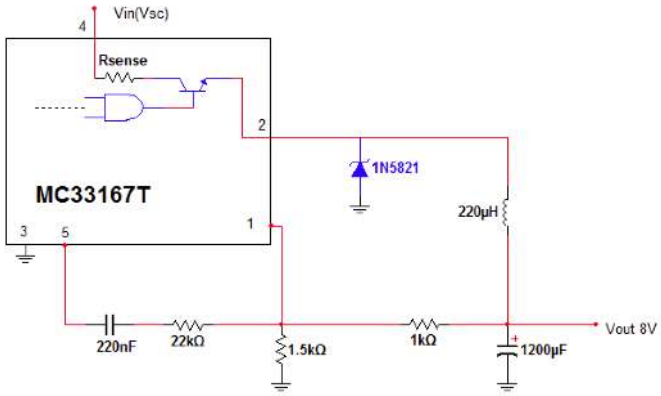


Fig. 6. Back End Circuit as a constant voltage for the embedded board.

capacitor voltage has risen above the $V_{In}+V_{Loss}$, where V_{Loss} is the minimum difference allowed (i.e., drop-out). The circuit at that point switched to boost mode as shown in Figure 7b. In boost mode, the energy transfer requires much shorter pulses ($\approx 20\,\mu s$ in the Figure 7b). We have observed the output of the final back-end converter to be fixed at 8.4 V from $V_{SC} = 10.5$ V up to $V_{SC} = 16$ V. We leave cloud computing using sychronous optimization as future work [11]–[15].

(a) Buck operation

(b) Boost operation

Fig. 7. Oscilloscope snapshots during (a) Buck and (b) Boost operation.

V. RELATED WORK

Solar panels and MPPT have been well studied. [16] presents a solar energy harvesting circuit for mobile phone battery chargers, which is capable of MPPT with a built-in battery protection. [17] used miniaturized photovoltaic

modules to perform automatic maximum power point tracking with minimum energy cost. [18] and [19] provide systems designs using solar panels for ultra-low power and unattended harvesting. The challenges in deciding the state of charge of a rechargeable batteries has been well studied in the literature [20]–[23]. The research on super-capacitors has mainly focused on their usage in vehicles due to their superior ability to quickly absorb the brake regeneration energy [6] or similar applications, such as elevators, where the storage and usage of the energy is in large energy bursts [8]. Recently, the usage of super-capacitors in bio-medical implants has been introduced as the primary source of energy buffering [24] and the usage of super-capacitors in mobile devices [16].

VI. CONCLUSION

This paper argues that the super capacitor buffering of solar energy (SOLARCAP) is a feasible foundation for future self-sustainable field systems. Compared to the conventional battery-based energy storage, SOLARCAP requires lower maintenance and it is much more environmentally friendly. We demonstrate that proper energy management circuitry along with system control software can ensure safe operation within permitted voltage range and harness the full buffered energy. Our SOLARCAP prototype can power a computing board with a 3.2 W of power consumption that can support conventional system software like Linux and perform field image processing like OpenCV. The super capacitors have relatively small energy storage capacity. We believe this can be mitigated by software-level adaptive resource management techniques. For example, most practical applications receive data at variable rates or patterns. The field system only needs to be powered when necessary so that it can stay in a low-power state over long periods of time. In addition, the software system and application can present dynamic knobs to tune between the processing quality-of-service and energy usage [21]. Specifically, a lower-level quality-of-service may be desirable to maintain sufficient system lifetime during low-energy periods. SOLARCAP's precise energy lifetime awareness is particularly beneficial to enable such software management.

ACKNOWLEDGMENT

This work was supported in part by the National Science Foundation grants CCF-0448413 and CCF-0937571.

REFERENCES

[1] P. F. Williams, "Street smarts: How intelligent transportation systems save money, lives and the environment," ACS Transportation Solutions Group, Xerox, Tech. Rep., Feb. 2009, http://www.acs-inc.com/wp_street_smarts_intelligent_transportation_systems.aspx.

[2] C. Anagnostopoulos, I. Anagnostopoulos, V. Loumos, and E. Kayafas, "A license plate-recognition algorithm for intelligent transportation system applications," *IEEE Trans. on Intelligent Transportation Systems*, vol. 7, no. 3, pp. 377–392, Sept. 2006.

[3] A. Mittal and D. Huttenlocher, "Scene modeling for wide area surveillance and image synthesis," in *Proc. of the IEEE Conf. on Computer Vision and Pattern Recognition*, Hilton Head, SC, June 2000, pp. 160–167.

[4] J. Malanowski, "Big Bother: How a million surveillance cameras in London are proving George Orwell wrong," *Washington Monthly*, Nov. 2009.

[5] Maxwell Corp., "K2 Series High Capacity Cells," 2012, http://www.maxwell.com/products/ultracapacitors/products/k2-series.

[6] N. Jinrui, W. Zhifu, and R. Qinglian, "Simulation and Analysis of Performance of a Pure Electric Vehicle with a Super-capacitor," in *IEEE Vehicle Power and Propulsion Conference*, 2006, pp. 1–6.

[7] H. Zhang, Y. Sun, S. Ding, and Y. Wang, "Application of super capacitor with full-digital converter in hybrid electric vehicle energy transmission system," in *27th Chinese Control Conference*, 2008, pp. 212–215.

[8] A. Rufer and P. Barrade, "A supercapacitor-based energy storage system for elevators with soft commutated interface," *IEEE Transactions on Industry Applications*, vol. 38, no. 5, pp. 1151–1159, 2002.

[9] R. Faranda and S. Leva, "Energy comparison of mppt techniques for pv systems," *WSEAS Transactions on Power Systems*, vol. 3, no. 6, pp. 446–455, 2008.

[10] A. Pressman, K. Billings, and T. Morey, *Switching Power Supply Design*. Mc Graw-Hill, 2009.

[11] T. Soyata and E. G. Friedman, "Synchronous performance and reliability improvements in pipelined asics," in *Proceedings of the IEEE ASIC Conference*, Sep 1994, pp. 383–390.

[12] T. Soyata, E. G. Friedman, and J. H. Mulligan, "Monotonicity constraints on path delays for efficient retiming with localized clock skew and variable register delay," in *Proceedings of the International Symposium on Circuits and Systems*, May 1995, pp. 1748–1751.

[13] T. Soyata, R. Muraleedharan, S. Ames, J. H. Langdon, C. Funai, M. Kwon, and W. B. Heinzelman, "Combat: mobile cloud-based compute/communications infrastructure for battlefield applications," in *SPIE Defense, Security, and Sensing 2009. Modeling and Simulation for Defense Systems and Applications VII*, vol. 8403-20, April 2012.

[14] T. Soyata, R. Muraleedharan, C. Funai, M. Kwon, and W. Heinzelman, "Cloud-Vision: Real-Time face recognition using a Mobile-Cloudlet-Cloud acceleration architecture," in *17th IEEE Symposium on Computers and Communications (IEEE ISCC 2012)*, Cappadocia, Turkey, July 2012.

[15] T. Soyata and J. Liobe, "pbCAM: probabilistically-banked content addressable memory," in *25th IEEE International System-on-Chip Conference*, Niagara Falls, NY, Sept. 2012.

[16] Y. C. L. Ian Y.W, Chung, "A low-cost photovoltaic energy harvesting circuit for portable devices," in *Proceedings of the IEEE PEDS 2011, Singapore, 5-8 December*, 2011, pp. 123–132.

[17] D. Brunelli, L. Benini, C. Moser, and L. Thiele, "An efficient solar energy harvester for wireless sensor nodes," in *Conf. on Design, Automation and Test in Europe (DATE)*, Munich, Germany, Mar. 2008, pp. 104–109.

[18] M. K. N. Khosropour, F. Krummenacher, "Fully integrated ultra-low power management system for micro-power solar energy harvesting applications," *Electronics Letters*, vol. 48, no. 6, pp. 338–339, 2012. [Online]. Available: http://link.aip.org/link/?ELL/48/338/1

[19] J. Kimball, B. Khun, and R. Balog, "A system design approach for unattended solar energy harvesting supply," *IEEE Transactions on Power Electronics*, vol. 24, no. 4, pp. 123–132, 2009.

[20] R. Casas and O. Casas, "Battery sensing for energy-aware system design," *Computer*, vol. 38, no. 11, pp. 48–54, Nov. 2005. [Online]. Available: http://dx.doi.org/10.1109/MC.2005.367

[21] H. Hoffmann, S. Sidiroglou, M. Carbin, S. Misailovic, A. Agarwal, and M. Rinard, "Dynamic knobs for responsive power-aware computing," in *16th Int'l Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, Newport Beach, CA, Mar. 2011, pp. 199–212.

[22] C.-h. Hsu and W.-c. Feng, "A power-aware run-time system for high-performance computing," in *Proceedings of the 2005 ACM/IEEE conference on Supercomputing*, ser. SC '05. Washington, DC, USA: IEEE Computer Society, 2005, pp. 1–. [Online]. Available: http://dx.doi.org/10.1109/SC.2005.3

[23] H. Zeng, C. S. Ellis, A. R. Lebeck, and A. Vahdat, "ECOSystem: Managing energy as a first class operating system resource," in *10th Int'l Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2002, pp. 123–132.

[24] W. Sanchez, C. Sodini, and J. Dawson, "An Energy Management IC for Bio-implants Using Ultracapacitors for Energy Storage," in *Symposium on VLSI Circuits/Technical Digest of Technical Papers*, 2010, pp. 63–64.