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BRIEF COMMUNICATION OPEN

Solution-based polycrystalline silicon transistors produced on a paper substrate

Miki Trifunovic[1], Paolo Maria Sberna[1], Tatsuya Shimoda[2] and Ryoichi Ishihara[1]

Printing of electronics is pursued as a low-cost alternative to conventional manufacturing processes. In addition, owing to relatively low process temperatures, flexible substrates can be used enabling novel applications. Among flexible substrates, paper was found to be a particularly interesting candidate, since it has an order of magnitude lower price than low-cost polymer alternatives, and is biodegradable. As ink materials, organic and metal-oxide semiconductors are thoroughly being investigated; however, they lack in electric performance compared to silicon in terms of device mobility, reliability, and energy efficiency. In recent years, liquid precursors for silicon were found and used to create polycrystalline silicon (poly-Si). However, fabrication of transistors on top of low-cost flexible substrates such as paper has remained an outstanding challenge. Here we demonstrate both p-channel and n-channel poly-Si thin-film transistors (TFTs) fabricated directly on top of paper with field-effect mobilities of 6.2 and 2.0 cm^2/V s, respectively. Many fabrication challenges have been overcome by limiting the maximum process temperature to approximately 100 °C, and avoiding liquid chemicals commonly used for etching and cleaning. Patterning of poly-Si has been achieved by additive selective crystallization of the precursor film using an excimer laser. This work serves as a proof of concept, and has the potential to further improve device performance. Owing to the low-cost, biodegradable nature of paper, and the high performance, reliability, and energy efficiency of poly-Si TFTs, this work opens a pathway toward truly low-cost, low-power, recyclable applications including smart packages, biodegradable health monitoring units, flexible displays, and disposable sensor nodes.

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INTRODUCTION

Integration of paper in electronics has sparked great interest due to the unique properties of paper despite fabrication challenges. The key features of paper are its recyclability, biodegradability, high porosity, importance for bio-chemical sensor applications[1–3] and low price (0.13 €/dm^2, Powercoat® HD) compared to low-cost polymer alternatives such as polyethylene naphthalate (PEN, 2.58 €/dm^2, Goodfellow) and polyethylene terephthalate (PET, 1.14 €/dm^2, Goodfellow). However, fabrication challenges arise as a result of the high porosity and surface roughness. In addition, the material cannot be exposed to temperatures higher than ~150 °C.[1] These limitations significantly impact the performance of electronics employing this substrate type. To avoid these limitations there have been reports of silicon electronics fabricated separately and transferred onto a paper substrate by pick & place methods.[4] Although this approach provides the best electronic performance, it falls short on economical advantages. For electronics directly fabricated on top of the substrate, although vacuum-based deposition on paper has been reported,[5,6] printing of liquid inks is the most economically desirable as it can be scaled up to roll-to-roll processes and has an additive patterning nature.[7]

Typical semiconducting ink materials, such as organic and metal-oxide semiconductors, lack in electronic performance compared to polycrystalline silicon (poly-Si).[8,9] Their typical field-effect mobilities are ~1 and ~10 cm^2/V s for organic and metal-oxide transistors, respectively. Although advances have been made in recent years, the device reliability is low due to their sensitivity to oxygen and moisture for organic,[10] and to light for metal-oxide devices.[11] Finally, these materials do not have balanced electron and hole mobilities, which prevents their implementation in complementary MOS (CMOS) circuits, and therefore makes them energy inefficient. Poly-Si on the other hand exhibits at least an order of magnitude higher mobilities (~100 cm^2/V s), is stable, and has both strong electron and hole devices enabling high-speed low-power applications.

Silicon inks were first reported in 2006[12] and employed at a relatively high annealing temperature (>350 °C), which obstructed their usage on low-cost flexible substrates, that typically have low-thermal budgets (<120–200 °C).[13] In 2015 an alternative process was reported which, synthesized poly-Si from the silicon ink by using an excimer laser.[14] Due to the short laser pulse duration (several nanoseconds) and high material absorption, the treatment is limited to the top several tens of nanometers of the silicon ink, avoiding significant damage to underlying substrates. Fabrication of transistors on top of paper remained challenging[15] as a result of the additional complexity when employing the substrate, such as avoiding high temperatures, wet chemicals other than the silicon ink, and additive patterning. In this work, we have successfully fabricated thin-film transistors (TFTs) directly on top of a paper substrate. We show a significant improvement in NMOS TFT by employing a blanket oxide etching prior to ion implantation, which limited the sample heating. In addition, we highlight solutions to three main challenges in the fabrication

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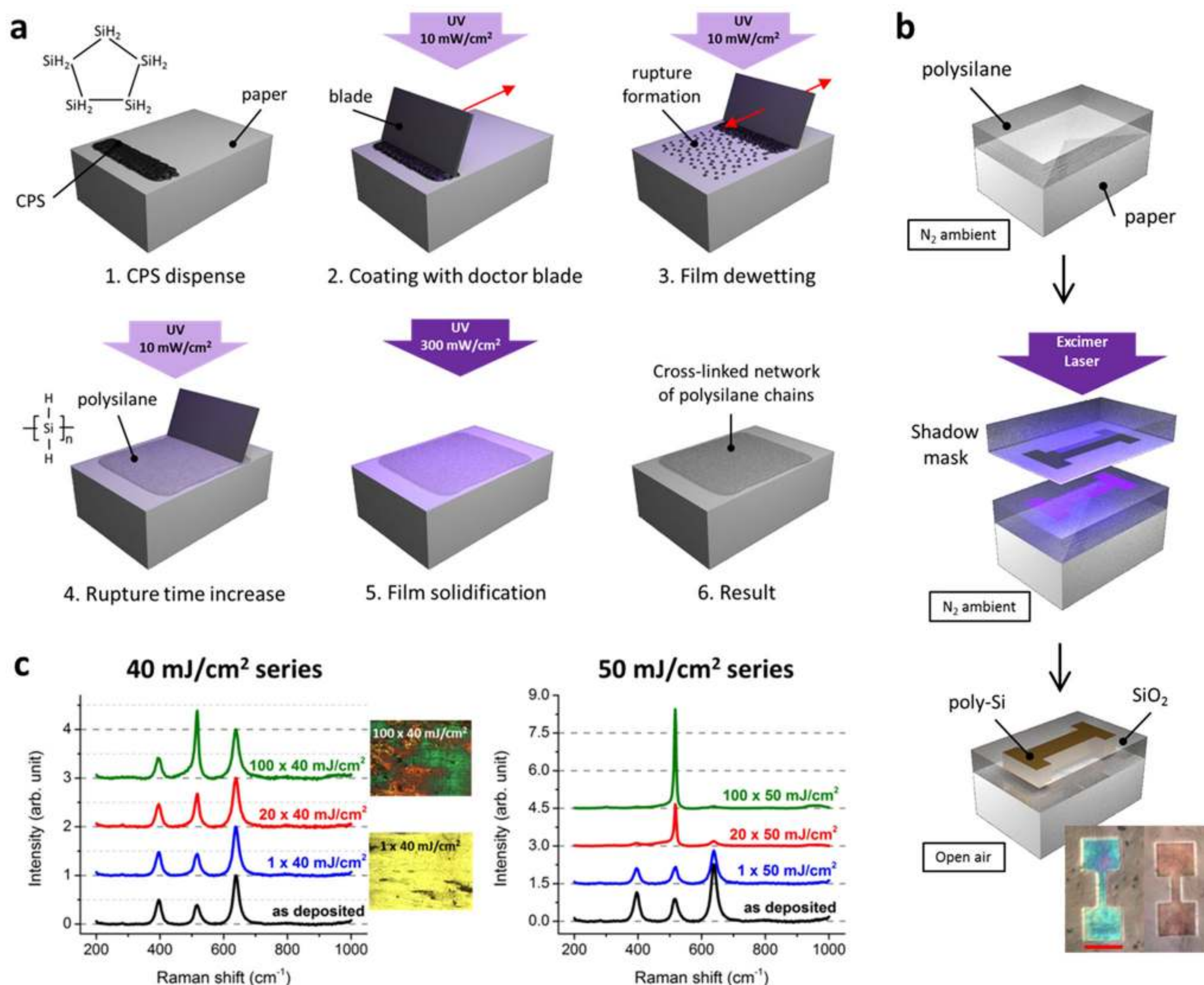

Fig. 1 Coating and crystallization of Si ink. **a** Diagram of the cyclopentasilane coating process on paper. Through continuous blade coating during UV polymerization, the liquid rupture time increases, resulting in an increasingly stable film. By using a high-intensity UV freeze, the film remains uniformly coated and is solidified. **b** Diagram of local crystallization of the polycrystalline silicon channel through a shadow mask, resulting in an additive patterning process. Red line in the microscope image inset indicates a size of 50 µm. **c** Raman spectroscopy measurement results of different laser crystallization recipes indicating numbers of pulses from 1 to 100 at laser fluences of 40 (left) and 50 (right) mJ/cm^2. Crystallization observed by the increasing Raman signal at 520 cm^{-1}. (Panel **c** reproduced with permission from ref. 15)

process: silicon ink coating, additive Si patterning, and metallic contact formation.

EXPERIMENTAL

The type of paper used in this work has a limited RMS roughness of less than 20 nm due to a protective coating on top of the substrate. Cyclopentasilane (CPS) was used as the liquid silicon precursor. This liquid was blade coated on the paper surface while being exposed to UV light, which gradually increases the viscosity of the ink through molecular ring-open polymerization.[16] After a stable film is formed, the film is solidified by a high-intensity UV light treatment for several seconds. This method was employed because the liquid has a poor wettability towards the substrate surface. The liquid must therefore be solidified before the film ruptures as a result of surface energy minimization. The rupture growth time is described by Eq. (1).[17]

$$\tau_{max} = \frac{48\pi^2 \gamma_{LA} \eta L^5}{|A_{ALS}|^2} \quad (1)$$

where τ_{max} is the maximum rupture growth time, γ_{LA} the surface free energy of the liquid–air boundary, η the viscosity of the liquid, L the thickness of the film, and A_{ALS} the Hamaker constant. The thickness of the liquid and its viscosity are two variables that are controlled. Although the thickness of the liquid has a strong impact in increasing the rupture growth time, there is a limitation to the amount of liquid to be used, since stresses in the film can cause it to crack as a result of hydrogen and silane radical effusion in the solidification process.[18] The viscosity is manipulated by photopolymerization of the CPS during coating. As soon as the rupture growth time reaches several seconds, a more intense UV light source can be employed to swiftly solidify the existing film. This process is illustrated in Fig. 1a.

For low-cost fabrication and also due to the liquid absorptive nature of paper, additive formation of poly-Si TFT patterns is desired. Polysilane can be crystallized in channel patterns by excimer-laser annealing through a shadow mask as shown in Fig. 1b. When left in open air, unexposed polysilane oxidizes into the insulating SiO_2 and electrically isolates the poly-Si channels. This method has been demonstrated by Okamoto et al.[19]

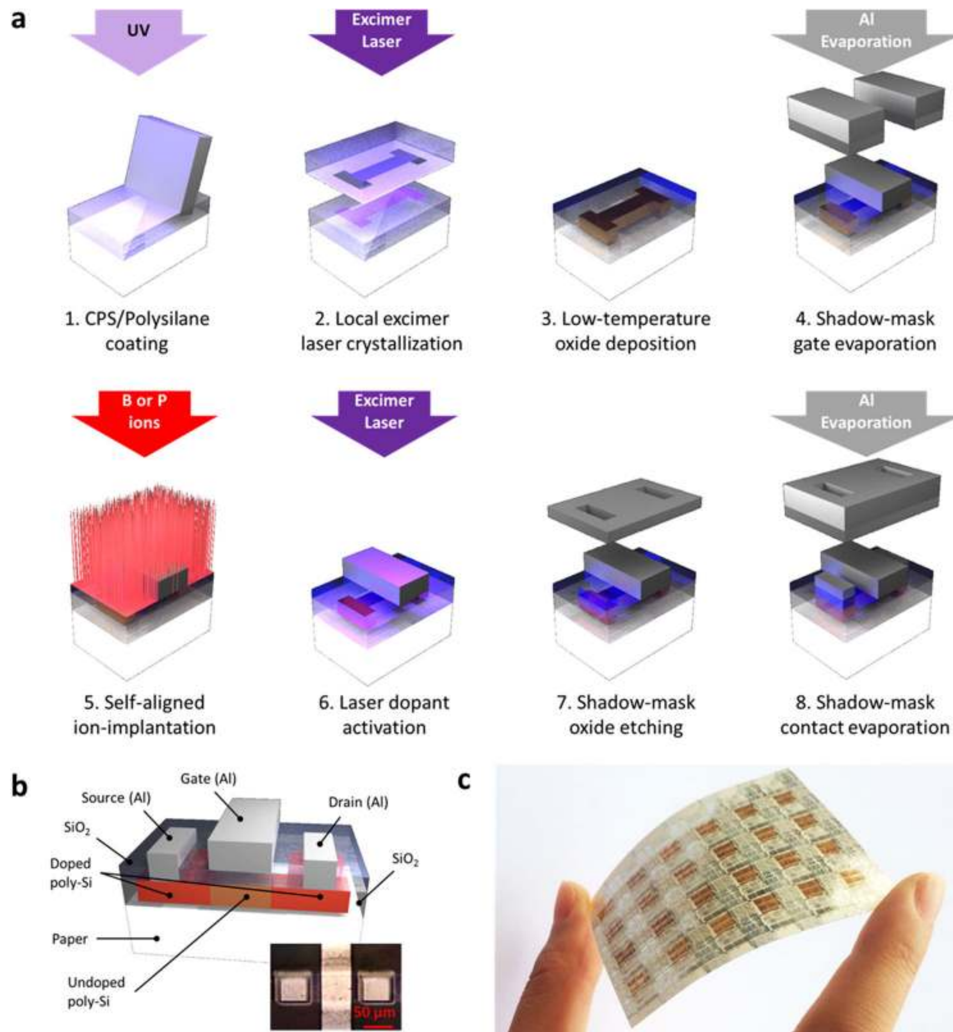

Fig. 2 Full liquid-Si-based TFT on paper fabrication process and results. **a** Diagram of the fabrication process of solution-based poly-Si TFTs on a paper substrate, starting with coating of CPS with UV light, excimer laser crystallization of the poly-Si channel, low-temperature oxide deposition, shadow mask gate evaporation, self-aligned ion-implantation, excimer laser dopant activation, shadow mask oxide etching, and finally shadow mask contact evaporation. **b** Diagram of the TFT cross-section with a microscope image of the fabricated TFT, red line indicating a size of 50 μm. **c** Optical image of the final sample of electronics on a paper substrate

for vacuum-based polysilane on a rigid substrate. Here we have applied the technique on solution-based polysilane on top of a paper substrate. Crystallization was confirmed by Raman spectroscopy as shown in Fig. 1c. Multiple laser pulses at a fluence of 50 mJ/cm^2 successfully crystallized the film. The color of the film changed from transparent to colorful, as a result of the material bandgap narrowing from 6.5 to ~2 eV.[20] Higher fluences would also lead to crystallization, although the film roughness will significantly increase due to hydrogen and silane radical outgassing and ablation.[14]

In order to imitate an additive metallic contact fabrication process, such as that used for printing, the desired Al shapes were directly formed by evaporation through a shadow mask, thereby avoiding the need to remove material in undesired locations. The mask was attached to the sample by an adhesive that has a melting temperature of ~80–100 °C. The adhesive was locally heated with a soldering iron around the edge of a carrier wafer in order to prevent the heat from reaching the paper. For the source and drain electrodes, prior to metal contact evaporation, oxide is removed by plasma etching through the same mask.

The full TFT fabrication process comprises eight main steps: CPS/polysilane coating, local excimer laser crystallization, low-temperature oxide deposition, shadow-mask gate evaporation, self-aligned ion implantation, laser dopant activation, shadow-mask oxide etching, and contact evaporation. All process steps were conducted below a maximum process temperature of ~100 °C. To limit the implantation energy of the n-type device, oxide was blanket stripped prior to implantation. A schematic of this process is shown in Fig. 2a. For a detailed description of the process, please refer to the "Methods" section. The TFT cross-section schematic and a microscope image are presented in Fig. 2b. An image of the final result is shown in Fig. 2c.

RESULTS

Transfer and output characteristics of two of the best performing P-type MOS transistor (PMOS) and N-type MOS transistor (NMOS) TFTs are shown in Fig. 3. With respect to the charge carrier mobility, the NMOS (2.0 cm^2/V s) performed had a lower value than the PMOS (6.2 cm^2/V s). This is attributed to the implantation damage by the heavier phosphorus ions that had not been effectively restored by the subsequent laser annealing step. According to calculations, the swing of the PMOS device surpasses the theoretical limit. We believe that the physics behind such a low swing is impact ionization-induced floating body effect, which imposes such an abrupt increase in drain current.[21] For a thorough

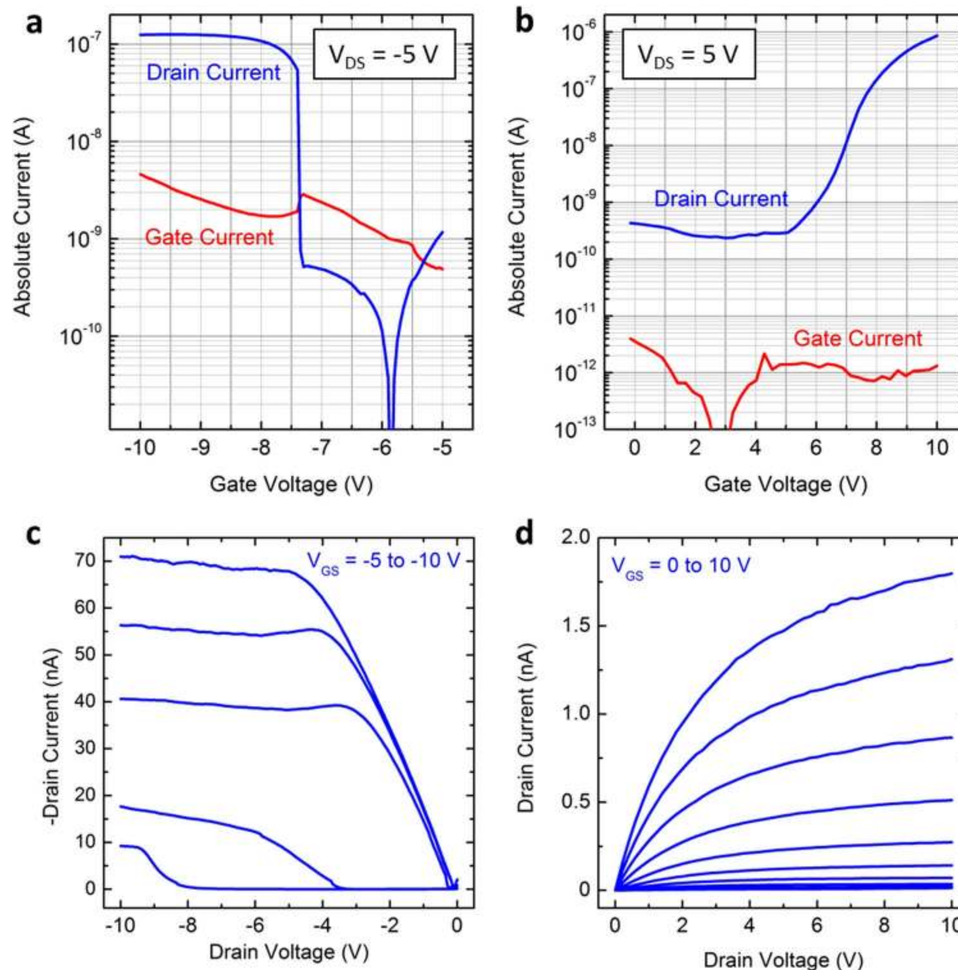

Fig. 3 Electric measurement results of liquid-Si-based TFTs produced on paper. **a** Transfer properties of PMOS TFT at a drain voltage of −5 V, showing both the drain current (blue), as well as the leakage current (orange). **b** Transfer properties of the NMOS TFT with a drain voltage of 5 V. **c** Output properties of the PMOS TFT with gate voltage ranging from −5 to −10 V in steps of 1.25 V. **d** Output properties of the NMOS TFT with gate voltages ranging from 0 to 10 V in steps of 1 V. All devices had a channel size of 50×50 µm. (Panels **a** and **b** reproduced, with permission, from ref. 15)

understanding a further investigation in this behavior is necessary. A high leakage current of 10^{-9} A is observed for the PMOS as a result of defects in the oxide from the sample heating by ion implantation. Since for the NMOS, the oxide layer was removed prior to implantation, lower energies could be used. As a result, heat production from implantation was limited, which minimized paper expansion, and the gate oxide of the NMOS stayed intact. Therefore, the NMOS performed significantly better in terms of leakage. Threshold voltages of approximately −7 and 8 V for the PMOS and NMOS devices, respectively, were observed. Limited I_{on}/I_{off} ratios of 10^3 were obtained as a result of charge carrier scattering from the rough channels due to laser ablation and outgassing. The output characteristics of both the devices show low contact resistances, and a parasitic resistance for device operation in the saturation regime. A summary of the device performance is shown in Table 1.

DISCUSSION

We have demonstrated poly-Si transistors created directly on top of a paper substrate employing a silicon ink. We have successfully surpassed printed organic devices and are competing with printed indium–gallium–zinc-oxide (IGZO) TFTs. The issue with IGZO however, is the absence of a strong p-type counterpart,[22] and their inclusion of In as one of the elements, which is a rare and expensive material.[23] For the devices fabricated in this work, there is still room for optimization to improve the silicon device performance. Two key elements require special attention. The first is the possible effect of paper contaminating the silicon channel. Since no barrier layer was formed on top of the coated paper, prior to the silicon ink coating, and due to the excimer laser crystallization, it is plausible that contaminants from the coating may enter the silicon channel disrupting the electronic device operation. In general, contamination would need to be limited during the process, since no chemical cleaning treatment can be applied, unlike in fabrication processes for conventional devices. The second element would be to further limit the maximum processing temperature, since the paper substrate is prone to expansion, which leads to alignment errors as well as stresses in the devices.

As a proof of concept, besides the silicon islands, vacuum-based processes have been used in this work; however, solution-based alternatives can potentially be used. For the gate insulator a viable solution-based option is still necessary; however, atomic layer deposition (ALD) systems have shown to be applicable in roll-to-roll processing systems.[24] Additionally, the methods developed in this work could also be applied on low-cost polymer substrates. This work presents an important milestone in terms of solution-based silicon electronics, paving a way toward reliable, low power, extreme low cost, flexible, and disposable electronics.

Table 1. TFT properties of silicon ink-based PMOS and NMOS TFT fabricated on top of a paper substrate

	PMOS	NMOS
μ_{FE} (cm^2/V s)	6.2	2.0
V_{th} (V)	−7.3	7.8
S (mV/dec)	27	600
Leakage (A)	10^{-9}	10^{-13}
Log (I_{on}/I_{off})	~3	~3

METHODS

Shadow masks

Two types of shadow masks were used in the fabrication process of the TFT on paper, one for the local crystallization of polysilane, and one for the metallic contact deposition. For the local crystallization, a 4″ quartz wafer was used with a thickness of 700 µm. A thickness of 100 nm of 99% Al with 1% Si was created by physical vapor deposition (PVD) on top of the substrate at 50 °C. Island patterns were created by etching the metallic film after patterning by photolithography. A combination of phosphoric, nitric, and acetic acid (PES-77) was used to chemically etch the Al film followed by a 5 min rinse in demineralized water. The mask is cleaned at 40 °C with acetone for 1 min, with 99% HNO_3 at room temperature for 10 min, and a final rinsing step with demineralized water for 5 min. For the shadow mask used for metal evaporation, a 4″, 550 µm thick silicon wafer is used as the starting substrate. Four micrometers thick 99% Al with 1% Si was created by PVD on the backside of the wafer, and 6 µm thick SiO_2 was created on the front side by plasma-enhanced chemical vapor deposition (PECVD) of tetraethyl orthosilicate. The oxide layer forms a hard mask for the following deep reactive ion-etching (DRIE) process. The oxide was patterned by photolithography and dry etching. Using a large over-etching time, the patterns through the silicon wafer were created, regardless of the sidewalls. The polymer deposited in the DRIE process was removed by 30 min of oxygen plasma treatment at 1000 W. The backside aluminum was removed by 30 min of PES-77, wet-chemical etching. Finally, the wafer was cleaned in 99% HNO_3 for 10 min followed by a 5 min rinse.

Thin-film transistors

The paper substrate (Powercoat®HD, Arjowiggins Creative Papers) was taped on a 4″ Si wafer using carbon tape. Inside a glovebox (MBraun, N_2), the paper is coated with 12.5 µL of pure CPS with a doctor blade, while at the same time being cured with a 10 mW/cm^2 UV light source (UV AHAND GS). Once the film stays stable for a few seconds, it is rapidly solidified by a UV light (Flood UV curing system, Loctite) with 300 mW/cm^2 intensity for 30 s. The film is subsequently further cured with the intensity of 10 mW/cm^2 for 30 min to ensure solidification throughout the thickness of the film. The lower intensity light source is chosen since it also irradiates heat and allows a larger fraction of the film to be polymerized while the degree of cross-linking is limited. In the case of high-intensity UV light, the degree of cross-linking would be so severe that the film will start to change color and behave like a semiconductor instead of an insulator. A quartz shadow mask is placed, metal side down, onto the sample and is fixed by a tape. A KrF excimer laser (248 nm, 20 ns) is used to crystallize the polysilane islands while leaving the parts covered by metal untreated. Laser fluences ranging from 40 to 100 mJ/cm^2 and numbers of pulses ranging from 1 to 100 are used. The sample is then exposed to open air for 1 day to allow the untreated polysilane to oxidize. A gate oxide of 100 nm thick SiO_2 is deposited by radio frequency plasma enhanced chemical vapor deposition (RF-PECVD) (AMIGO, Elettrorava) at 120 °C radiative heating. Compared to other low temperature alternative processes such as ALD, the RF-PECVD oxide performed best as shown in the Supplementary Information. The temperature experienced by the wafer in this process is ~100 °C. A through-wafer etched shadow mask was aligned by hand with an optical microscope for monitoring alignment markers. The mask was attached to the silicon carrier wafer of the paper sample by melting a wax (Crystalbond™ 590, Ted Pella. Inc.) locally around the edges of the wafers with a soldering iron. The 500 nm thick Al gate metal was deposited by evaporation. The temperature reached by the wafer is ~60 °C. The mask is subsequently removed by elevating the temperature of the edges to ~100 °C. Wax residues are removed by manual wiping with methanol. Ion implantation was used to dope the source and drain regions of the poly-Si channel. The gate metal blocks dopant ions from entering the channel directly underneath the gate, resulting in a self-aligning process. Boron ions were used to implant at an energy of 30 keV, with a dose of $3.0 \cdot 10^{15}$ ions/cm^2 for p-type devices. Phosphorus ions were used to implant at an energy of 10 keV with a dose of $5.0 \cdot 10^{15}$ ions/cm^2 for n-type devices. Prior to the implantation of the phosphorus ions, oxide was removed by a blanket plasma-etching step. This allowed the reduction in ion implantation energy. Dopants were activated by the same KrF excimer laser as used for the crystallization process. The same range of fluences and numbers of pulses were used. A second through-wafer etched shadow mask was aligned and attached to the carrier wafer by the wax. This time, patterns expose contact locations, and a dry etching process was employed to remove the oxide at the specific locations. Immediately after this etching process, 500 nm Al contact metal was deposited by evaporation without removing the mask, allowing the metal to reach the silicon channel in the exact locations where the oxide was removed. Finally, the shadow mask is removed and the paper may be peeled off the carrier wafer.

Material and device characterization

In order to assess the crystallinity of the excimer laser-annealed polysilane samples, Raman spectroscopy (Renishaw InVia, 514 nm) was employed. Additionally a change in color from transparent to light brown reveals the change in material bandgap, giving an indication of the transformation process. The process was repeated over at least 20 samples, with each sample exposed to various excimer laser treatments on predefined locations. The reproducibility of the results depended on the condition of the laser, the substrate, and the starting material in terms of thickness, curing, and aging. For this work, stated results met our assumptions and were the most reproducible with a standard deviation in the optimized crystallization laser fluence of ~10 mJ/cm^2, and hence chosen for further analysis. For electrical measurements, a semiconductor parameter analyzer (HP4156) was used under ambient conditions. Since this work was aiming for a proof of concept, sacrificial design structures were used due to a large misalignment between layers due to the shadow masks being aligned manually. Therefore, a limited number of devices within a sample were operational. Statistical conclusions could therefore not be taken from these results alone. Therefore, in order to assess the potential of these devices, the best-performing ones were chosen and are still subject to further process optimization.

Data availability statement

The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

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AUTHOR CONTRIBUTIONS

M.T. and P.M.S. characterized and synthesized the materials, designed, fabricated, and characterized the transistors, and prepared the figures. T.S. advised on material usage. M.T. wrote the manuscript with comments from all authors. R.I. supervised the project.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj Flexible Electronics* website (https://doi.org/10.1038/s41528-017-0013-x).

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REFERENCES

1. Tobjörk, D. & Österbacka, R. Paper electronics. *Adv. Mater.* **23**, 1935–1961 (2011)..
2. Ahmed, S., Bui, M. P. N. & Abbas, A. Paper-based chemical and biological sensors: engineering aspects. *Biosens. Bioelectron.* **77**, 249–263 (2016).

3. Xia, Y., Si, J. & Li, Z. Fabrication techniques for microfluidic paper-based analytical devices and their applications for biological testing: a review. *Biosens. Bioelectron.* **77**, 774–789 (2016).
4. Kim, D. H. et al. Ultrathin silicon circuits with strain-isolation layers and mesh layouts for high-performance electronics on fabric, vinyl, leather, and paper. *Adv. Mater.* **21**, 3703–3707 (2009).
5. Zschieschang, U. et al. Organic electronics on banknotes. *Adv. Mater.* **23**, 654–658 (2011).
6. Martins, R. F. et al. Recyclable, flexible, low-power oxide electronics. *Adv. Funct. Mater.* **23**, 2153–2161 (2013).
7. Mitzi, D. B. (ed) *Solution Processing of Inorganic Materials* (John Wiley & Sons, 2009).
8. Berggren, M., Nilsson, D. & Robinson, N. D. Organic materials for printed electronics. *Nat. Mater.* **6**, 3–5 (2007).
9. Perelaer, J. et al. Printed electronics: the challenges involved in printing devices, interconnects, and contacts based on inorganic materials. *J. Mater. Chem.* **20**, 8446–8453 (2010).
10. Sirringhaus, H. Reliability of organic field-effect transistors. *Adv. Mater.* **21**, 3859–3873 (2009).
11. Jeong, J. K. The status and perspectives of metal oxide thin-film transitors for active matrix flexible displays. *Semicond. Sci. Technol*. **26**, 1–10 (2011).
12. Shimoda, T. et al. Solution-processed silicon films and transistors. *Nature* **440**, 783–786 (2006).
13. Zardetto, V., Brown, T. M., Reale, A. & Di Carlo, A. Substrates for flexible electronics: a practical investigation on the electrical, film flexibility, optical, temperature, and solvent resistance properties. *J. Polym. Sci. Part B* **49**, 638–648 (2011).
14. Trifunovic, M., Shimoda, T. & Ishihara, R. Solution-processed polycrystalline silicon on paper. *Appl. Phys. Lett.* **106**, 163502 (2015).
15. Trifunovic, M., Sberna, P. M., Shimoda, T. & Ishihara, R. Polycrystalline silicon TFTs on a paper substrate using solution-processed silicon. In *IEEE International Electron Devices Meeting (IEDM)* 32–33 (IEEE: San Francisco, CA, USA, 2016).
16. Sugiyama, A., Shimoda, T. & Chi, D. H. Ab initio study of the polymerization of cyclopentasilane. *Mol. Phys.* **108**, 1649–1653 (2010).
17. Masuda, T., Matsuki, Y. & Shimoda, T. Stability of polydihydrosilane liquid films on solid substrates. *Thin Solid Films* **520**, 5091–5096 (2012).
18. Garino, T. J. The cracking of sol-gel films during drying. *MRS Proc.* **180**, 497–502 (1990).
19. Okamoto, K., Shinohara, M., Yamanashi, T., Miyazaki, S. & Hirose, M. Laser-induced hydrogen desorption from polysilane and its application to silicon pattern generation. *Appl. Surf. Sci.* **79**, 57–61 (1994).
20. Masuda, T., Matsuki, Y. & Shimoda, T. Pyrolytic transformation from polydihydrosilane to hydrogenated amorpohous silicon film. *Thin Solid Films* **520**, 6603–6607 (2012).
21. Yu, R. et al. Impact ionization induced dynamic floating body effect in junctionless transistors. *Solid-State Electron.* **90**, 28–33 (2013).
22. Pattanasattayavong, P., Thomas, S., Adamopoulos, G., McLachlan, M. A. & Anthopoulos, T. D. p-channel thin film transistors based on spray-coated Cu2O films. *Appl. Phys. Lett.* **102**, 163505 (2013).
23. Davies, E. Endangered elements. *Chem. World* 50–54 (2011).
24. Maydannik, P. S., Kääriäinen, T. O. & Cameron, D. C. An atomic layer deposition process for moving flexible substrates. *Chem. Eng. J.* **171**, 345–349 (2011).

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