SCIENCE CHINA Materials ARTICLES

mater.scichina.com link.springer.com Published online 26 December 2018 | https://doi.org/10.1007/s40843-018-9380-8
Sci China Mater 2019, 62(6): 803–812

Solution-processed amorphous gallium-tin oxide thin film for low-voltage, high-performance transistors

Jinhua Ren, Kaiwen Li, Jianwen Yang, Dong Lin, Haoqing Kang, Jingjing Shao, Ruofan Fu and Qun Zhang*

ABSTRACT Gallium-tin oxide (GTO) semiconductor thin films were prepared by spin-coating with 2-methoxyethanol as the solvent. Their crystal structures, optical transparency, chemical states and surface morphologies, along with the electrical properties, were dependent on Ga contents and annealing temperatures. The optimized GTO channel layer was applied in the high-*k* Al_2O_3 thin film transistor (TFT) with a low operation voltage of 2 V, a maximum field-effect mobility of 69 $cm^2 V^{-1} s^{-1}$, a subthreshold swing (SS) of 76 mV dec^{-1}, a threshold voltage of 0.67 V and an on-off current ratio of $1.8×10^7$. The solution-processed amorphous-GTO-TFTs would promote the development of low-consumption, low-cost and high performance In-free TFT devices.

Keywords: GTO semiconductor films, thin-film transistor, stability, Al_2O_3 dielectric

INTRODUCTION

Amorphous oxide semiconductors (AOS) are achieving attention over amorphous silicon and low-temperature polycrystalline silicon (LTPS) recently [1]. In_2O_3, ZnO and SnO_2 based semiconductors are promising candidates for information displays [2–4]. Particularly, mass production of amorphous-InGaZnO (a-IGZO) panel has been realized. However, In is a rare element (0.25 ppm) in the earth's upper continental crust, prompting researchers to exploit In-free materials [5]. As for Zn-Sn-O (ZTO) [6] and ZnON [7], weak Zn–O bonds in their lattice lead to instable thin film transistor (TFT) devices [8]. Hence, SnO_2 based semiconductors are emerging as promising channel materials. In the SnO_2-based channels, Sn^{4+} with a $4d^{10}5s^0$ electronic configuration can contribute to the high mobility, which is similar to the 5s orbital of In^{3+} (IGZO) [9]. In^{3+} may be replaced by Sn^{4+} in TFTs to avoid high fabrication cost. In the last few years, Yang *et al.* [10–12] prepared high performance SnO_2-based TFTs by radio-frequency (RF) magnetron sputtering. It is well known that ion bombardment and incorporation results in a large number of defects in the films [13]. In addition, in the sputtering process, multi-metal thin film probably has different composition from the target due to preferential sputtering, especially for IGZO [14]. Therefore, more researchers are turning to solution process method for realizing low-cost electronics. Recent reports [15,16] showed solution processed SnO_2 TFTs have better performance than vacuum based devices. Pure SnO_2 films tend to crystallize, which does not lead to the uniformity for TFT devices. Besides, high carrier concentration in pure SnO_2 also affects the electrical performance of devices, such as stability and current on-off ratio (I_{on}/I_{off}). From the periodic table of elements, it can be found that the similar ion radius of Ga (0.62 Å) and Sn (0.69 Å) may reduce structural defects in the Ga-doped SnO_2 system. In the previous reports [17,18], Ga is an oxygen vacancy inhibitor and can weaken the crystallinity of films. Recently, Matsuda *et al.* [19] reported RF magnetron sputtered a-GaSnO (GTO)-TFTs with high mobility of 25.6 $cm^2 V^{-1} s^{-1}$ at 350°C. Zhang *et al.* [20] reported nanocrystalline Ga-rich GTO-TFTs with mobility of 1.03 $cm^2 V^{-1} s^{-1}$ at 900°C. The high annealing temperature is not compatible with high-*k* dielectric and flexible substrates.

In this paper, solution-processed a-GTO-TFTs with various Ga content and under different annealing temperatures are investigated. The stability of the optimum device is evaluated. Based on these results, a-GTO-TFTs with Al_2O_3 high-*k* dielectric layer show high mobility and low operation voltage.

Department of Materials Science, National Engineering Laboratory for TFT-LCD Materials and Technologies, Fudan University, Shanghai 200433, China
* Corresponding author (email: zhangqun@fudan.edu.cn)

 © Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

EXPERIMENTAL SECTION

Precursor solution preparation

0.1 mol L^{-1} $SnCl_2·2H_2O$ (Aladdin, 99.99%) and various amounts of $Ga(NO_3)_3·xH_2O$ (Aladdin, 99.9%) (Ga:Sn = 0, 10, 20, 50 at.%) were dissolved in 10 mL 2-methoxyethanol successively in sealed reagent bottles. Then, they were stirred by a magnetic stirrer at room temperature for 2 h in ambient. For Al_2O_3 dielectric, 0.3 mol L^{-1} $Al(NO_3)_3·9H_2O$ (Aladdin, 99.99%) was dissolved in 5 mL 2-methoxyethanol and then stirred at room temperature for 3 h.

Thin film and device fabrication

For GTO-SiO_2 device, p-Si with 270 nm thermally grown SiO_2 was cleaned by acetone, ethyl alcohol and deionized water successively. Then the surface of SiO_2 was treated by oxygen plasma to improve the adhesive strength of GTO solution. The above GTO solutions were filtered through 0.22 μm PTFE filter and then spin-coated onto the SiO_2 substrate with the rotation speed of 3,500 rpm for 30 s. The sol films were then baked on a hot plate to be preheated at 150°C for 10 min to evaporate the solvent. The resulting gel films were annealed in a tube furnace at 300, 350 and 400°C for 1 h in air. Finally, ITO source/drain (S/D) electrode arrays (W/L=450 μm/80 μm, W and L is width and length of electrodes) were deposited by RF magnetron sputtering. For GTO-Al_2O_3 device, p-Si wafers were ultrasonically cleaned by 2% HF aqueous solution, water, acetone and ethyl alcohol. Similarly, they were bombarded with oxygen plasma to improve hydrophilicity. The prepared Al^{3+} solution was also filtered through 0.22 μm PTFE filter and spun onto the Si wafers. Then, it was pre-annealed on a hotplate at 220°C for 10 min. The samples were then cured under ultraviolet lamp for 10 min to promote the crosslinking reactions in the gel film. Taking the annealing temperature of active layers into account, the cured Al_2O_3 gel films were then annealed at 450°C in air for 30 min. The fabrication method of channel layers is similar to the GTO-SiO_2 device. The entire device was completed after the deposition of ITO electrodes. In the meantime, the GTO films were also spin-coated on a glass substrate under the same condition.

Thin film and device characterization

The thermal behavior of GTO and Al_2O_3 precursor solutions was monitored in ambient air using a thermal gravimetric (TGA, TA Q500) with a heating rate of 10°C min^{-1}. The film thicknesses were measured *via* a stylus profiler (Kosaka Laboratory ET3000). The device structure was observed by a field-emission scanning electron microscope (FE-SEM-4800-1) in sectional view. The surface information of thin films was detected by energy disperse spectroscopy (EDS) attachment. X-ray diffraction (XRD, Bruker D8 Advanced and Da Vinci Design system) was used to characterize the crystal structure of thin films. Optical transmittance of GTO films was obtained from ultraviolet-visible (UV, Shimadzu, UV2400) spectrophotometer. X-ray photoelectron spectroscopy (XPS, ThermoFischer, ESCALAB 250Xi) was used to analyze the chemical components and oxidation states of the surfaces of GTO channels. The surface morphologies of active layer were examined by an atomic force microscope (AFM, Dimension Edge, Bruker). The capacitance per unit area of Al_2O_3 dielectric layer was measured with a WK6515B precision impedance analyzer. I–V, transfer and output characteristic curves of GTO-TFTs were measured by a Keithley 4200 semiconductor parameter analyzer.

RESULTS AND DISCUSSION

Fig. 1a shows the TGA curves of Al_2O_3 and 20 at.% GTO gels where the initial weight loss below 130°C is due to the evaporation of 2-methoxyethanol (gray region). The gradual weight loss up to 400°C for Al_2O_3 gel is ascribed to the evaporation of the bound water and the decomposition of nitrate groups (yellow region) [21]. For GTO gel, condensation process gradually leads to a network of Ga–Sn–O bonds with increasing temperature (yellow region) [20]. The faster mass loss for Al_2O_3 gel may originate from the lower Al^{3+} weight ratio in the Al_2O_3 precursor solution (7.2 wt.%) than that of GTO solution (52.6 wt.% for Sn^{4+}, 27.3 wt.% for Ga^{3+}). Fig. 1b shows the XRD patterns of GTO thin films on glass substrates annealed at 350°C with Ga content from 0 to 50 at.%. The pure SnO_2 film shows a weak peak at 2θ=37.9°, representing (200) crystal planes of cassiterite SnO_2 (JCPDS No. 41-1445) [22]. The poor crystallinity may be due to a low temperature. It is reported that SnO_2 films present obvious polycrystalline peaks at the temperature above 350°C [16]. However, the unobvious peak after doping 10 at.% Ga indicates that Ga can inhibit the crystallization of SnO_2 lattice. As the Ga content increases to 20 and 50 at.%, GTO thin film becomes amorphous. The degradation of SnO_2 thin film crystallinity may derive from the induced stress and the distortion of structures [18]. Due to ionic radius difference, Ga^{3+} may occupy Sn^{4+} sites in GTO films. Optical spectra of GTO films demonstrate the transmit-

 © Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

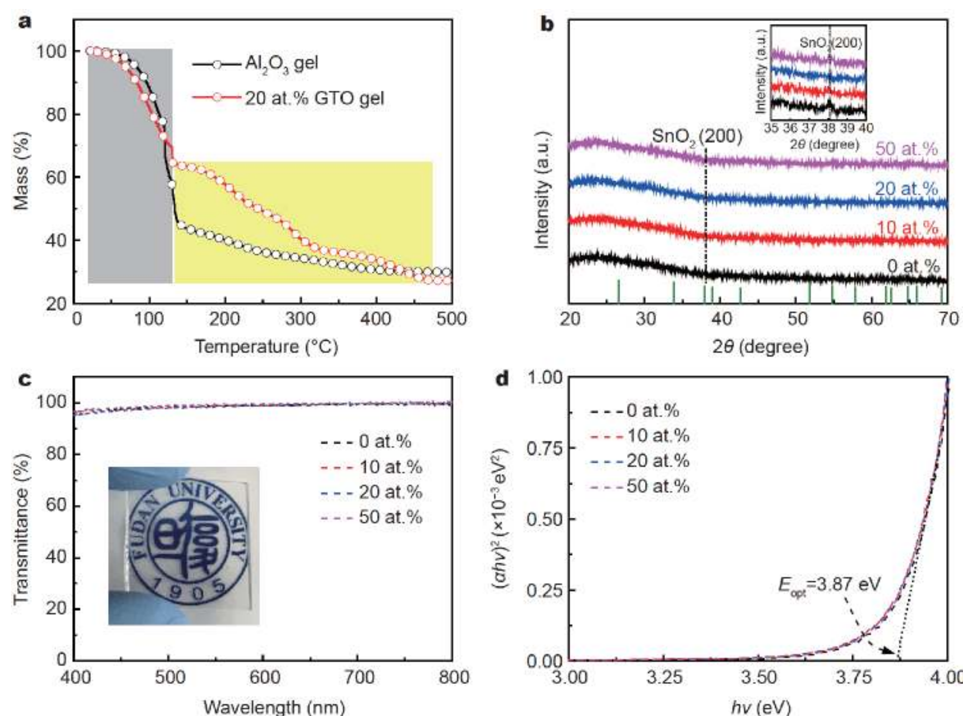

Figure 1 (a) TGA curves of Al_2O_3 and 20 at.% GTO gels, (b) XRD patterns of GTO thin films, (c) optical transmittance of a-GTO thin films (inset: the photograph of 20 at.% GTO thin film), (d) Tauc plots of a-GTO thin films.

tance more than 95% from 400 to 700 nm (Fig. 1c). The optical bandgap (E_g) of GTO films, calculated from the formula: $(\alpha h\nu)^2=A(h\nu-E_g)$, where α is absorption coefficient, is around 3.87 eV. This value is larger than that of IGZO films (3.17–3.38 eV), indicating their excellent optical performance [23]. We do not observe the obvious red shift of bandgap after Ga incorporation which is consistent with a previous report [17].

The concentration of oxygen defects plays an important role in determining the carrier concentration of oxide semiconductor thin films, and thus affects the electrical performance of TFTs including mobility (μ) and threshold voltage (V_{th}). Hence, XPS measurements were conducted to reveal the chemical information of GTO channels, as depicted in Fig. 2. The binding energies (BE) of all elements were calibrated with reference to the C 1s line at 284.6 eV for charge shift effect. In Fig. 2a, O 1s peaks were deconvoluted into three sub-peaks at 530.4 eV (M–O–M lattice oxygen, O_I), 531.3 eV (oxygen defects, O_{II}) and 532.3 eV (adsorbed oxygen: O_2, OH species, O_{III}) respectively [24,25]. It has been calculated that the atomic ratios of O_{II} component ($O_{II}/(O_I+O_{II}+O_{III})$) are 24.5%, 33.7%, 41.6%, 36% and 15.1% for the samples annealed at 300°C, 350°C, 400°C (20 at.% Ga) and the samples doped with 0, 50 at.% Ga (350°C annealing temperature). Oxygen defects related to carrier concentration can be modulated by altering annealing temperatures and doping contents. The O_{III} component decreases from 22.5% to 10.9% when the temperature increases from 300 to 400°C. OH-related species become heavily oxidized at high temperature in accordance with the TGA results. O_I component slightly decreases (53% to 47.5%) as the temperature increases, leading to the loss of metal atoms during the high temperature treatment [26]. It is well known that the adequate amount of carriers in the channel layer is beneficial to the off-operation mode of normal TFTs. Nevertheless, excess carriers will make channels difficult to be depleted [27]. Consequently, the excess electrons in the conductive SnO_2 thin film must be inhibited to achieve the enhancement-mode TFT device. The Sn 3d peaks at 486.4 (Sn $3d_{5/2}$) and 494.8 eV (Sn $3d_{3/2}$) [20] do not obviously shift after Ga incorporation, indicating the oxidation state of Sn element is not affected evidently, as shown in Fig. 2b. The shift of ~0.3 eV to higher BE of Sn 3d shows more metal bonds in 50 at.% GTO film as evidenced in O 1s peak. The BE range for Sn^{4+} ions is 486–487.1 eV [28]. From Fig. 2c, Ga 3d peaks are located at 20.2 eV [20]. The Ga and Sn orbital peaks in the full spectra (Fig. S1) indicate the successful fabrication of GTO thin films lays the foundation for

 © Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

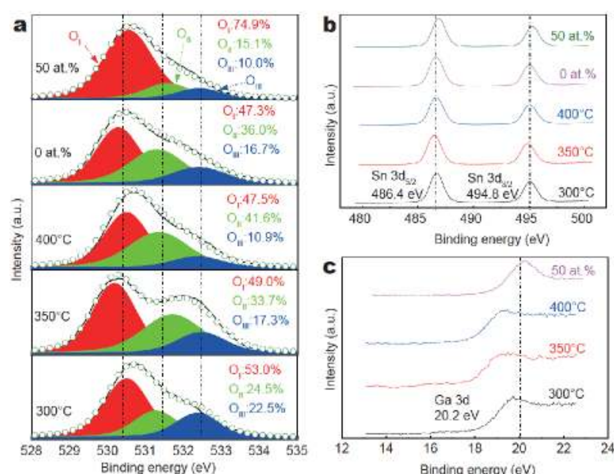

Figure 2 (a) O 1s XPS fine spectra of GTO channels under different annealing temperatures (300, 350 and 400°C at 20 at.% Ga) and doping contents (0 and 50 at.% Ga at 350°C), (b) XPS spectra of Sn 3d region, (c) XPS spectra of Ga 3d region.

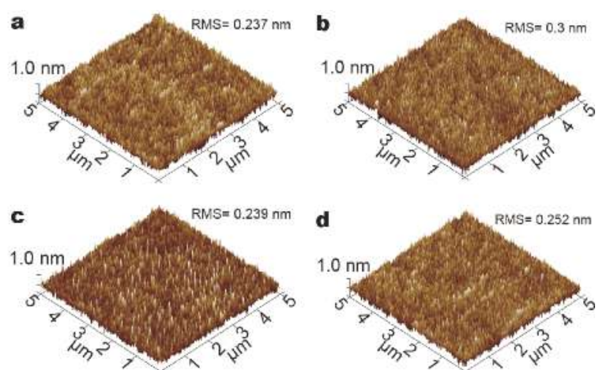

Figure 3 AFM morphologies of GTO channels with Ga content at (a) 0, (b) 10, (c) 20, (d) 50 at.%.

the subsequent fabrication of TFT devices.

AFM images of GTO channels are shown in Fig. 3. No evident grain accumulation on GTO channels may be responsible for the weak crystallization or amorphous state. The root-mean-square (RMS) roughness of 0.237, 0.300, 0.239 and 0.252 nm for the samples with 0, 10, 20 and 50 at.% Ga, respectively, indicates that Ga doping exerts no obvious effects on the surface undulation. It is well known that low RMS roughness reduces carrier scattering and ensures the high performance of TFTs [29]. This may be due to the small radius difference between Ga^{3+} and Sn^{4+}.

Based on above results, bottom-gate top-contact TFTs were fabricated with GTO thin films. The top view of channels is shown in Fig. 4a. Fig. 4b shows the FE-SEM cross sectional image of the 20 at.% GTO-TFT. The thicknesses of GTO layer and ITO electrode are about 35 and 50 nm, respectively. The corresponding EDS pattern of the thin film indicates the uniformity of elements distribution (Fig. S2). I–V curves were carried out to test the electrical contact properties of GTO-TFTs with different Ga contents (Fig. 4c, inset: test schematic). Linear dependence in positive and negative bias voltage ranges demonstrates the low-resistance contact between ITO electrodes and GTO thin films, which indicates ohmic contacts [30]. The typical transfer curves of samples with different annealing temperatures and Ga doping contents are shown in Fig. 4d and 4e. The detailed device parameters calculated from transfer characteristic curves are shown in Table 1. The field effect mobility (μ_{FE}) is calculated from $\mu_{FE}=(dI_D/dV_G)/(C_iWV_D/L)$ at low V_D [31] (Fig. S3). From Fig. 4d, it can be seen that GTO devices with superior performance can be formed at 350°C. Nevertheless, low annealing temperature will lead to poor mobility and large SS. It is reported that the degree of oxygen defects generation is dependent on the annealing temperature which affects the electron concentration in channels, which has been elucidated by XPS results [32]. It is reported that electron transport in AOS semiconductors is predominant by hopping percolation mechanism and accelerated with increasing electron concentration [33,34]. Although the GTO3-TFT (Table 1) has higher mobility than those annealed at lower temperature, its SS deteriorates and V_{th} shifts to the more negative values, leading to high energy consumption. From Fig. 4e, as Ga doping content increases from 0 to 20 at.%, the off-state current decreases from 3×10^{-5} to 4×10^{-11} A, which demonstrates that Ga element acts as the carrier inhibitor in the GTO system. It is also known that a larger metal ion electronegativity (χ_z) difference will control the oxygen defects more effectively [35]. The electronegativity difference of Ga(3+) (1.756) and O (3.61) is slightly more than that of Sn(4+) (1.824) and O, leading to carrier suppression effect [36]. It is worth noting that Shin *et al.* [37] also observed the charge carrier suppression effect in GTO-TFTs fabricated *via* co-sputtering method. Nevertheless, oxygen chemical states are unknown in channel layers. When Ga content increases to 50 at.%, the mobility degrades seriously as I_{on} decreases and V_{th} also shifts more positively. From above results, the appropriate doping level in our experimental conditions is 20 at.%. The μ_{FE}, SS, V_{th} and I_{on}/I_{off} are 6.8 $cm^2 V^{-1} s^{-1}$, 0.9 V dec^{-1}, 0.7 V and 2.1×10^6, respectively, in enhancement mode, demonstrating the reliability of these solution-processed GTO channels in the fabrication of TFTs on SiO_2 substrates. Fig. 4f shows

 © Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

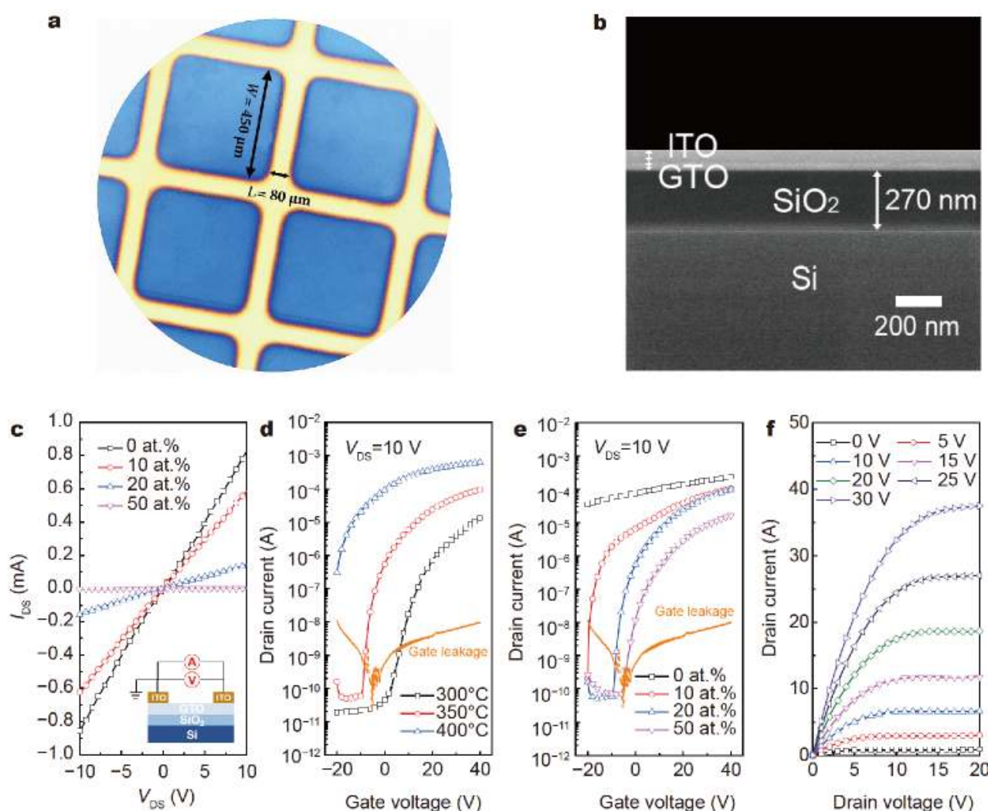

Figure 4 (a) The top view of GTO-TFT channels, (b) FE-SEM cross sectional view of the 20 at.% GTO-TFT, (c) *I*–*V* curves of GTO channels with different Ga contents, (d) transfer curves of GTO-TFTs under different annealing temperatures, (e) transfer curves of GTO-TFTs with different Ga doping contents, (f) output curves for the GTO-TFT with Ga content of 20 at.%. All of TFTs are swept with the gate voltage from −20 to 40 V at V_{DS}=10 V.

Table 1 Fundamental parameters and performance of GTO-SiO_2 and GTO-Al_2O_3 devices

Sample	Doping content (at.%)	Temperature (°C)	μ_{FE} (cm^2 V^{-1} s^{-1})	SS (V dec^{-1})	V_{th} (V)	$I_{on/off}$
GTO1	20	300	1.2–1.7	2.1–2.3	7.0–8.7	5.0×10^4–4.6×10^5
GTO2	20	350	6.8±0.4	0.9±0.4	0.7±0.6	$(1.0–2.1)\times10^6$
GTO3	20	400	8.7–9.6	1.6–1.9	<−20	$\sim10^2$–2.0×10^3
GTO4	0	350	11.8	28.7	<−20	$\sim10^1$
GTO5	10	350	9.2–9.9	0.3–1.0	−13–−9.2	5.0×10^4–5.2×10^5
GTO6	20	350	6.8±0.4	0.9±0.4	0.7±0.6	$(1.0–2.1)\times10^6$
GTO7	50	350	0.9–1.5	1.3–2.0	5.8–7.0	2.5×10^5–1.7×10^6
GTO-Al_2O_3	20	350	69	0.076	0.67	1.8×107

the typical output characteristic curves of the optimized TFT (GTO6, see Table 1) which exhibits the hard saturation at V_D=20 V.

To our knowledge, there are almost no reports about the stability of solution processed SnO_2 based TFTs. The stabilities of TFTs are crucial to the application of display backplanes such as AMLCDs and AMOLEDs. Fig. 5a shows clockwise hysteresis characteristic of GTO6-TFT at V_{DS}=1 and 10 V. The hysteresis voltage shift is about 9.2 V at V_{DS}=100 nA. Positive bias stress (PBS) and negative bias stress (NBS) tests were carried out at bias voltages of +20 V and −20 V for 1,200 s (Fig. 5b and 5c). In the PBS test, the V_{th} positively shifts by ~6.6 V which is larger than that of sputtered GTO-TFTs under the same stress time [19]. We can observe a slightly decreased SS with the extension of time because more interface states

 © Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

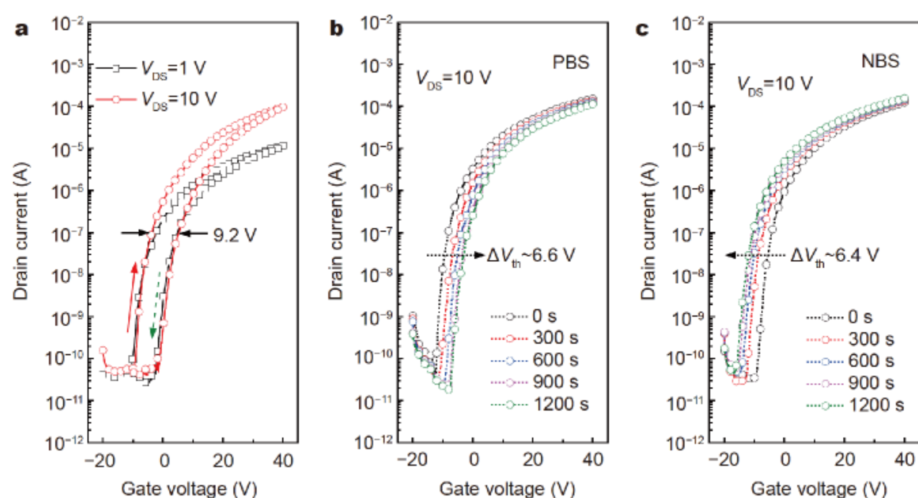

Figure 5 (a) Hysteresis characteristic of 20 at.% GTO-SiO_2-TFT, (b) PBS test, (c) NBS test.

are filled during PBS process [38]. On the other hand, it is reported that the electric field applied in the channel layer can result in the adsorption of O_2 (acceptor) and desorption of adsorbed H_2O (donor) which can reduce electrons in the channel layer [39]. Both mechanisms can contribute to the positive V_{th} shift. Besides, the V_{th} negatively shifts by ~6.4 V under NBS after the device is stressed 1,200 s, which can be explained by the H_2O adsorption mechanism [40]. In this case, the mechanism can be expressed by $H_2O+h^+=H_2O^+$ where h^+ and H_2O^+ are holes in the channel layer and water molecules positively charged on the back surface of channel layer. Although GTO-TFTs have been fabricated by solution process on SiO_2 substrates successfully, they are confronted with many challenges such as low mobility, high SS and instability, making them insufficient to be put into practice.

In order to improve the a-GTO-TFT performance, SiO_2 was replaced by Al_2O_3 thin film as the dielectric layer. XRD pattern of Al_2O_3 thin film exhibits its amorphous state (Fig. 6a). The RMS roughness of 0.16 nm in the area of 5×5 μm^2 can be derived from the AFM image of Al_2O_3 thin film. The leakage property of Al_2O_3 thin film with the thickness of ~30 nm is shown in Fig. 6b. It can be obtained that the breakdown field strength of ~4.4 MV cm^{-1} ensures the reliability of Al_2O_3 dielectric. It is acknowledged that electrical double layer formed in the solution-processed metal oxide gate dielectrics will lead to higher capacitance [41,42], as shown in the inset of Fig. 6b. Because TFTs were measured in direct voltage, the capacitance per unit area of 257 nF cm^{-2} linearly extrapolated to 1 Hz (not the actual value) was adopted for mobility calculation to avoid the overestimation [43]. Based on these results, the relative dielectric constant (ε_r) of Al_2O_3 thin film, calculated from $\varepsilon_r=C_{ox}d/\varepsilon_0$ where d is the thickness, C_{ox} the capacitance per unit area, ε_0 the vacuum dielectric constant, is about 8.7. This value is lower than the theoretical value of 9 due to the holes in Al_2O_3 dielectric layer. Branquinho *et al.* [44] also observed the similar phenomenon in the aqueous combustion synthesis of Al_2O_3 thin film.

The typical transfer characteristic curves of a-GTO-Al_2O_3 TFT with the gate voltage swept from −1 to 2 V (Fig. 6c) exhibit excellent performance such as a maximum field-effect mobility of 69 cm^2 V^{-1} s^{-1}, a low SS of 76 mV dec^{-1}, V_{th} of 0.67 V, I_{on}/I_{off} of 1.8×10^7, low hysteresis voltage shift of 0.12 V and low operation voltage of 2 V. The gate leakage current at V_{DS}=2 V of ~1.1×10^{-8} A demonstrates the reliability of these Al_2O_3 dielectrics. The histograms (Fig. S4) of the μ_{FE} (~69±10 cm^2 V^{-1} s^{-1}, ~65±15 cm^2 V^{-1} s^{-1}) and V_{th} (0.62±0.3 V, 0.71±0.3 V) for two batches of GTO-TFT arrays demonstrate the device fabrication are reproducible. In particular, the low SS closing to the room-temperature limit, 60 mV dec^{-1}, is attributed to the high quality interface [45]. The concentration of total interfacial trap states at the GTO/Al_2O_3 interface calculated from $N_t=[SS\log(e)/(kT/q)-1]C_{ox}/q$ is about 4.01×10^{11} cm^{-2} smaller than that of the aqueous IWO/Al_2O_3 interface (4.4×10^{11} cm^{-2}) [46,47]. This may be attributed to the higher viscosity of 2-methoxyethanol than that of water which will form more compact sol films under the strong centrifugal force. It is worth notiing that the hysteresis property of our GTO-TFT is

 © Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

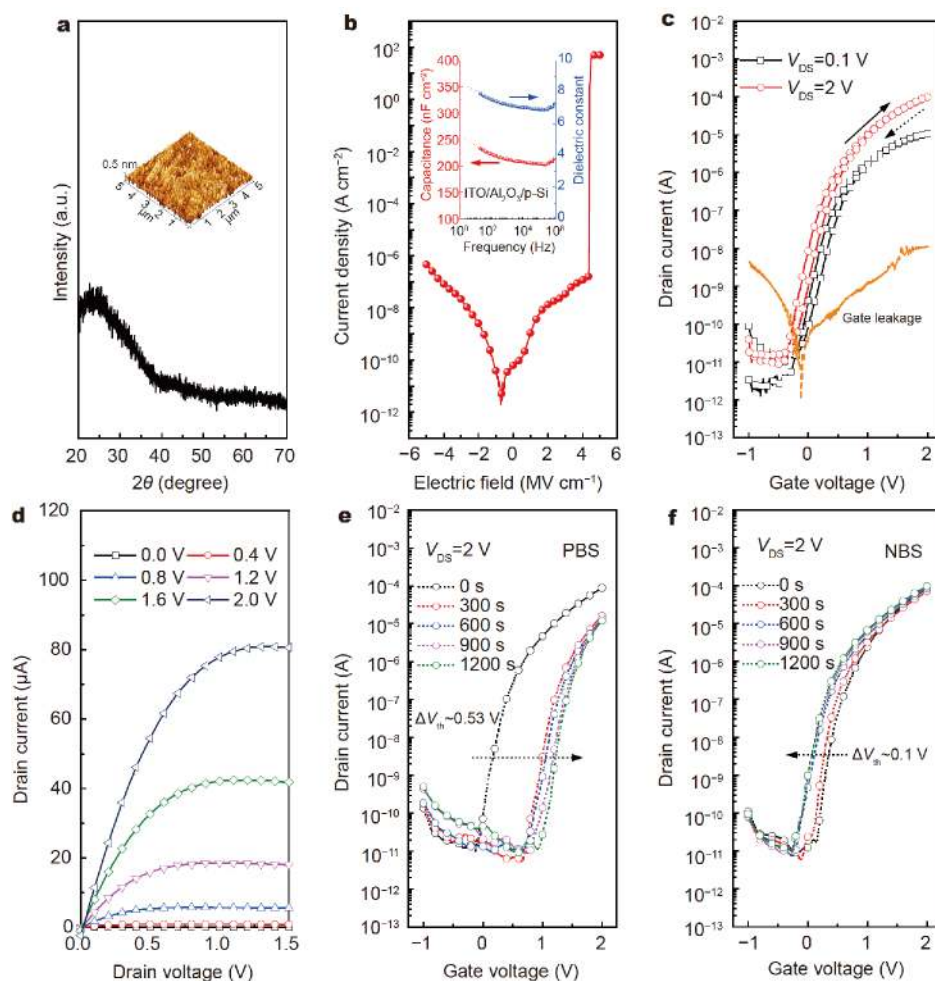

Figure 6 (a) XRD pattern of Al_2O_3 dielectric layer (inset: AFM surface morphology), (b) the breakdown of Al_2O_3 (inset: capacitance and dielectric constant), (c) transfer curves of GTO-Al_2O_3 device, (d) output curves of GTO-Al_2O_3 device, (e) PBS test, (f) NBS test.

better than that of the pure SnO_2 thin film transistor derived from metalorganic precursor [15]. According to the previous report [48], a clockwise hysteresis behavior is induced by electron trapping at the acceptor-like trap states in Al_2O_3 bulk or at the GTO/Al_2O_3 interface. The smaller N_t than that of SiO_2 device (1.04×10^{12} cm^{-2}) may result in better hysteresis property. Research shows that the mobility enhancement for high-k Al_2O_3 dielectric is related to the atomic clean interface and low trap density [49]. Furthermore, the enhancement may be ascribed to the presence of trapped electrons in the solution-processed high-k dielectrics [50]. Fig. 6d shows the corresponding output curves which exhibits excellent electron modulation capacity and hard saturation property. The device parameters are detailed in Table 1. The PBS (+2 V) and NBS (−2 V) stabilities of GTO-Al_2O_3 devices are shown in Fig. 6e and 6f. It can be seen that the V_{th} shift of GTO-Al_2O_3 device under 1,200 s stress is only 0.53 V and 0.1 V for PBS and NBS tests, respectively, which is better than SiO_2 device, indicating the remarkable improvements of stabilities of the GTO device. It is reported that the origin of PBS instability of TFTs is trapped charges at the localized states at the semiconductor/sol-gel-Al_2O_3 interface [51]. Besides, we studied the stability of IZO-based and GTO channels which shows potential application (Table S1). In AOS materials, electron transport is governed by thermally activated electron hopping [33]. Fig. 7 shows energy-band diagram where localized states represent disordered metal ions. When an external electric field is applied, electrons will flow from a low energy band to a high energy band by "variable-range-hopping (VRH) percolation model" [33]. According to the VRH model, the μ_{FE} of amorphous TFTs strongly depends on the gate capacitance variation

© Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

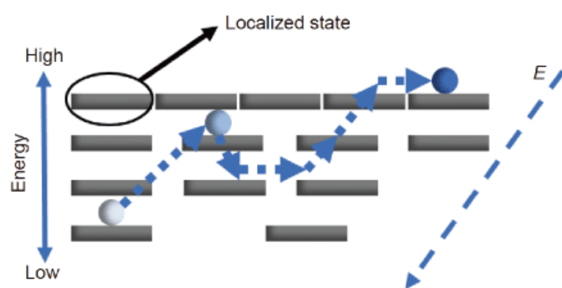

Figure 7 Energy-band diagram of the amorphous semiconductor.

which can be expressed by the reduced formula $\mu \sim \mu_{FE}^{0}(C_i/C_i^{0})^{\gamma-2}$. Compared with the a-GTO-SiO_2 device, the significant mobility enhancement is also attributed to the increase of gate capacitance (12.8 nF cm^{-2} for SiO_2, 257 nF cm^{-2} for Al_2O_3) [52]. The optimal performance for SnO_2 based TFTs has been realized in this work. But there still exist many challenges such as the degraded mobility in the PBS test. The trapped charge at GTO/Al_2O_3 interface will cause phonon scattering or coulomb scattering, leading to the mobility degradation [53]. Li *et al.* [54] also observed this phenomenon in IGZO/Al_2O_3 system. In the future, more effective methods will be adopted, such as SiO_2/Al_2O_3 bilayer, to improve the performance of the GTO device further. Related work is ongoing.

CONCLUSIONS

In this study, solution processed GTO thin films were applied in the fabrication of GTO-SiO_2-TFTs. The electrical properties, crystal structures, optical transparency and surface morphologies were investigated as a function of Ga contents. Results indicate that 20 at.% Ga content and 350°C annealing temperature may be a proper range for the acceptable performance of GTO-TFTs. The maximum μ_{FE}, SS, V_{th} and I_{on}/I_{off} for the optimized GTO-TFT are 6.8 $cm^2\ V^{-1}\ s^{-1}$, 0.9 V dec^{-1}, 0.7 V and 2.1×10^6, respectively. PBS and NBS tests of the corresponding device show positive shift of 6.6 V and negative shift of 6.4 V under 1,200 s bias stress which can be interpreted by charge trapping and H_2O adsorption mechanisms. In order to improve the performance of GTO-TFT, SiO_2 was substituted by high-*k* Al_2O_3 as the dielectric layer. The GTO-Al_2O_3-TFT represents the enhanced performance, such as a low operation voltage of 2 V, a maximum μ_{FE} of 69 $cm^2\ V^{-1}\ s^{-1}$, a SS of 76 mV dec^{-1}, V_{th} of 0.67 V, I_{on}/I_{off} of 1.8×10^7 and a small hysteresis voltage of 0.12 V. PBS and NBS tests demonstrate its better stabilities than GTO-SiO_2 device (PBS: 0.53 V, NBS: −0.1 V). The PBS instability of devices may originate from trapped charges at the localized states at the semiconductor/sol-gel-Al_2O_3 interface. This work may pave the way for the solution-processed, low cost and low consumption In-free transparent electronic devices.

Received 28 July 2018; accepted 5 December 2018; published online 26 December 2018

1 Nomura K, Ohta H, Takagi A, *et al.* Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. Nature, 2004, 432: 488–492
2 Liu G, Liu A, Zhu H, *et al.* Low-temperature, nontoxic water-induced metal-oxide thin films and their application in thin-film transistors. Adv Funct Mater, 2015, 25: 2564–2572
3 Dong J, Han D, Li H, *et al.* Effect of Al doping on performance of ZnO thin film transistors. Appl Surf Sci, 2018, 433: 836–839
4 Yang J, Ren J, Lin D, *et al.* Amorphous nickel incorporated tin oxide thin film transistors. J Phys D-Appl Phys, 2017, 50: 355103
5 Haxel G, Hedrick JB, Orris GJ, *et al.* Rare earth elements: critical resources for high technology, US Geological Survey fact sheet 087-02. Technical report, US Geological Survey, 2002
6 Niang KM, Cho J, Heffernan S, *et al.* Optimisation of amorphous zinc tin oxide thin film transistors by remote-plasma reactive sputtering. J Appl Phys, 2016, 120: 085312
7 Kyung-Chul Ok , Hyun-Jun Jeong , Hyun-Suk Kim , *et al.* Highly stable ZnON thin-film transistors with high field-effect mobility exceeding 50 cm^2/Vs. IEEE Electron Device Lett, 2015, 36: 38–40
8 Kamiya T, Nomura K, Hosono H. Subgap states, doping and defect formation energies in amorphous oxide semiconductor *a*-$InGaZnO_4$ studied by density functional theory. Phys Status Solidi A, 2010, 207: 1698–1703
9 Hosono H. Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application. J Non-Crystalline Solids, 2006, 352: 851–858
10 Yang J, Meng T, Yang Z, *et al.* Investigation of tungsten doped tin oxide thin film transistors. J Phys D-Appl Phys, 2015, 48: 435108
11 Yang J, Fu R, Han Y, *et al.* The stability of tin silicon oxide thin-film transistors with different annealing temperatures. EPL, 2016, 115: 28006
12 Yang J, Yang Z, Meng T, *et al.* Effects of silicon doping on the performance of tin oxide thin film transistors. Phys Status Solidi A, 2016, 213: 1010–1015
13 Ross RC, Messier R. Microstructure and properties of RF-sputtered amorphous hydrogenated silicon films. J Appl Phys, 1981, 52: 5329–5339
14 Yabuta H, Sano M, Abe K, *et al.* High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature RF-magnetron sputtering. Appl Phys Lett, 2006, 89: 112123
15 Huang G, Duan L, Dong G, *et al.* High-mobility solution-processed tin oxide thin-film transistors with high-κ alumina dielectric working in enhancement mode. ACS Appl Mater Interfaces, 2014, 6: 20786–20794
16 Jang J, Kitsomboonloha R, Swisher SL, *et al.* Transparent high-performance thin film transistors from solution-processed SnO_2/ZrO_2 gel-like precursors. Adv Mater, 2013, 25: 1042–1047
17 Park JH, Choi WJ, Chae SS, *et al.* Structural and electrical properties of solution-processed gallium-doped indium oxide thin-

 © Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

film transistors. Jpn J Appl Phys, 2011, 50: 080202
18 Park WJ, Shin HS, Ahn BD, *et al.* Investigation on doping dependency of solution-processed Ga-doped ZnO thin film transistor. Appl Phys Lett, 2008, 93: 083508
19 Matsuda T, Umeda K, Kato Y, *et al.* Rare-metal-free high-performance Ga-Sn-O thin film transistor. Sci Rep, 2017, 7: 44326
20 Zhang X, Lee H, Kim J, *et al.* Solution-processed gallium–tin-based oxide semiconductors for thin-film transistors. Materials, 2018, 11: 46
21 Zhang YG, Huang GM, Duan L, *et al.* Full-solution-processed high mobility zinc-tin-oxide thin-film-transistors. Sci China Technol Sci, 2016, 59: 1407–1412
22 Epifani M, Arbiol J, Díaz R, *et al.* Synthesis of SnO_2 and ZnO colloidal nanocrystals from the decomposition of Tin(II) 2-ethylhexanoate and zinc(II) 2-ethylhexanoate. Chem Mater, 2005, 17: 6468–6472
23 Park HW, Choi MJ, Jo Y, *et al.* Low temperature processed InGaZnO thin film transistor using the combination of hydrogen irradiation and annealing. Appl Surf Sci, 2014, 321: 520–524
24 Li H, Qu M, Zhang Q. Influence of tungsten doping on the performance of indium–zinc–oxide thin-film transistors. IEEE Electron Device Lett, 2013, 34: 1268–1270
25 Rim YS, Kim DL, Jeong WH, *et al.* Effect of Zr addition on ZnSnO thin-film transistors using a solution process. Appl Phys Lett, 2010, 97: 233502
26 Tsaroucha M, Aksu Y, Irran E, *et al.* Synthesis of stannyl-substituted Zn_4O_4 cubanes as single-source precursors for amorphous tin-doped ZnO and Zn_2SnO_4 nanocrystals and their potential for thin film field effect transistor applications. Chem Mater, 2011, 23: 2428–2438
27 Ide K, Kikuchi Y, Nomura K, *et al.* Effects of excess oxygen on operation characteristics of amorphous In-Ga-Zn-O thin-film transistors. Appl Phys Lett, 2011, 99: 093507
28 Concepción P, Pérez Y, Hernández-Garrido JC, *et al.* The promotional effect of Sn-beta zeolites on platinum for the selective hydrogenation of α,β-unsaturated aldehydes. Phys Chem Chem Phys, 2013, 15: 12048–12055
29 Lin T, Li X, Jang J. High performance p-type NiO_x thin-film transistor by Sn doping. Appl Phys Lett, 2016, 108: 233503
30 García Núñez C, Pau JL, Ruíz E, *et al.* Thin film transistors based on zinc nitride as a channel layer for optoelectronic devices. Appl Phys Lett, 2012, 101: 253501
31 Fortunato E, Barquinha P, Martins R. Oxide semiconductor thin-film transistors: A review of recent advances. Adv Mater, 2012, 24: 2945–2986
32 Banger KK, Yamashita Y, Mori K, *et al.* Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a 'sol–gel on chip' process. Nat Mater, 2011, 10: 45–50
33 Lee E, Ko J, Lim KH, *et al.* Gate capacitance-dependent field-effect mobility in solution-processed oxide semiconductor thin-film transistors. Adv Funct Mater, 2014, 24: 4689–4697
34 Jeong S, Ha YG, Moon J, *et al.* Role of gallium doping in dramatically lowering amorphous-oxide processing temperatures for solution-derived indium zinc oxide thin-film transistors. Adv Mater, 2010, 22: 1346–1350
35 Yang J, Pi S, Han Y, *et al.* Characteristic of bismuth-doped tin oxide thin-film transistors. IEEE Trans Electron Devices, 2016, 63: 1904–1909
36 Mann JB, Meek TL, Allen LC. Configuration energies of the main group elements. J Am Chem Soc, 2000, 122: 2780–2783
37 Shin SY, Moon YK, Kim WS, *et al.* Characterization of the SnO_2 based thin film transistors with Ga, In and Hf doping. J Nanosci Nanotechnol, 2012, 12: 5459–5463
38 Chen TC, Chang TC, Hsieh TY, *et al.* Investigating the degradation behavior caused by charge trapping effect under DC and AC gate-bias stress for InGaZnO thin film transistor. Appl Phys Lett, 2011, 99: 022104
39 Jeong JK, Won Yang H, Jeong JH, *et al.* Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors. Appl Phys Lett, 2008, 93: 123508
40 Liu PT, Chou YT, Teng LF. Environment-dependent metastability of passivation-free indium zinc oxide thin film transistor after gate bias stress. Appl Phys Lett, 2009, 95: 233504
41 Zhang H, Guo L, Wan Q. Nanogranular Al_2O_3 proton conducting films for low-voltage oxide-based homojunction thin-film transistors. J Mater Chem C, 2013, 1: 2781–2786
42 Heo JS, Choi S, Jo JW, *et al.* Frequency-stable ionic-type hybrid gate dielectrics for high mobility solution-processed metal-oxide thin-film transistors. Materials, 2017, 10: 612
43 Jeong S, Lee JY, Lee SS, *et al.* Metal salt-derived In–Ga–Zn–O semiconductors incorporating formamide as a novel co-solvent for producing solution-processed, electrohydrodynamic-jet printed, high performance oxide transistors. J Mater Chem C, 2013, 1: 4236–4243
44 Branquinho R, Salgueiro D, Santos L, *et al.* Aqueous combustion synthesis of aluminum oxide thin films and application as gate dielectric in GZTO solution-based TFTs. ACS Appl Mater Interfaces, 2014, 6: 19592–19599
45 Cao Q, Xia MG, Shim M, *et al.* Bilayer organic–inorganic gate dielectrics for high-performance, low-voltage, single-walled carbon nanotube thin-film transistors, complementary logic gates, and p–n diodes on plastic substrates. Adv Funct Mater, 2006, 16: 2355–2362
46 Jiang Q, Lu J, Cheng J, *et al.* Combustion-process derived comparable performances of Zn–(In:Sn)–O thin-film transistors with a complete miscibility. Appl Phys Lett, 2014, 105: 132105
47 Liu A, Liu G, Zhu H, *et al.* Eco-friendly, solution-processed In–W–O thin films and their applications in low-voltage, high-performance transistors. J Mater Chem C, 2016, 4: 4478–4484
48 Xu W, Wang H, Xie F, *et al.* Facile and environmentally friendly solution-processed aluminum oxide dielectric for low-temperature, high-performance oxide thin-film transistors. ACS Appl Mater Interfaces, 2015, 7: 5803–5810
49 Xu W, Wang H, Ye L, *et al.* The role of solution-processed high-κ gate dielectrics in electrical performance of oxide thin-film transistors. J Mater Chem C, 2014, 2: 5389–5396
50 Zeumault A, Subramanian V. Mobility enhancement in solution-processed transparent conductive oxide TFTs due to electron donation from traps in high-k gate dielectrics. Adv Funct Mater, 2016, 26: 955–963
51 Avis C, Jang J. High-performance solution processed oxide TFT with aluminum oxide gate dielectric fabricated by a sol–gel method. J Mater Chem, 2011, 21: 10649–10652
52 Tiwari N, Rajput M, John RA, *et al.* Indium tungsten oxide thin films for flexible high-performance transistors and neuromorphic electronics. ACS Appl Mater Interfaces, 2018, 10: 30506–30513
53 Park JS, Jeong JK, Mo YG, *et al.* Impact of high-k TiO_x dielectric on device performance of indium-gallium-zinc oxide transistors. Appl Phys Lett, 2009, 94: 042105
54 Li J, Zhou F, Lin HP, *et al.* SiO_x interlayer to enhance the

 © Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018

performance of InGaZnO-TFT with AlO_x gate insulator. Curr Appl Phys, 2012, 12: 1288–1291

Acknowledgements This work was supported by the National Natural Science Foundation of China (61471126) and a grant from Science and Technology Commission of Shanghai Municipality (16JC1400603).

Author contributions Zhang Q supervised the experimental work. Ren J designed this work, prepared all samples and performed sample characterizations. All authors contributed to the discussion and writing of the manuscript.

Conflict of interest The authors declare no conflict of interest.

Supplementary information Supplementary data are available in the online version of the paper.

Jinhua Ren is currently pursuing the PhD degree in physics and electronics at the Department of Materials Science, Fudan University. His current research interest includes thin film transistors based on amorphous oxide semiconductors.

Qun Zhang is currently a professor at the Department of Materials Science, Fudan University. His current research interest includes oxide semiconductors, thin-film transistor, LCD, and AMOLED.

溶液法制备低电压及高性能非晶GaSnO薄膜晶体管

任锦华, 李凯文, 杨建文, 林东, 康皓清, 邵晶晶, 傅若凡, 张群*

摘要 本文以乙二醇单甲醚为溶剂，采用旋涂法制备了GaSnO半导体薄膜，研究了不同Ga掺杂含量和退火温度条件下薄膜的晶体结构、光学性质、化学价态和表面形貌信息，同时研究了GaSnO薄膜晶体管的电学性质. 接着采用高k值的Al_2O_3薄膜作为介质层，将上述优化好的GaSnO薄膜作为沟道层，制备了GaSnO/Al_2O_3薄膜晶体管. 实验研究发现，器件的性能得到了显著的提升，工作电压仅为2 V，最大场效应迁移率为69 cm^2 V^{-1} s^{-1}，阈值电压为0.67 V，电流开关比为1.8×10^7. 溶液法制备的非晶GaSnO薄膜晶体管可能会促进高性能无铟TFT器件以及低功耗、低成本电子器件的开发.

 © Science China Press and Springer-Verlag GmbH Germany, part of Springer Nature 2018