Research Square

Preprints are preliminary reports that have not undergone peer review.
They should not be considered conclusive, used to inform clinical practice,
or referenced by the media as validated information.

Solution Processed Low Voltage Metal-Oxide transistor by using TiO_2 /Li-Al_2O_3 stacked Gate Dielectric

Nila Pal
Indian Institute of Technology Banaras Hindu University: Indian Institute of Technology BHU Varanasi
Utkarsh Pandey
Indian Institute of Technology Banaras Hindu University: Indian Institute of Technology BHU Varanasi
Sajal Biring
Ming Chi University of Technology
Bhola Nath Pal (bnpal.mst@iitbhu.ac.in)
Indian Institute of Technology Banaras Hindu University: Indian Institute of Technology BHU Varanasi
https://orcid.org/0000-0001-7512-3441

Research Article

Keywords: Solution process, Metal oxide semiconductor, Ion-conducting gate dielectric, Bilayer stack dielectric, TFT, Schottky junction

Posted Date: May 11th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-350224/v1

License: This work is licensed under a Creative Commons Attribution 4.0 International License.
Read Full License

Version of Record: A version of this preprint was published at Journal of Materials Science: Materials in Electronics on January 29th, 2022. See the published version at https://doi.org/10.1007/s10854-021-07581-z.

// Abstract

A solution processed top-contact bottom gated SnO_2 thin-film transistor (TFT) has been fabricated by using a TiO_2/ Li-Al_2O_3 bilayer stacked gate dielectric that show operating voltage of this TFT within 2.0 V. It is observed that the bilayer dielectric has much higher areal capacitance with lower leakage current density that significantly improve the overall device performance of TFT. The TFT with bilayer gate dielectric shows an effective carrier mobility (μ_{sat}) of 9.2 $cm^2V^{-1}s^{-1}$ with an on/off ratio of 7.1×10^3 which are significantly higher with respect to the TFT with a single layer Li-Al_2O_3 gate dielectric. The origin of this improvement is due to the Schottky junction between the highly doped silicon (p^{++}-Si) and TiO_2 of bilayer stacked dielectric that induced electrons to the channel which reduces the dielectric/semiconductor interface trap state. This investigation opens a new path to develop TFT device performance using a suitable bilayer stack of gate-dielectric.

1. Introduction

The charge carrier conduction of the channel of a thin film transistor (TFT) normally occurs within < 10 nm thickness of the semiconductor film next to the gate-dielectric.[1] Therefore, the field effect charge transport phenomena of a TFT is not only dependent on the microstructures of the semiconductor but is also strongly affected by the surface properties of the gate-insulator. Conventional silicon gate dielectric (SiO_2) commonly offers smooth surface morphology which is capable of minimizing the defect density of semiconductor-insulator interface. However, the dielectric constant of SiO_2 is very low (3.9). Therefore, to reduce the operating voltage of a TFT below 2 V for portable electronics application, it requires very low thickness of SiO_2 (< 10 nm) which sometime becomes very licky.[2,3] Employment of high-k dielectric materials insead of SiO_2 is the best alternative which allow us to deposit thicker dielectric film by maitaining the advantage of low operating voltage TFT fabrication.[4,5,6,7,8] However, ionic bonds in high-k dielectrics results in high defect concentrations with oxygen vacancies (V_O) being the primary source of traps. These can be source of fixed charges or act as electron traps, scattering carriers in channel (decreasing mobility), changing the threshold voltage (V_T) and assisting dielectric breakdown and gate-leakage mechanism,[9] decreasing device performance, and affects the stability and reliability of devices. To overcome these problems different approaches like inorganic-organic hybrid dielectric,[10]{Canimkurbey, 2019 #81} Ta_2O_5/SiO_2 multicomponent dielectric,[11] bilayer-dielectric stack[12,13,14], have been used. A new method to reduce the semiconductor-insulator interface trap-states is found by implying n-type TiO_2 as interface layer between highly doped silicon (p^{++}-Si) substrate and high-k ion conducting Li_5AlO_4 dielectric, which drastically enhance the TFT device performance due to the formation of Schottky junction of p^{++}-Si/TiO_2.[15]However, capacitance of this $Li_5AlO_{4/}TiO_2$ stacked dielectric reduce rapidly > 10^4 Hz. To enhance this frequency range and overall performance of TFT, more detailed study is required for different combinations of stacked dielectric.

In this work, we have synthesized Li-doped alumina ($Li\text{-}Al_2O_3$) thin film by sol-gel method and have used this ionic dielectric to fabricate TiO_2 /$Li\text{-}Al_2O_3$ stacked gate dielectric. The variation of areal capacitance of this bilayer stacked gate dielectric only 20% up to the frequency 10^5 Hz. To realize the overall improvement of TFT performance and the mechanism of this development, two sets of solution processed SnO_2 TFT were fabricated; one with TiO_2 gate interface and another without gate interface. Comparative studies of these two TFT reveals a significant improvement of device performance. A schematic presentation of energy band gap of multilayer thin films and related charge transfer of p^{++}-Si/TiO_2 Schottky junction explain the probable reason for enhancing device performance.

2. Experimental

2.1 Material Synthesis

As mentioned earlier, all TFTs are fabricated by low-cost solution processed technique. In this process, both gate dielectric (TiO_2 and $Li\text{-}Al_2O_3$) and semiconducting layers (SnO_2) are deposited from the precursor solution by spin coating method. For TiO_2 deposition, a solution of 100 mM was prepared by dissolving Titanium(IV) Butoxide in 2-methoxy ethanol (2ME) followed at the room temperature stirring process by a magnetic stirrer about 30 minutes. Similarly, to prepare the $Li\text{-}Al_2O_3$ dielectric, two different solutions of lithium acetate and aluminium nitrate nonahydrate of concentration 500 mM were prepared by using 2-methoxy ethanol as solvent. These two homogeneous solutions are mixed with a ratio of 1:11 to maintain the atomic ratio of the final product of $Li\text{-}Al_2O_3$. This mixture of solutions was left for 24 hours for proper gelation before depostion.[16] Finally, solution was filtered by 0.45 μm PVDF filter before spin coating. For semiconductor (SnO_2) thin film deposition, a solution of $SnCl_2$ has been prepared by using 2-methoxy ethanol as solvent.

2.2 Device Fabrication

Metal-Oxide TFTs are fabricated in a top-contact bottom-gate configuration by using highly p-doped Si wafer (p^{++}-Si) as a substrate as well as gate electrode. Initially, all the Si wafers are cleaned with standard cleaning process. After wet cleaning, wafers were treated with an oxygen plasma for 10 minutes before spin coating. Plasma treatment makes the surface hydrophilic which increases the adhesive property and helps to form pinhole free smooth film during spin coating. Two types of devices are fabricated without and with TiO_2 interface named as Device 1 and Device 2 shown in Fig. 1a and b, respectively. The TiO_2 thin film is deposited on p^{++}-Si wafer spin coating with a spinning speed of 3500 rpm for 40 seconds followed by a drying process of a preheated hot-plate (set at 90°C) to evaporate the solvent. Afterwards, this film was annealed at 350°C for 30 minutes to form a polycrystalline thin film of TiO_2. On top of this, the precursor solution of $Li\text{-}Al_2O_3$ was spin coated with a speed 5000 rpm for 50s followed by annealing process at 350°C for 30 minute. The dielectric film coating was repeated three times to achieve a desired thickness of the dielectric layer. Finally this film was annealed at 500°C for one hour to form $Li\text{-}Al_2O_3$ thin film. For Device 1, the same procedure was followed except the TiO_2 layer deposition. After dielectric

deposition, the precursor solution of SnO_2 was spin coated (4000 rpm for 40 sec.) and subsequent annealing (500C for 30 minute) process.[17] Finally, aluminium source/drain electrode are deposited by thermal evaporation method with width-to-length ratio of 118. In addition to this TFT fabrication, the metal-insulator-metal (MIM) devices (Fig. 1c and d) were fabricated in a similar process for the electrical characterization of single and bilayer dielectric thin films.

2.3 Material and Device characterization

Crystal phase/structural analysis of thin films were carried out by grazing incidence XRD (Rikagu, Smart Lab) with monochromatized Cu Kα radiation (λ = 1.5405 Å). Atomic force microscopy (AFM) study has been performed by using "NTMDTNTEGRA-prima" to measure the roughness of different thin film surfaces. Thin films are deposited on p^{++}-Si substrate in both cases. Frequency vs. Capacitance (C-f) measurement has been done by LCR meter (keysight LCR meter E4990A). All the electrical characteristics of TFTs and leakage current measurement of MIM devices have been measured by semiconductor parameter analyzer (KEYSIGHT B1500A).

3. Results And Discussions

3.1 Grazing Incidence X-Ray Diffraction Pattern of Thin Films

To analyse the structural properties of spin coated TiO_2, Li-Al_2O_3 and SnO_2 thin film, individually all these thin films were deposited on p^{++}-Si substrate under the same condition of TFT fabrication. Figure 2a shows the GIXRD patterns of TiO_2 thin film which indicates a crystalline peak at 2θ ~ 25.28, which is corresponding to the (101) plane of stable anatase phase of TiO_2. The GIXRD patterns of Li-Al_2O_3 dielectric which is shown in Fig. 2b, didn't show any diffraction peak, indicating the amorphous nature of Li-Al_2O_3 dielectric.

The GIXRD pattern of SnO_2 thin film has been shown in Fig. 2c that clearly identified diffraction peaks at the 2θ angle 26.6, 34.2, 52.7, and 54.7 which are corresponds the reflection planes of (110), (101), (211) and (220) respectively; justify the tetragonal phase of SnO_2 (JCPDS 88–0287).

3.2 Surface Morphology of Dielectric Thin Films

The surface morphologies of single layer Li-Al_2O_3 and bilayer TiO_2/Li-Al_2O_3 dielectrics were studied by atomic force microscopy (AFM). All these dielectric layers were deposited on p^{++}-Si substrates with the same condition as for TFT fabrication. The 2-D and 3-D morphologies of these two dielectric thin films are shown in Fig. 3a and 4b represent the AFM images of Li-Al_2O_3 dielectric whereas, Fig. 3c and 4d are AFM pictures of TiO_2/Li-Al_2O_3 dielectrics. Figure 3 shows that the RMS roughness of both dielectric thin films are < 1 nm which is suitable for high performance TFT fabrication. However, compared to single layer Li-Al_2O_3 surface (0.26 nm) a little bit smoother than bilayer TiO_2/Li-Al_2O_3 surface (0.46 nm).

3.3 Dielectric and Electrical characterization

The leakage current density and areal capacitance of single layer and bilayer dielectric are measured with metal-insulator-metal (MIM) architecture which is shown in Fig. 4. Figure 4a shows the leakage current density vs. applied voltage graphs of both dielectric thin films. This data indicates that stacked dielectric of p^{++}-Si /TiO_2/Li-Al_2O_3/Al device has one order lower leakage current density than p^{++}-Si /Li-Al_2O_3/Al device at applied voltage 2 V with a current density of 6.2 $\times 10^{-5}$ A/cm^2 where as single layer dielectric MIM device shows a current density of 2.0 $\times 10^{-4}$ A/cm^2 at 2.0 V. The dielectric-leakage current of bilayer film is reasonably low for TFT fabrication that operates within 2.0 V operating voltage. The reduction of gate-leakage current in case of bilayer dielectric may be resulted from the lattice mismatch of two different materials with different grain shapes at the interfaces, which is well understood from the earlier multilayered dielectric studies.[14]

The variation of capacitance per unit area of the same set of MIM devices with frequencies (20 to 10^5 Hz) at room temperature are represented in Fig. 4b. It is well known that the capacitance decreases with frequency due to the different relaxation times originated from different types of polarization contribution.[6] Similar behavior is observed in both types of MIM devices that reduce significantly > 10^3Hz. However, the capacitance of single layer p^{++}-Si/ Li-Al_2O_3/Al device changes more rapidly compared to bilayer p^{++}-Si/TiO_2/Li-Al_2O_3/Al MIM device. The measured areal capacitance (C) values of single and bilayer MIM devices are 55 nF/cm^2 and 66 nF/cm^2 at 50 Hz frequency, respectively. This study is the indication of the higher areal capacitance value with wider frequency range of a bilayer stacked dielectric thin film which originated from additional TiO_2 layer. The TiO_2/Li-Al_2O_3 bilayer act as series combination of TiO_2 and Li-Al_2O_3 parallel plate capacitor and the resultant capacitance can be written as;

$$\frac{1}{\mathrm{C}_{\mathrm{effective}}} = \frac{1}{C_{\mathrm{Ti}O_2}} + \frac{1}{C_{Li-Al_2O_3}}$$

The high-k value of TiO_2 layer increases the capacitance of TiO_2/Li-Al_2O_3 dielectric with respect to Li-Al_2O_3 single layer.

3.4 Electical Characterization of Single and Bilayer Dielectric Thin Film Transistor

To realize the performance of these dielectric layers for the application of gate dielectric of TFTs, two sets of devices have been fabricated. Device 1 is the reference TFT without TiO_2 gate interface and Device 2 is TFT with TiO_2 gate-interface in between gate electrode and Li-Al_2O_3 gate-dielectric. A higher channel length of 200 µm with W/L (W = 23.6 mm, L = 0.2 mm) ratio of 118 is chosen to avoid the overestimation of carrier mobility value due to grain boundary effect, which is highly dominating below 25 µm channel length and W/L ratio of 10. [17,18] Additionally, high-performance TFT with larger device area demands good quality of dielectric with pinhole-free uniform thin film with very low defect states. Figure 5 shows

transistor characteristics of two types of device, and are measured at ambient conditions. The I_D-V_D characteristics of Device 1 and Device 2 are shown in Fig. 5 a and b, respectively. The applied V_D are swept from 0 to 1V with different constant gate voltages ranging from − 0.2 to 2.0V with step of 0.2V. The linear and saturation region of the output characteristics are clearly shown by the figurefor both sets of devices.

The Transfer characteristics of SnO_2 TFT without and with TiO_2 interface are shown in Fig. 5c and d. The gate to source voltages is swept from − 0.2 to 2V keeping V_D constant at 1V for both devices. All the measurement conditions and parameters are kept the same for all devices. From comparative data of transfer characteristics (Fig. 5e and f), it is observed that the threshold voltage of Device 2 (0.29V) is sufficiently lower than Device 1 (0.85 V). Besides, the calculated value of I_{ON}/I_{OFF} ratio for Device 2 is 7.2 x 10^3 which is higher than Device 1 (i.e. 3.6 x10^3). The effective carrier mobility (μ), subthreshold swing (SS) and dielectric/semiconductor interface trap-states (N_{SS}^{Max}) of TFT have been calculated by using the following equations.[19]

$$SS = \left[\frac{d\left(logI_D\right)}{dV_G}\right]^{-1} \ldots\ldots\ldots\ldots.\ldots(1)$$

$$I_D = \mu C\frac{W}{2L}\left(V_G - V_T\right)^2 \ldots\ldots\ldots\ldots(2)$$

$$N_{SS}^{Max} = \left[\frac{SS \times loge}{\frac{kT}{q}} - 1\right]\frac{C}{q} \ldots..(3)$$

Where k, T and q are the Boltzmann constant, temperature in absolute scale and charge of electron respectively. The saturation carrier mobilities of both devices are calculated by using Eq. 1 and extracted from the linear fitting of $(I_D)^{1/2}$ vs. V_G plot. From comparision of both devices, it is observed that device 2 shows better performance having saturation electron mobility of 9.2 $cm^2V^{-1}s^{-1}$ than device 1 that shows saturation electron mobility of 7.7 $cm^2V^{-1}s^{-1}$. The subthreshold swing (SS) value of both devices are extracted from the slope at lower gate-voltage regime of the log (I_D) vs. V_G graphs (shown in Fig. 5 e and f) and by using Eq. 2. Device 2 has lower SS value (250 mV/decade) than Device 1 (280 mV/decade). The dielectric-semiconductor interface trap-state densities have been derived from Eq. 3. Device 1 has a 1.5 time higher interface trap-state density than Device 2. The lower (N_{SS}^{Max}) leads to less trapping of

charge carriers in the dielectric-semiconductor interface, resulting in improvement of effective mobility and higher drain current.[20] All the TFT parameters are summarized in Table 1.

Table 1 : Summary of the TFT parameters of SnO_2 transistors with single layer and bilayer stack gate-dielectrics.

Device	Threshold Voltage (V)	I_{ON}/I_{OFF}	Subthreshold Swing (mV/decade)	Saturation Mobility ($cm^2V^{-1}s^{-1}$)	Interface trap-state density (cm^{-2})
Si^{++}/Li-Al_2O_3/SnO_2/Al	0.85	$3.6x10^3$	280	7.7	$1.6x10^{12}$
Si^{++}/TiO_2/Li-Al_2O_3/SnO_2/Al	0.29	$7.2x10^3$	250	9.2	$1.1x10^{12}$

To understand the reason behind the higher performance of device 2 with TiO_2/Li-Al_2O_3 stack dielectric, a schematic diagram of energy bands of two types of SnO_2 TFTs have been illustrated in Fig. 6. Since p^{++}-Si(111)/TiO_2 interface forms a Schottky junction at zero gate bias, the electron of TiO_2 layer transferred to the p^{++}-Si gate-electrode creates a depleted layer of positive charge at TiO_2 thin film. However, hole is not allowed to transfer from p^{++}-Si to TiO_2 layer due to large potential barrier in p^{++}-Si(111)/TiO_2 interface.[21,22] Hence, the layer of positive charge of TiO_2 thin film induces electrons of the channel of TFT (SnO_2) to accumulate at the Li-Al_2O_3/SnO_2 interface, which initially fills up the electron trap-states (N_{SS}^{Max}) at the dielectric/semiconductor interface (Fig. 6a).

This phenomenon is happening without gate-bias. Therefore, TiO_2 thin film effectively reduces the interface trap-states, resulting in a lower sub-threshold swing and threshold voltage. Although, this phenomena is not occurring in device 1 because of the high barrier height of insulating Li-Al_2O_3 layer. Therefore, electrons cannot be ejected from Li-Al_2O_3 to p^{++}-Si gate-electrode (Fig. 6c). Under accumulation mode operation, a positive gate voltage is applied to both of the devices (Fig. 6band d). However, this bias does not change the depletion layer width of p^{++}-Si(111)/TiO_2 interface due to the intermediate insulating Li-Al_2O_3 layer. This phenomena effectively enhances the accumulation of mobile charge carriers in the channel of device 2, that improves the device performance over Device 1.

4. Conclusion

In conclusion, high-performance solution processed low operating voltage SnO_2 thin-film transistor has been fabricated onto sol-gel derived ion-conduction Li-Al_2O_3 dielectric by using TiO_2 gate interface. A comparative study of two sets of SnO_2 TFTs with and without TiO_2 interface have been demonstrated. The Schottky junction formation between p^{++}-Si and n-type TiO_2 help to accumulate extra electrons at the Li-Al_2O_3/SnO_2 interface, which essentially fills up the interface trap-states and reduces the sub-threshold swing (SS) as well as threshold voltage (V_T) and enhance the saturation carrier mobility of the device with compared to the device without TiO_2 interface. The high-k value of TiO_2 improves the capacitance of

the TiO_2 / Li-Al_2O_3 stack dielctric as well as it’s leakage current also reduced compared to single layered Li-Al_2O_3 dielectric. We have achieved an effective carrier mobility (μ_{sat}) of 9.2 $cm^2V^{-1}s^{-1}$, SS of 250 mV/decade, and V_T of 0.29 V in TiO_2/ Li-Al_2O_3 stack TFT with an I_{ON}/I_{OFF} ratio of $7.2x10^3$. This investigation opens a new path to develop high- performance TFT devices by using a suitable bilayer stack of gate-dielectrics.

Declarations

Acknowledgement

This work was supported by the "Science and Engineering Research Board," India (EMR/2015/000689). The authors are grateful to the Central Instrument Facility Centre, IIT (BHU), for providing the AFM measurement facility. Nila Pal thanks DST-SERB for providing SRF fellowship, and Utkarsh Pandey thanks IIT (BHU) for providing Ph.D. fellowship.

Conflict of interest The authors declare no competing financial interest.

References

1. J. Zaumseil, H. Sirringhaus, Electron and ambipolar transport in organic field-effect transistors. Chemical reviews **107**(4), 1296–1323 (2007)
2. J. Robertson, R.M. Wallace, High-K materials and metal gates for CMOS applications. Materials Science and Engineering: R: Reports **88**, 1–41 (2015)
3. I.R. Committee, International technology roadmap for semiconductors. 2008
4. B.N. Pal, B.M. Dhar, K.C. See, H.E. Katz, Solution-deposited sodium beta-alumina gate dielectrics for low-voltage and transparent field-effect transistors. *Nature materials* 2009, *8* (11), 898
5. N.K. Chourasia, A. Sharma, V. Acharya, N. Pal, S. Biring, B.N. Pal, Solution processed low band gap ion-conducting gate dielectric for low voltage metal oxide transistor. J. Alloy. Compd. **777**, 1124–1132 (2019)
6. B. Wang, W. Huang, L. Chi, M. Al-Hashimi, T.J. Marks, A. Facchetti, High-k gate dielectrics for emerging flexible and stretchable electronics. Chemical reviews **118**(11), 5690–5754 (2018)
7. A. Sharma, N.K. Chourasia, A. Sugathan, Y. Kumar, S. Jit, S.-W. Liu, A. Pandey, S. Biring, B.N. Pal, Solution processed Li 5 AlO 4 dielectric for low voltage transistor fabrication and its application in metal oxide/quantum dot heterojunction phototransistors. *Journal of Materials Chemistry C* 2018, *6* (4), 790–798
8. A. Sharma, N.K. Chourasia, V. Acharya, N. Pal, S. Biring, S.-W. Liu, B.N. Pal, Ultra-Low Voltage Metal Oxide Thin Film Transistor by Low-Temperature Annealed Solution Processed LiAlO 2 Gate Dielectric. Electron. Mater. Lett. **16**(1), 22–34 (2020)

9. S. Mohsenifar, M. Shahrokhabadi, Gate stack high-κ materials for Si-based MOSFETs past, present, and futures. *terminology* 2015, *2*, 5
10. Q. Li, S. Li, D. Yang, W. Su, Y. Wang, W. Zhou, H. Liu, S. Xie, Designing hybrid gate dielectric for fully printing high-performance carbon nanotube thin film transistors. *Nanotechnology* 2017, *28* (43), 435203
11. J. Martins, A. Kiazadeh, J.V. Pinto, A. Rovisco, T. Gonçalves, J. Deuermeier, E. Alves, R. Martins, E. Fortunato, P. Barquinha, Ta2O5/SiO2 Multicomponent Dielectrics for Amorphous Oxide TFTs. Electronic Materials **2**(1), 1–16 (2021)
12. J.-W. Jo, K.-H. Kim, J. Kim, S.G. Ban, Y.-H. Kim, S.K. Park, High-mobility and hysteresis-free flexible oxide thin-film transistors and circuits by using bilayer sol–gel gate dielectrics. ACS Appl. Mater. Interfaces **10**(3), 2679–2687 (2018)
13. K. Pak, J. Choi, C. Lee, S.G. Im, Low-Power, Flexible Nonvolatile Organic Transistor Memory Based on an Ultrathin Bilayer Dielectric Stack. Advanced Electronic Materials **5**(4), 1800799 (2019)
14. J.-P. Locquet, C. Marchiori, M. Sousa, J. Fompeyrine, J.W. Seo, High-K dielectrics for the gate stack. J. Appl. Phys. **100**(5), 051610 (2006)
15. A. Sharma, N.K. Chourasia, N. Pal, S. Biring, B.N. Pal, Role of electron donation of TiO2 gate interface for developing solution-processed high-performance one-volt metal-oxide thin-film transistor using ion-conducting gate dielectric. *The Journal of Physical Chemistry C* 2019, *123* (33), 20278–20286
16. Y. Liu, P. Guan, B. Zhang, M.L. Falk, H.E. Katz, Ion dependence of gate dielectric behavior of alkali metal ion-incorporated aluminas in oxide field-effect transistors. Chem. Mater. **25**(19), 3788–3796 (2013)
17. K. Okamura, D. Nikolova, N. Mechau, H. Hahn, Appropriate choice of channel ratio in thin-film transistors for the exact determination of field-effect mobility. *Applied Physics Letters* 2009, *94* (18), 183503
18. G. Adamopoulos, A. Bashir, S. Thomas, W.P. Gillin, S. Georgakopoulos, M. Shkunov, M.A. Baklar, N. Stingelin, R.C. Maher, L.F. Cohen, Spray-Deposited Li-Doped ZnO Transistors with Electron Mobility Exceeding 50 cm2/Vs. Advanced materials **22**(42), 4764–4769 (2010)
19. E. Fortunato, P. Barquinha, R. Martins, Oxide semiconductor thin-film transistors: a review of recent advances. *Advanced materials* 2012, *24* (22), 2945–2986
20. C. Zhu, A. Liu, G. Liu, G. Jiang, Y. Meng, E. Fortunato, R. Martins, F. Shan, Low-temperature, nontoxic water-induced high-k zirconium oxide dielectrics for low-voltage, high-performance oxide thin-film transistors. *Journal of Materials Chemistry C* 2016, *4* (45), 10715–10721
21. S. Avasthi, W.E. McClain, G. Man, A. Kahn, J. Schwartz, J.C. Sturm, Hole-blocking titanium-oxide/silicon heterojunction and its application to photovoltaics. Appl. Phys. Lett. **102**(20), 203901 (2013)
22. J. Jhaveri, A.H. Berg, J.C. Sturm, Isolation of hole versus electron current at p-Si/TiO 2 selective contact using a heterojunction bipolar transistor structure. *IEEE Journal of Photovoltaics* 2018, *8* (3), 726–732

Figures

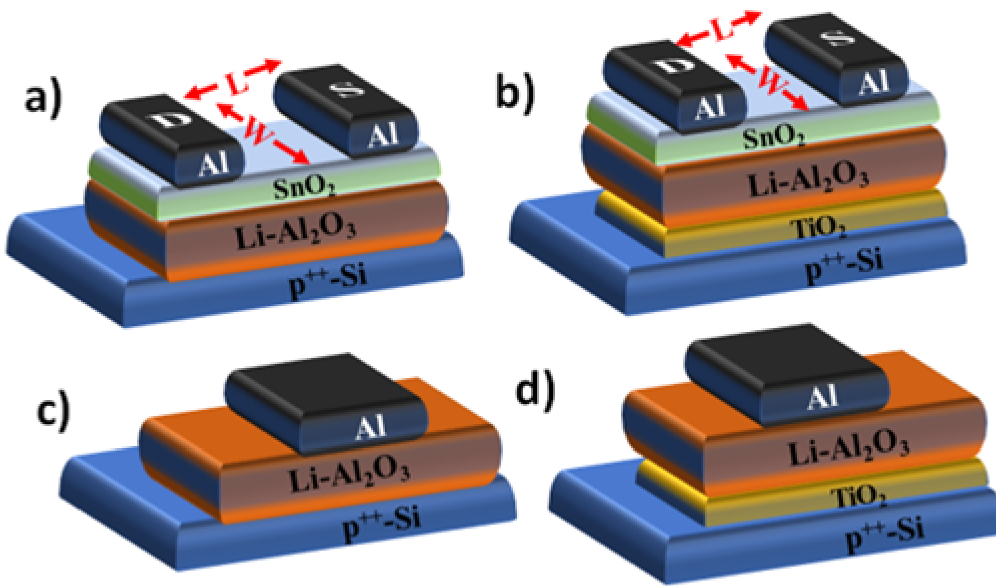

Figure 1

Schematic diagram of TFT devices , a) Device 1 with single layer Li-Al2O3 gate-dielectrc, b) Device 2 with bilayer TiO2/Li-Al2O3 gate-dielectric. MIM devices with c) Li-Al2O3 gate-dielectric and, d) TiO2/Li-Al2O3 gate-dielectric.

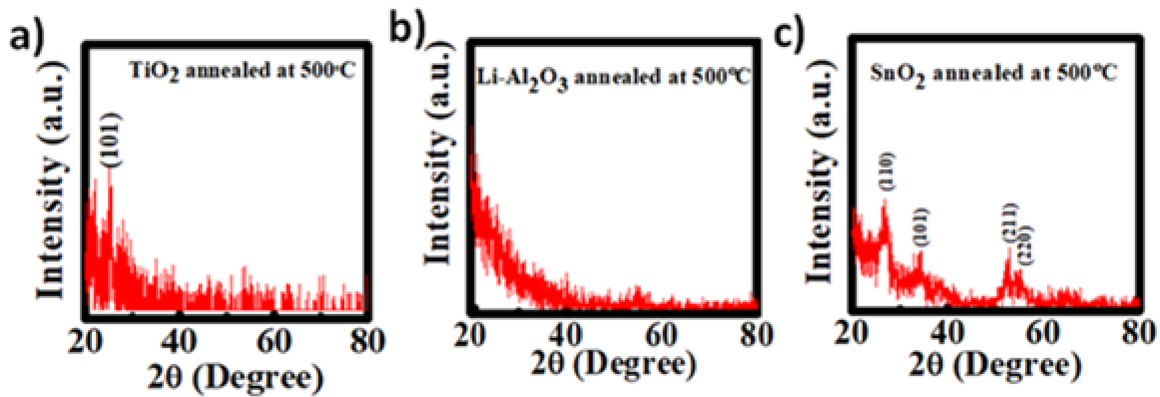

Figure 2

The GIXRD patterns of a) TiO2, b) Li-Al2O3 dielectric, and c) SnO2 semiconductor layer annealed at 500C.

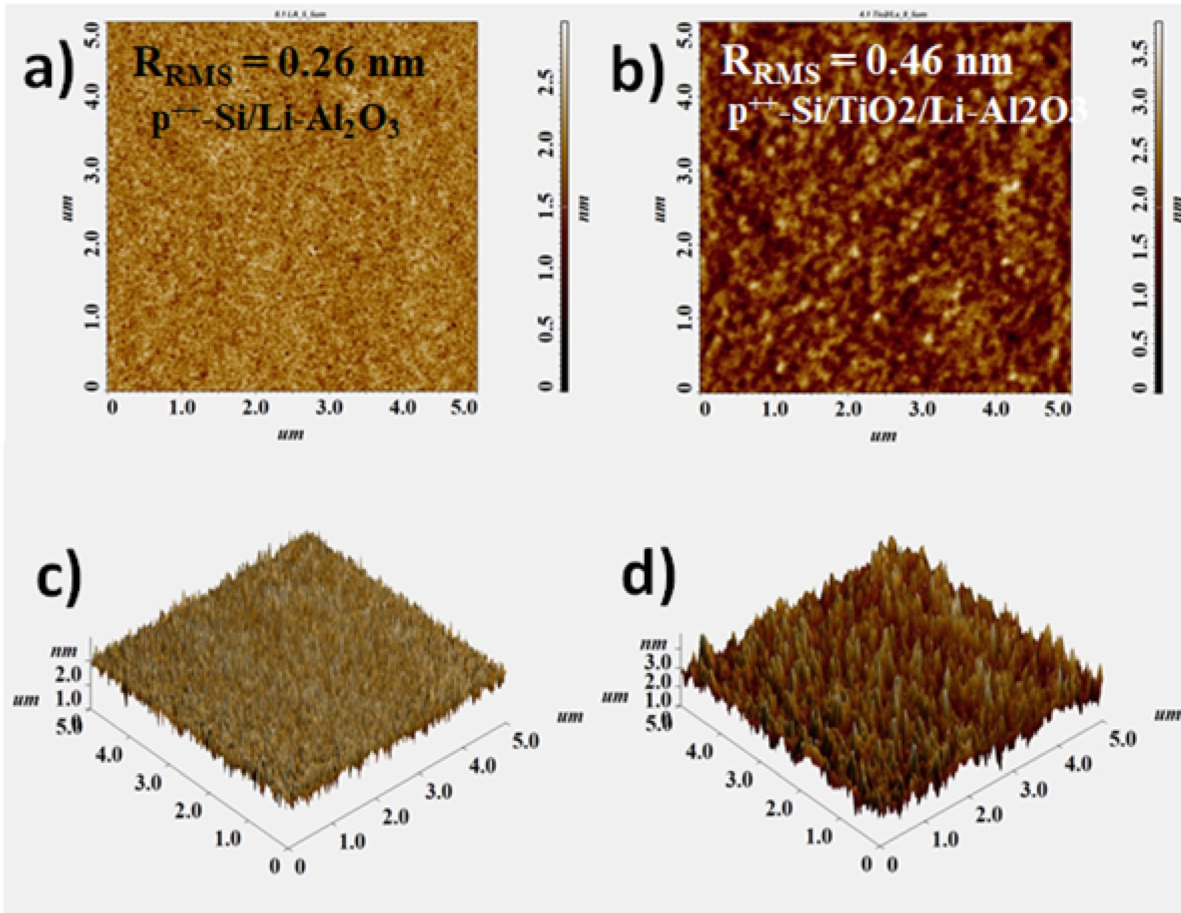

Figure 3

2D AFM image of a) Li-Al2O3 and b) TiO2/Li-Al2O3 dielectric. 3D AFM images of c) a) Li-Al2O3 and b) TiO2/Li-Al2O3 dielectric.

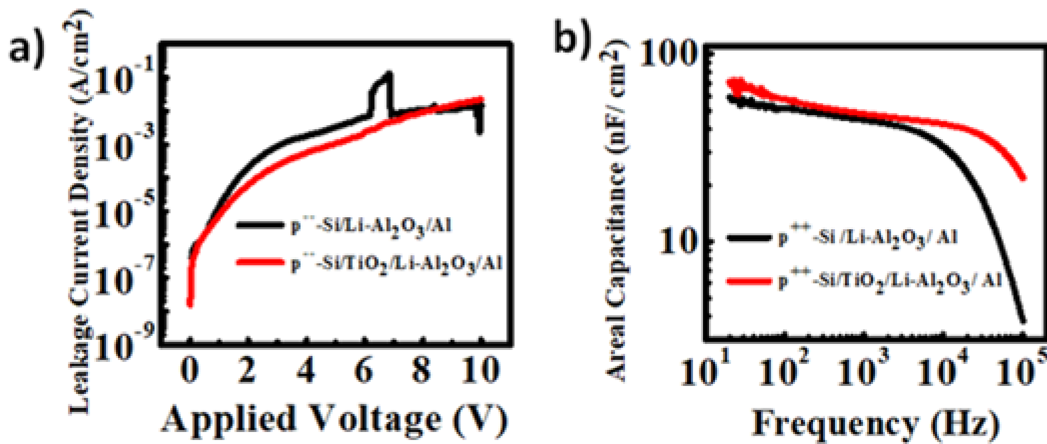

Figure 4

Variation of a) Leakage current density with applied voltage, and b) Areal capacitance with frequency for p++-Si/Li-Al2O3/Al and p++-Si/TiO2/Li-Al2O3/Al MIM devices.

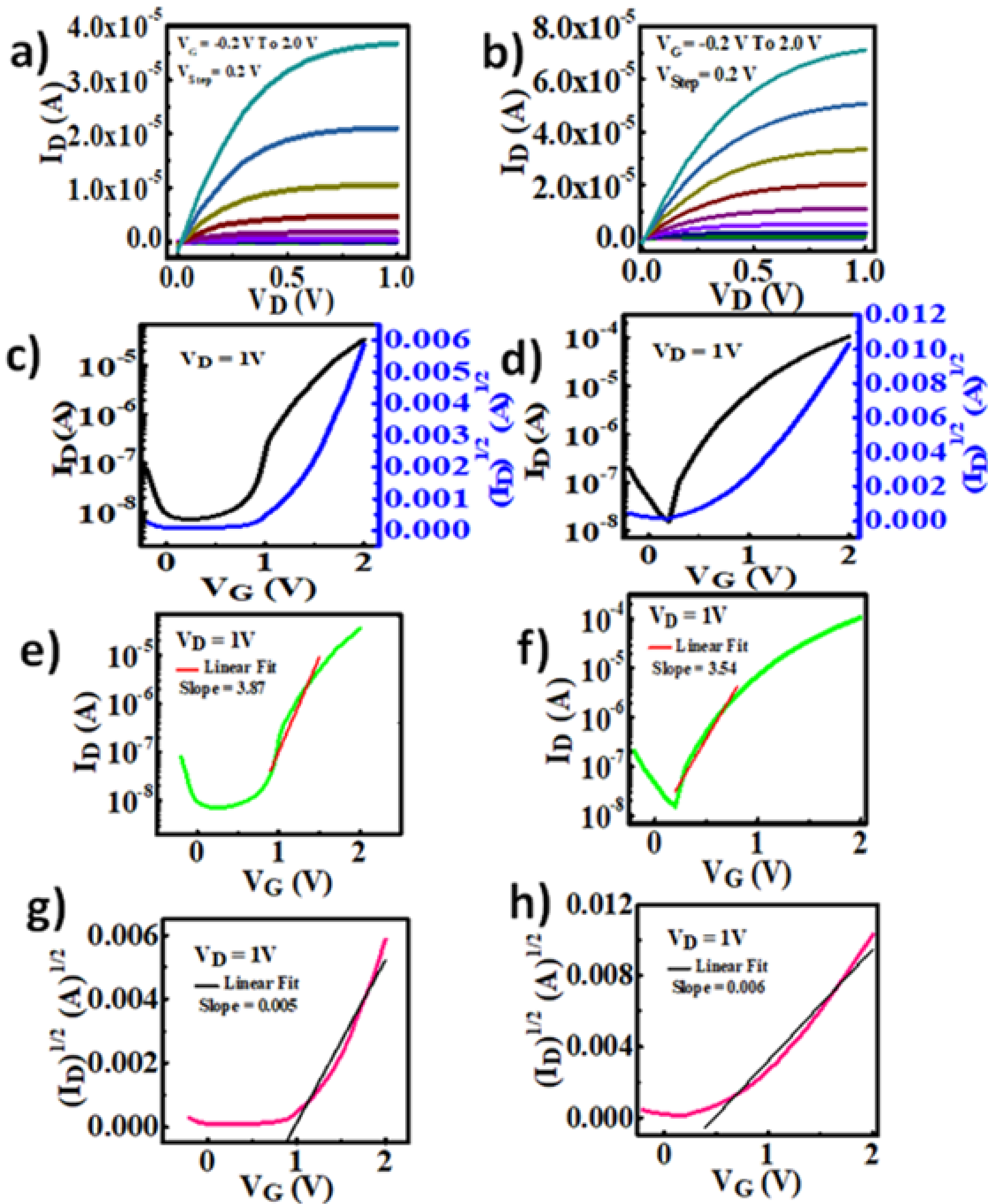

Figure 5

Transistor characterization of single layer and bilayer gate-dielctric SnO2 TFT. a) and b) Output chracteristics; c) and d) Transfer characteristics; e) and d) Linear fit of log(ID) vs. VG curve to extract SS value; g) and h) Linear fit of (ID)1/2 vs. VG to extract carrier mobility of Device 1 and Device 2, respectively.

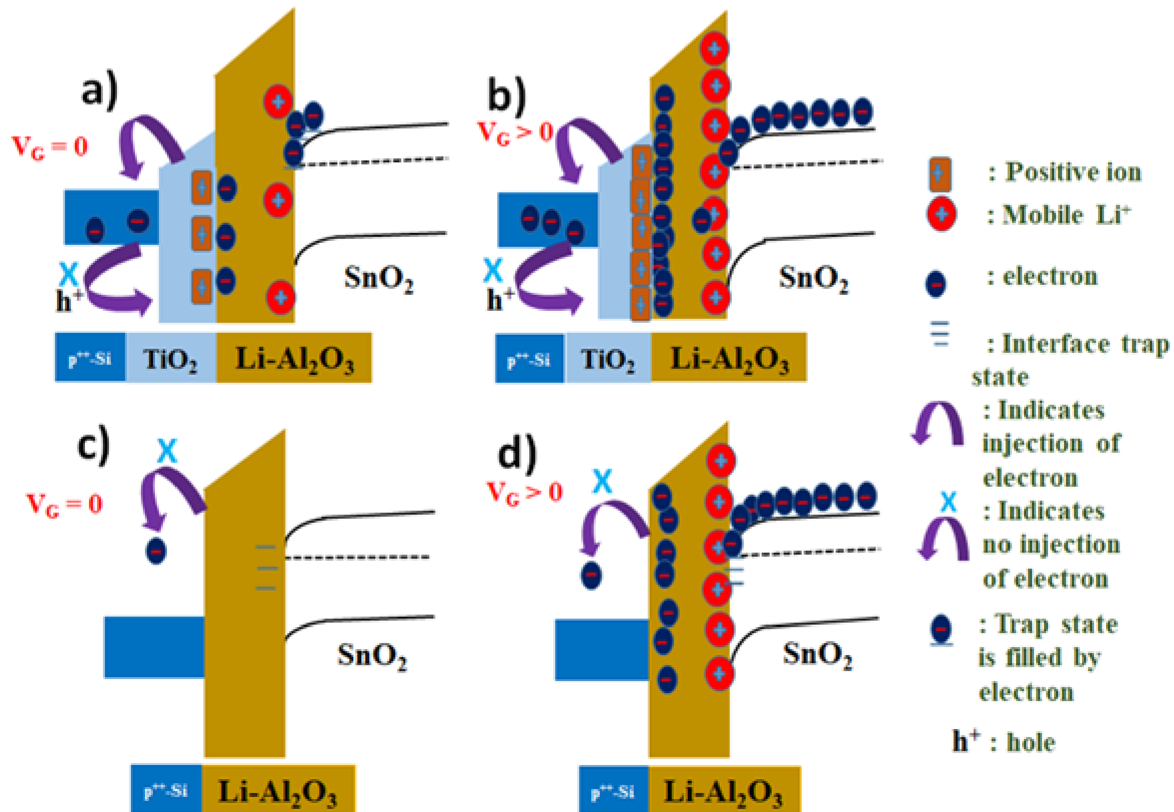

Figure 6

Metal-Insulator-Semiconductor structures illustrating the mechanism of variation in transistor performances with single layer and bilayer dielectric stack. Enery band diagram of a) and c) without applied bias, and b) and d) with applied positive bias of Device 2 with bilayer TiO2/Li-Al2O3 dielectric and Device 1 with single layer Li-Al2O3 dielectric, respectively.