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Solution processed molecular floating gate for flexible flash memories

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Solution processed fullerene (C_{60}) molecular floating gate layer has been employed in low voltage nonvolatile memory device on flexible substrates. We systematically studied the charge trapping mechanism of the fullerene floating gate for both p-type pentacene and n-type copper hexadecafluorophthalocyanine ($F_{16}CuPc$) semiconductor in a transistor based flash memory architecture. The devices based on pentacene as semiconductor exhibited both hole and electron trapping ability, whereas devices with $F_{16}CuPc$ trapped electrons alone due to abundant electron density. All the devices exhibited large memory window, long charge retention time, good endurance property and excellent flexibility. The obtained results have great potential for application in large area flexible electronic devices.

The next-generation electronic systems are expected to be light, flexible and portable for applications in integrated circuits (ICs), organic light emitting diodes (OLEDs), solar cells, radio frequency identification (RFID) tags and so on[1–9]. Memory is an essential part of electronic systems for data processing, storage and communication; however, currently available inorganic memories are not compatible with flexible substrates. Thus new approaches to develop flexible memory are necessary to realize large area flexible electronics. Tremendous efforts have been made towards developing high-density, high-speed and nonvolatile memory devices[10–15]. Among many types of nonvolatile memory, transistor-based flash memory with nano-segmented floating gate architecture have attracted huge interest due to the massive memory capacity and advanced fabrication technology[16]. The stored charges are located in the potential well of the blocking and tunnelling dielectric layers, resulting in nonvolatile memory operations. If the charge storage layers are made up of thin films, any dielectric defects would leak the stored charges and degrade the retention property of the device. Therefore, a monolayer consists of well-separated nanoparticles could be a best choice to store the charges. On this regard, multidisciplinary efforts have been taken in recent years to fabricate metal nanocrystal based floating gate layer, including thermal evaporation[17,18], electrostatic self-assembly[19,20], micro-contact printing[21] and synthesis in block copolymer[22,23]. However, nanoparticle assembly and morphology of the nanoparticle film should be controlled carefully to avoid nanoparticle-to-nanoparticle charge tunnelling. One solution to the problem is to utilize alternate charge storage elements with high charge-carrier binding energies and large area densities. Molecular materials, which are on the order of nanometer or even sub-nanometer in size, represent such idealized candidates with high charge density storage sites[24]. Among them, C_{60}, the most common buckyball clusters in fullerene family, are of great interest due to their potential applications in electronic devices using their semiconducting features[25,26]. Most of the reports on C_{60} are based on time-consuming vacuum sublimation process, which is not compatible with large area roll-to-roll fabrication method[27]. A facile solution processing method to obtain the floating gate layer should be favorable for technological applications. C_{60} derivatives have gained a lot of attention in transistors, photovoltaic devices and memory cells due to their high solubility in organic solvent[28–33]. However, the synthesis of C_{60} derivatives are still complicated and expensive; meanwhile their electronic performances are not as good as pristine C_{60}[34]. Pristine C_{60} is reasonably soluble in organic solvents which could pave a way for solution processed molecular gated flexible flash memories. The preparation of defined density of molecular charge trapping elements via simple solution process remains challenging.

In this work, we demonstrate a simple approach for the preparation of C_{60} molecular floating gate layer on a flexible substrate. The coverage of the molecular floating gate or the density of molecular charge trapping layer is facilely controlled by spin-coating method in a single step. We systematically study the charge trapping mechanism of the C_{60} floating gate under ambient conditions. Flash memory transistors with air-stable p-type pentacene and n-type copper hexadecafluorophthalocyanine ($F_{16}CuPc$) as semiconductors have been fabricated. The pentacene device exhibited a memory window of 4 V with both hole and electron trapping ability, while the

$F_{16}CuPc$ device trapped electrons alone with a memory window of 2 V. All the devices exhibited charge retention larger than 10^4 s with good cell-to-cell uniformity. The electrical performances of all the devices are well-maintained even after 500 programming/erasing cycles and did not degrade substantially upon bending.

Results

Device struture and operation mechanism. The overall fabrication of the memory transistor is illustrated schematically in Figure 1a. Atomic layer deposited aluminum oxide (Al_2O_3) was selected as the blocking dielectric layer on top of the silver (Ag) gate electrode on flexible poly(ethylene terephthalate) (PET) substrate. The atomic layer deposition technique allows for a high quality, defect-free dielectric layer with good barrier properties at low substrate temperature. Al_2O_3 has been demonstrated as a promising high-k dielectric candidate to minimize gate leakage current and achieve low voltage operation in thin film memory transistors[35–38]. C_{60} was spin-coated over the Al_2O_3 and then thermally annealed at 120°C for 10 min. A thin layer of poly(4-vinylphenol) (PVP) was then spin-coated onto the C_{60} layer using orthogonal solvents in order to prevent the dissolution of the C_{60} layer. A detailed description of the fabrication process is given in the experimental section. PVP possesses high resistivity and thermal stability, and has been demonstrated as a good polymer dielectrics[19]. In our designed dielectric system, PVP has relatively low dielectric constant (4.7) compared with Al_2O_3 (7)[39,40]. According to the equation $E_1 = V_g/(d_1 + d_2(\varepsilon_1/\varepsilon_2))$, where ε_i are the dielectric constants and d_i are the thicknesses of the two dielectric layers, the applied electrical field in PVP layer (E_1) is relatively stronger than in Al_2O_3 layer. Therefore, this system enables efficient charge transfer from the semiconductor layer to charge trapping layer through the tunnelling dielectric layer. Due to their good stabilities in ambient, pentacene and $F_{16}CuPc$ were chosen as the p-type and n-type semiconductor to investigate the charging mechanism of the C_{60} floating gate layer. Figure 1b illustrates the chemical structures of the organic small molecular materials used in this study. Figure 1c displays the atomic force microscopy (AFM) image of the C_{60} film spin-coated at 1000 rpm. The C_{60} film exhibited a surface morphology of separated islands, which is favorable for charge storage. The surface morphology of the C_{60} film spin-coated through high speed is also analyzed and shows relatively low densities (see supporting information Figure S1). Previous studies have shown that the memory capacity is dependent on the charge trapping element density, while the memory window increases with enhanced trapping sites[36]. Therefore, unless otherwise mentioned, all the memory devices are based on a C_{60} layer resulting from the low spin-coating speed (1000 rpm).

Electrical performance of p-type memory device. To investigate the trapping capability of C_{60} in the p-type memory device, we first fabricated a transistor with pentacene as the semiconductor layer. The schematic representation of the tunnelling of charge carriers in pentacene device is illustrated in Figure 2a. The holes are tunnelled through the PVP layer from the highest occupied molecular orbital (HOMO) of pentacene to C_{60} layer while electrons are tunnelled from the lowest unoccupied molecular orbital (LUMO) of pentacene to C_{60} trapping layer. It should be noted that intrinsic hole density is higher than electron density in pentacene[41,42]. Figure 2b shows the electrical characteristics of the pentacene memory device before and after applying the negative gate pulses (−5 V for 100 ms). The electrical properties were found to be uniform by examining different devices. The memory transistors show a hole mobility of about 5×10^{-2} cm^2 V^{-1} s^{-1} and current on/off ratio of about 10^3 while the transistors without C_{60} possess a mobility of about 0.1 cm^2 V^{-1} s^{-1}. The slightly decreased mobility can be attributed to the increased surface roughness when introducing the C_{60} layer under PVP. The applied electrical field is about 1.1 MV/cm in the tunnelling PVP layer, which is appropriate for efficient charge injection. The high mobility of C_{60} can guide fast charge distribution and assist the charging process when the charge injection is non-uniform across the C_{60} layer. The trend of the transfer curves reveals a typical hole trapping behavior indicating holes are injected from pentacene channel into C_{60} Layer through PVP by the application of

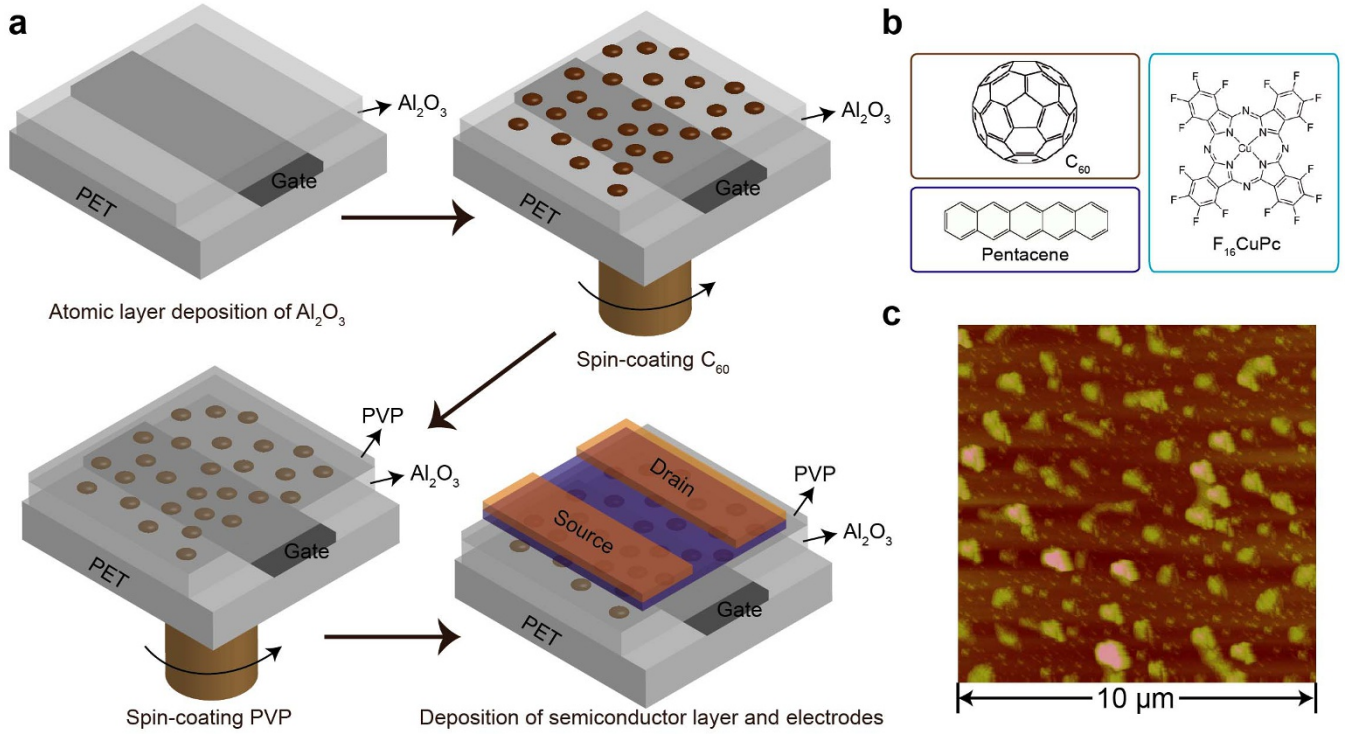

Figure 1 | (a) Schematic diagram depicting the basic fabrication process of the molecular floating gate memory device. (b) Chemical structure of the molecules. (c) Tapping-mode AFM image of the C_{60} layer.

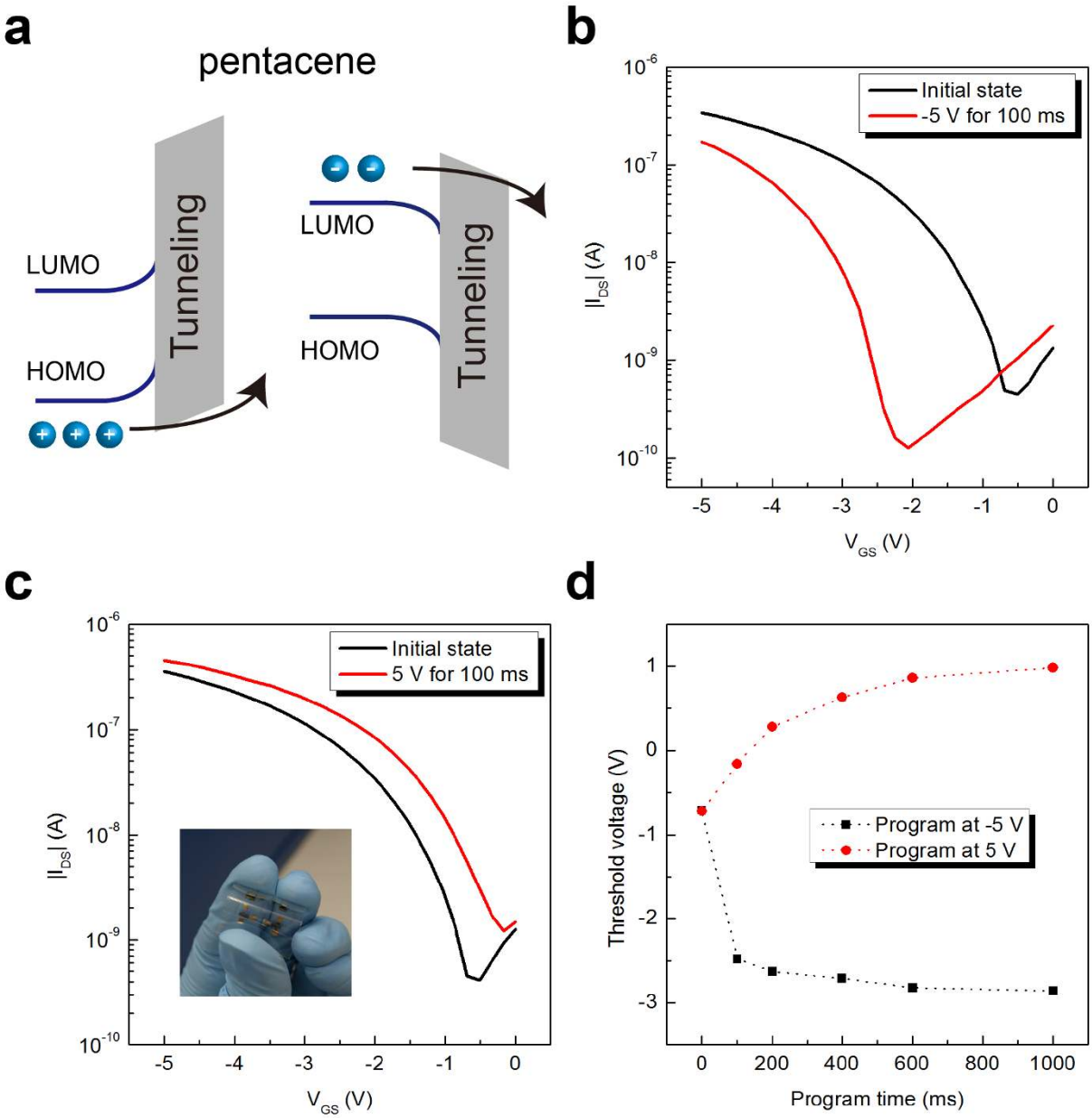

Figure 2 | (a) Energy band diagram of the pentacene based memory device. (b) Transfer characteristics of the memory transistor before and after negative gate bias. (c) Transfer characteristics of the memory transistor before and after positive gate bias. Inset: Optical imgae of the flexible memory device. (d) Threshold voltage with respect to the gate bias time.

the electric field. The trapped holes in C_{60} layer screened the channel and resulted in decreasing the effective gate electric field. In order to analyze the charging effect of the dielectric system, we also fabricated the device without C_{60} layer (see supporting information Figure S2). Almost negligible charging and discharging is observed in PVP/Al_2O_3 stack layers, therefore the charge carriers should mostly be trapped in C_{60} Layer. The electrical characteristics of the memory devices before and after applying the positive gate pulses (5 V for 100 ms) are shown in Figure 2c. The results indicate that electron trapping also occurs using C_{60} as the floating gate. In addition, pentacene has instrinsic electron mobility which makes them available to be trapped. This observation is interesting as most of the flash memory devices are based on single charge carrier trapping mechanism[17,43]. At the same electrical field, the amount of stored holes is more than the electrons according to the equation $Q = C \times \Delta V_{th}$ where Q is the stored charges, C is the capacitance of the dielectrics and ΔV_{th} is the threshold voltage shift. The V_{th} as a function of bias time is summarized in Figure 2d. The V_{th} shift increases with increased programming operation time, both in hole and electron charging process. Furthermore, V_{th} reach certain saturated values after long bias time, which is similar with metal nanoparticle floating gate memory[21,44]. During the charging process, the charge carriers (holes or electrons) trapped in the C_{60} layer can increase the capacitive coupling effect thus limited amount of trapped charge carriers are available at certain gate bias. In addition, the saturation rate of hole trapping process is observed to be quicker than electron trapping process. This may be attributed to the high hole mobility than electron mobility in pentacene[45].

With the property of trapping both holes and electrons, the memory window of the pentacene devices could be further enhanced. Figure 3a and 3b show the electrical characteristics of the two states (The state after positive gate bias 5 V for 1 s is denoted as ON state and the state after negative gate bias −5 V for 1 s is denoted as OFF state). The memory window (V_{th} shift) can reach about 4 V and the

maximum ON/OFF current ratio is about 1.5×10^3. This result is better than previously reported low voltage memory with conventional charge trapping layers such as evaporated metal layer and self-assembled nanoparticles[20,35]. It should be noted that the memory window depends strongly on the applied gate bias and lager bias could lead to larger memory windows[21]. Here we kept the applied voltage not exceeding 5 V to ensure the low voltage operation of the memory. The operation mode of the memory transistor has been reproducibly and reversely switched from one state to another state. The endurance properties of the pentacene device were studied by repeated application of gate bias pulses of ±5 V. Figure 3c illustrates the pulse sequence in the test. The ON and OFF state is well maintained for more than 500 cycles as shown in Figure 3d. In addition, we performed the data retention experiment on the devices and Figure 3e illustrates the test pulse sequence. In between the different measurement points, the devices are kept without applying any gate biases. The retention capability is shown in Figure 3f. The memory window is maintained at 82.1% for 10^4 s, which is comparable with previously reported low voltage organic memory devices[3,20,35]. In our device, the high energy barrier height of C_{60} surrounded by PVP suppresses the charge transport between each C_{60} island. At the same time, charge leakage from C_{60} to the semiconductor channel is effectively prohibited by the PVP tunnelling layer[46–48]. Therefore, the charge carriers (holes and electrons) are confined at the C_{60} floating gate[49]. Overall, both the positive part and negative part of the memory windows are suitable for the use as nonvolatile storage media.

Electrical performance of n-type memory device. We further explore the trapping capability of C_{60} in n-type memory device, in which $F_{16}CuPc$ is selected as the semiconductor layer. Figure 4a depicts the energy band diagram of charge carrier tunnelling in $F_{16}CuPc$ based device. Figure 4b shows the electrical characteristics

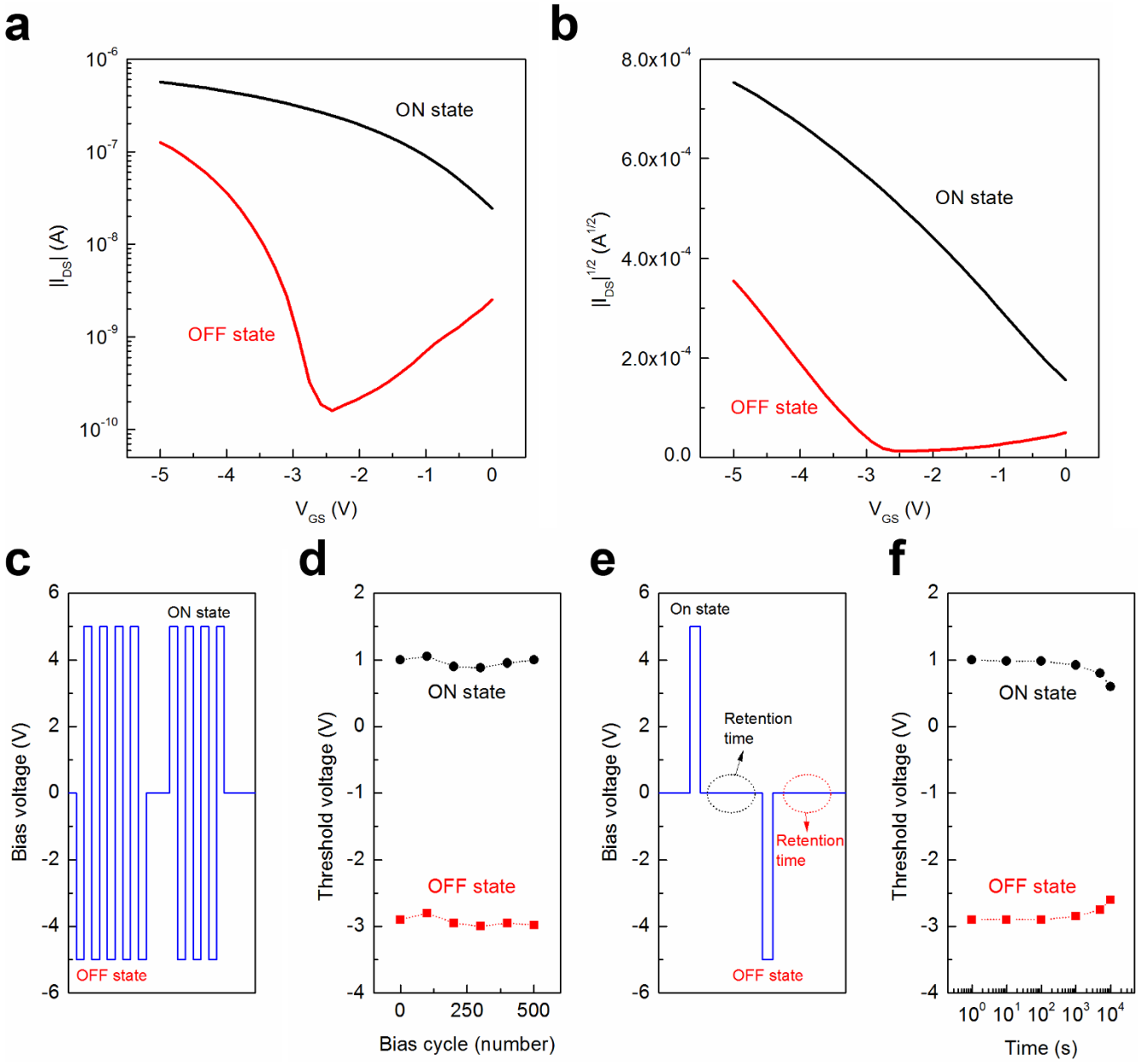

Figure 3 | (a) Transfer curve ($I_{DS} - V_{GS}$) of the pentacene memory at ON and OFF state on log scale. (b) Transfer curve ($|I_{DS}|^{1/2} - V_{GS}$) of the pentacene memory at ON and OFF state on linear scale. (c) Test pulse sequence for the endurance test. (d) Endurance characteristics of the pentacene device as a function of bias cycles. (e)Test pulse sequence for the retention test. (f) Data retention capability as a function of time.

of $F_{16}CuPc$ memory device before and after applying a positive gate pulse (5 V for 100 ms). The electrons tunnelled from $F_{16}CuPc$ channel into the C_{60} Layer through PVP, resulting in a decreased effective gate electrical field. Such a destructive electrical field leads to a reduced channel conductance, and the transfer curves shift towards the positive direction. The $F_{16}CuPc$ device without C_{60} layer is also fabricated and almost no charging effect of the dielectric system is observed (see supporting information Figure S3). The memory transistors show an electron mobility of about 1.8×10^{-3} cm^2 V^{-1} s^{-1} and current on/off ratio of about 10^2 while the $F_{16}CuPc$ transistors without C_{60} show a mobility of about 3×10^{-3} cm^2 V^{-1} s^{-1}. Further applying a negative gate pulse (−5 V for 100 ms) do not induce a negative shift of the transfer curves, which might be originated from the extremely low hole mobility of $F_{16}CuPc$[50]. It is understood that available minority carrier (hole) density in $F_{16}CuPc$ is much lower than the minority carrier (electron) density in pentacene. Therefore, we found both electron and hole trapping in pentacene based devices where as only electrons are trapped in $F_{16}CuPc$ based devices. The V_{th} with respect to the bias time is summarized in Figure 4d. The V_{th} shift towards more positive direction with prolonged bias, suggesting that additional charge carrier is brought to the molecular floating gate with increased bias time. The saturated level is also be observed here, demonstrating both trapped holes and electrons would cause capacitive coupling in the C_{60} floating gate.

Figure 5a and 5b show the electrical characteristics of the $F_{16}CuPc$ memory device at two states (The high conductance state is denoted as ON state and the low conductance state is denoted as OFF state). The memory window is about 2 V and the maximum ON/OFF current ratio is about 7×10^2. Continuous application of gate bias pulses of ±5 V for 1 s is carried out to measure the endurance properties as illustrated in Figure 5c. The ON and OFF state has been well maintained for more than 500 cycles as shown in Figure 5d. The test pulse sequence for the data retention test in $F_{16}CuPc$ device is illustrated in Figure 5e. The ON state and OFF state is well separated with respect to the elapsed time as shown in Figure 5f. About 19.2%

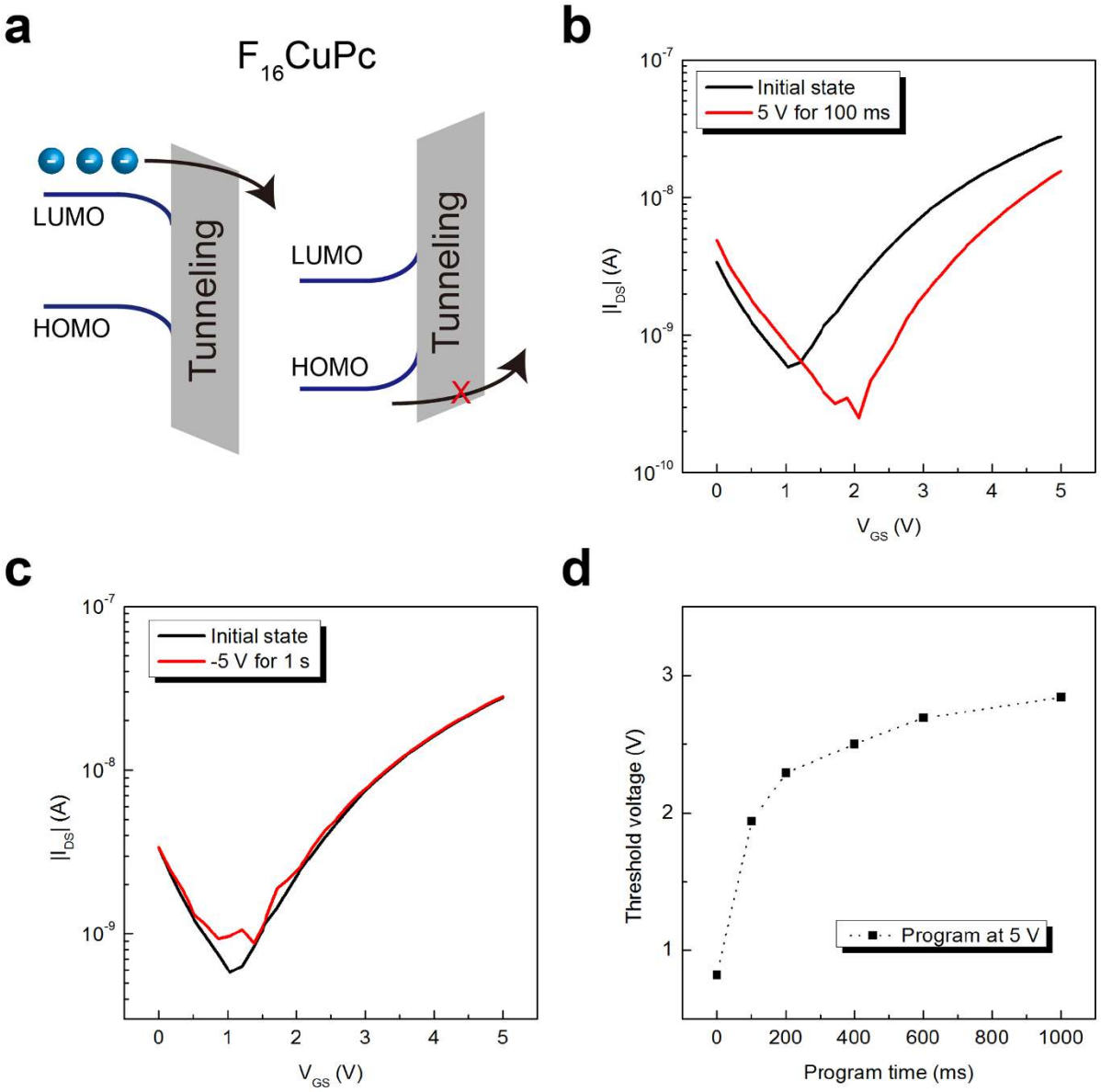

Figure 4 | (a) Energy band diagram of the $F_{16}CuPc$ based memory device. (b) Transfer characteristics of the memory transistor before and after positive gate bias. (c) Transfer characteristics of the memory transistor before and after negative gate bias. (d) Threshold voltage as a function of the gate bias time.

of the memory window is lost after a retention time of 10^4 s. The storage ability of the memory is comparable to recently reported memory devices based on n-type semiconductors[51,52].

Bending stability of the memory devices. In addition to the reliable memory operations, the bending stability is another important parameter to examine the reliability of the flexible devices. The organic/inorganic bilayer dielectric structure used in our device can reduce the possibility of cracking or delamination during repetitive bending[53]. Flexibility tests using cyclic bending were performed both in tensile and compressive mode with a bending radius of 10 mm. Figure 6a shows the schematic diagram of the bended device in a compressive state and Figure 6b illustrates the tensile state. The strain can be estimated from the equation D/2R, where D is the thickness of the substrate and R is the bending radius[54]. The bending tests were done up to 500 times to confirm the flexibility of both the pentacene and F_{16}CuPc devices. Figure 6c and 6d show the memory window as a function of compressive bending cycles. Figure 6e and 6f show the memory window as a function of tensile bending cycles. These results confirm that all the devices exhibit stable programmable properties with good mechanical flexibility.

Discussion

The high mobility of C_{60} can guide fast charge distribution and assist the charging process when the charge injection is non-uniform across the C_{60} layer. For the pentancene based p-type semiconductor devices, the trend of the transfer curves shows a typical hole trapping behavior indicating holes are injected from pentacene channel into C_{60} Layer through PVP by the application of the electric field. Due to intrinsic electron mobility as minority carriers, electron trapping also occurs using C_{60} as the floating gate in pentacene based devices. In

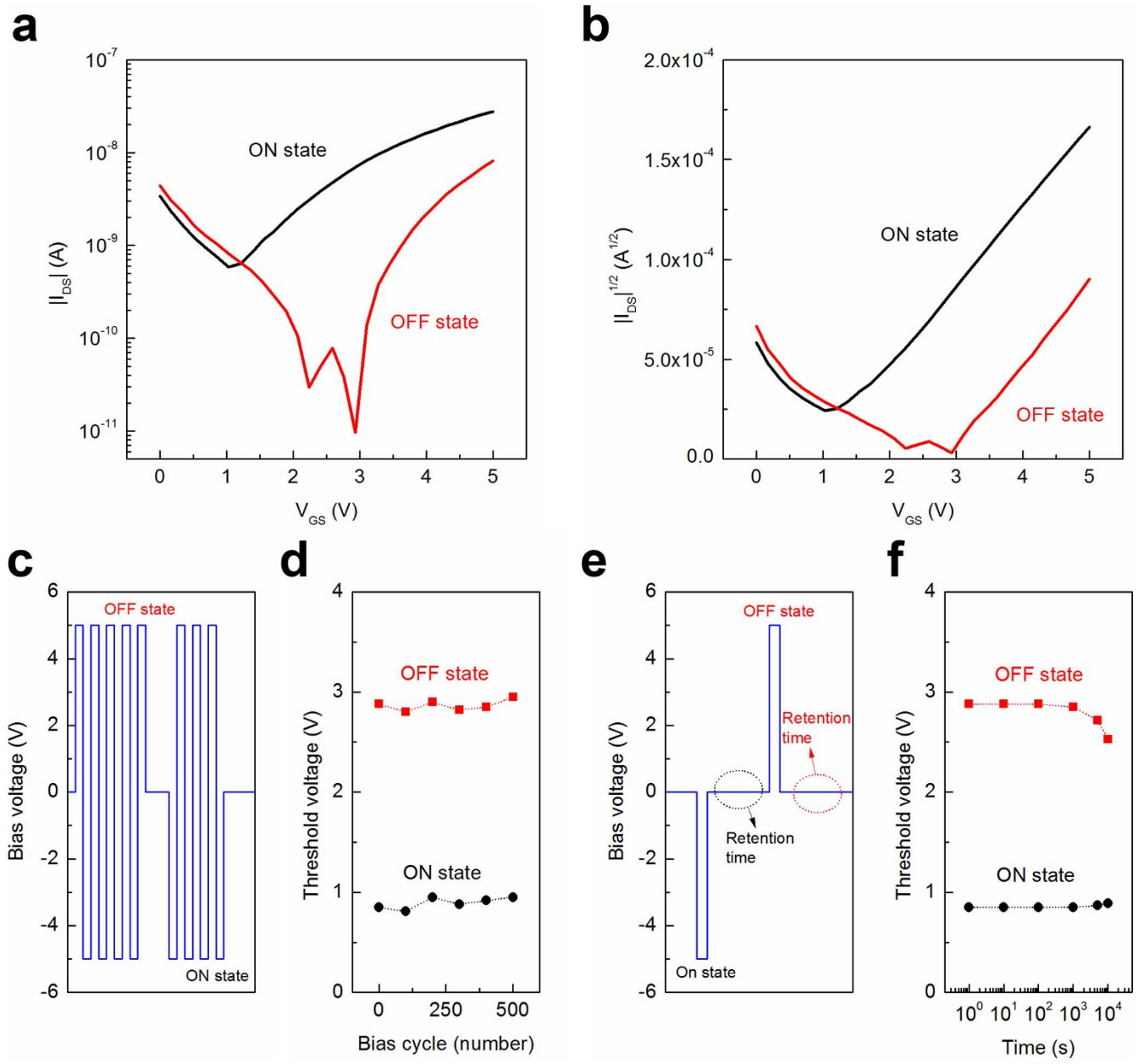

Figure 5 | (a) Transfer curve ($I_{DS} - V_{GS}$) of the F_{16}CuPc memory at ON and OFF state on log scale. (b) Transfer curve ($|I_{DS}|^{1/2} - V_{GS}$) of the F_{16}CuPc memory at ON and OFF state on linear scale. (c) Test pulse sequence for the endurance test. (d) Endurance characteristics of the F_{16}CuPc device with respect to the number of bias operations. (e)Test pulse sequence for the retention test. (f) Data retention capability with respect to the elapsed time.

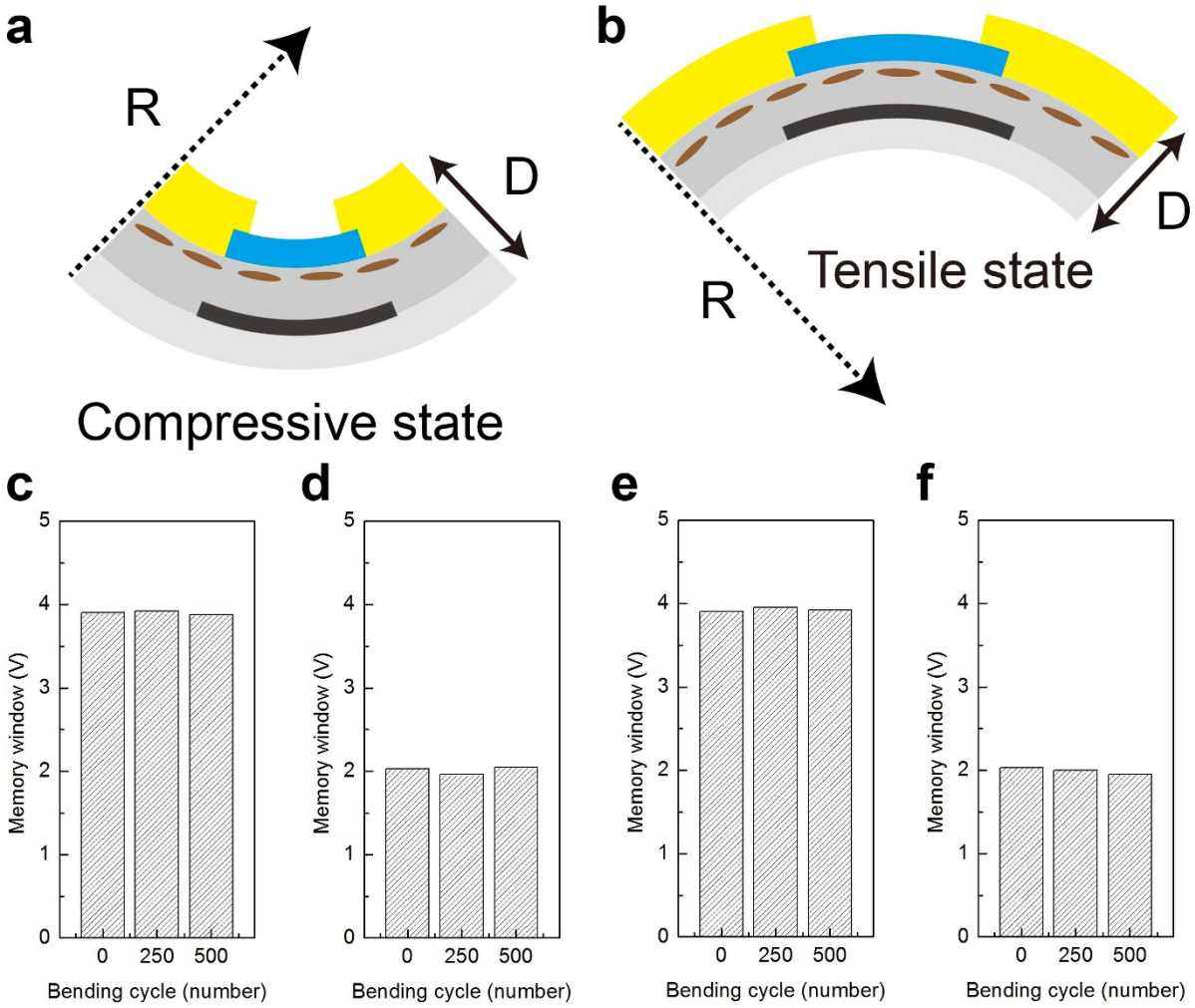

Figure 6 | (a) Schematic illustration of the device at compressive state. (b) Schematic illustration of the device at tensile state. (c) Memory window of the pentacene device with respect to compressive bending cycles. (d) Memory window of the $F_{16}CuPc$ device with respect to compressive bending cycles. (e) Memory window of the pentacene device with respect to tensile bending cycles. (f) Memory window of the $F_{16}CuPc$ device with respect to tensile bending cycles.

addition, due to the high intrinsic hole mobility of holes than electrons in pentacene, the saturation rate of hole trapping process is observed to be quicker than electron trapping process. For the pentacene based devices, both the positive part and negative part of the memory windows are suitable for the use as nonvolatile storage media. On the other hand, for the devices based on n-type semiconductor $F_{16}CuPc$, available minority carrier (hole) density is much lower than the minority carrier (electron) density in pentacene. Therefore, only electrons are trapped in $F_{16}CuPc$ based devices. The electrons tunnelled from $F_{16}CuPc$ channel into the C_{60} Layer through PVP, resulting in a decreased effective gate electrical field which leads to a reduced channel conductance, and the transfer curves shift towards the positive direction. During the charging process, due to the increased capacitive coupling between the trapped charge carriers (holes or electrons) in the C_{60} layer limited amount of trapped charge carriers are available at certain gate bias for both pentacene and $F_{16}CuPc$ based devices.

Although metal nano-floating gate have been widely investigated as the charge trapping layer in flash memories, they are still suffering from poor processability to implement them in printing technology. The solution processed molecular materials should be a choice for large area printable electronics. On the other hand, unlike conventional metal or metal nanoparticle based memory device, the trapping capability of C_{60} will be of great importance to realize functional nonvolatile memory. Since molecular materials can be functionlized to obtain multifunctional properties, it is important to understand the working mechanism of such molecular floating gate devices. The C_{60} floating gates showed ambipolar trapping behavior in the pentacene based memories and unipolar trapping behavior in the $F_{16}CuPc$ based memories. The approach to trap both holes and electrons in memory devices is an important to achieve large memory window and other electrically variable properties.

Our fabrication methods including the fabrication of C_{60} molecular floating gate layer and PVP tunneling dielectric layer are solution-processed. The simplified fabrication steps and low temperature processing method is quite promising for flexible electronics. The sucessful adopting of this structure on flexible substrates demonstrates that this method is mass-producible to construct innovative large area electronics.

In conclusion, we have demonstrated that solution processed C_{60} could be an excellent candidate for molecular floating gate in flexible flash memories. By adopting C_{60} as the charge trapping layer in both pentacene and $F_{16}CuPc$ memory transistors, reliable p-type and n-type memory devices has been achieved. All these devices show large memory window, long retention time, good endurance properties and excellent mechanical flexibilities. More importantly, our results

show that the use of molecular floating gate for the realization of new organic flash memory devices offers a promising route for the future development of advanced organic electronics.

Methods

Materials. PVP (average Mw ~25,000), C_{60} (99.5%), pentacene (sublimated grade) and $F_{16}CuPc$ (sublimated grade) were purchased from Aldrich. PET substrates were cut from commercially available PET films. All chemicals and solvents were used without further purification in the experiment.

Device fabrication. PET substrate was cleaned in an ultrasonic bath with detergent, acetone, and isopropanol prior to processing. 20 nm Ag film was thermally evaporated as the gate electrode. 40 nm Al_2O_3 layer was deposited using a Savannah 100 ALD system at a substrate temperature of 80°C. C_{60} was dissolved in 1,2,4-trichlorobenzene (TCB) (10 mg ml^{-1}) and spin-coated at different speeds on the Al_2O_3 layer with subsequent annealing for 10 min at 120°C in a nitrogen environment. After that, the PVP film was fabricated by spin-coating the prepared solution (5 mg ml^{-1} in isopropanol). The resulted film was annealed at 100°C for 1 hour in a vacuum oven and the thickness was about 20 nm. 40 nm pentacene or 25 nm $F_{16}CuPc$ were thermally deposited as the semiconductor layer at a rate of 0.1 to 0.2 Å s^{-1}. The substrate temperature was always kept at room temperature when depositing the p-type and n-type semiconductor films. Gold (Au) electrodes were employed as the source and drain contacts for both p-channel and n-channel memory transistors. 40 nm Au films were thermally evaporated through a shadow mask at a rate of 0.2 Å s^{-1}, with a channel length to channel width ratio of 50 μm/1000 μm.

Characterization. The morphology of the C_{60} layer was investigated by AFM (Veeco Multi mode). The thicknesses of the deposited films were measured by an ellipsometer. The electrical characteristics of the memory transistors were measured using a Keithley 2612 source meter. All measurements were conducted in atmospheric environment with a relative humidity of 60% and a temperature of 25°C.

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Author contributions

Y.Z. performed the experiments and wrote the paper. S.T.H., Y.Y., L.B.H., L.Z. and J.H. assisted with the experiments, discussed the results and commented on the manuscript. V.A.L.R. supervised the project and finalized the manuscript.

Additional information

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