Source Current Harmonic Analysis of Adjustable Speed Drives Under Input Voltage Unbalance and Sag Conditions

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***Abstract*—Adjustable Speed Drives (ASDs) have become the primary choice for most new and retrofit precision motor-control applications, offering major improvements in system efficiency. The significant increase in the use of ASDs makes it important to understand the compatibility issues between ASDs and their electrical environment in order to appropriately design the electrical systems. Even though there have been numerous studies addressing ASD effects on power systems, models for predicting the effect of the source voltage sags or unbalance have been limited. This paper is devoted to the analysis of utility-side input current harmonics under input voltage unbalance and sag conditions and the effects of these harmonics on the distribution transformer K-factor for practical ASD systems. The relationships between the unbalanced input voltages, the resulting input current harmonics, the input inductance, and the required transformer K-factor are explored for 5 hp, 100 hp, and 600 hp power distribution systems with ASDs. The results can be used as a design guide for power distribution system design with ASDs. Theoretical derivations are accompanied by both simulations and experimental results to provide verification of key conclusions.**

***Index Terms*—Adjustable speed drives (ASDs), crest factor, K-factor transformer, power factor, power quality, total harmonic distortion (THD), voltage unbalance and sag.**

I. Introduction

VARIOUS power quality problems and survey results in electrical distribution systems have been reported in [1]–[3]. Industries and businesses most commonly affected by these problems include: automobile manufacturing plants, medical centers, semiconductor plants, broadcasting facilities, and commercial buildings. It is estimated that industrial and digital economy companies collectively lose $45.7 billion a year to outages and another $6.7 billion each year to power quality phenomena [4]. Among the various power quality disturbances, voltage sags are considered to be the most frequent cause for process interruptions [5].

The principal cause of voltage sags is an increase in load current that may extend over a period of one cycle to a few hundred cycles of the ac source [6]. Such short-term increase in load currents may occur due to motor starting, transformer inrush, short circuits and fast reclosing of circuit breakers [7]. A significant proportion of voltage sags caused by short circuit events result in a transient voltage unbalance.

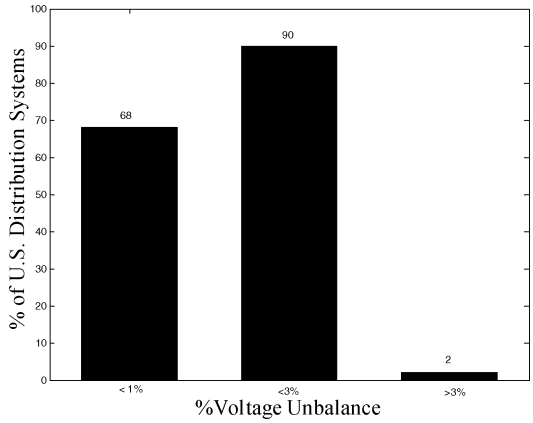

Fig. 1. Approximate voltage unbalance percentage in U.S. distribution systems.

In addition to voltage sags that are transient events, persistent voltage unbalance conditions also commonly appear in power distribution systems [8]. Fig. 1 illustrates field survey results of persistent voltage unbalances in U.S. distribution systems [9].

The objective of this paper is to quantify the effects of both short-term and long-term voltage unbalances on modern electronic loads such as ASDs. The current THD analysis in this paper applies to both voltage sags and persistent unbalance, while the K-factor analysis is only relevant when long-term voltage unbalance conditions exist.

There have been numerous papers describing the behavior of ASDs under input voltage unbalance and sag conditions. Several of the papers discuss the undesired resultant "tripping" of ASDs [6], [10], [11]. It has generally been known from tests and field experience that the three-phase diode bridge in a typical ASD often operates as a single-phase rectifier connected between the two lines with the highest voltage difference during voltage sag events. Test results from a 5 hp ASD presented in [8] indicates that raising the voltage unbalance from 0.6 to 2.4% causes the input current unbalance to increase from a nominal 13% to a maximum 52% [8].

Although these earlier papers present quantitative and empirical results for specific cases, they do not provide generalized techniques for quantifying the input power quality indices for practical ASD diode bridges. More specifically, the analysis in this paper is developed to accommodate arbitrary values of line

Manuscript received September 24, 2004; revised August 15, 2005. Paper no. TPWRD-00446-2004.

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Digital Object Identifier 10.1109/TPWRD.2006.871022

impedance and FINITE values of dc bus capacitance that include the effects of the resulting ripple in the dc link voltage.

In addition, the critical boundary conditions separating three-phase and single-phase operation of the rectifier bridge have not been evaluated in previous literature. The objective of this paper is to develop analytical techniques to determine the input current harmonic characteristics and the required transformer K-factor resulting from variable amplitudes of input voltage unbalance and different input inductance values for practical ASDs ranging from 5 hp to 600 hp.

Among the various power quality indices, K-factor is used as a measure of the additional losses attributable to harmonics and the resulting eddy current losses with 60 Hz excitation. K-factor is defined in Underwriters Laboratories Inc. standard UL 1561: "Dry-Type General Purpose and Power Transformers." It represents a derating factor for a transformer that indicates its suitability for use with loads that draw nonsinusoidal currents. It is particularly useful for specifying transformers that are connected to nonlinear loads such as ASD systems.

Transformers with K-factor ratings of 4, 7, 13, 20 and 30 are often available for ASD applications. Making the correct selection of the K-factor ensures appropriate safety levels while minimizing the overall system cost. Parameters that influence the required transformer K-factor include the input line inductance values, the dc bus capacitance value, the input voltage unbalanced amplitudes and phase angles, and the load conditions. Results presented in this paper will quantify the impact of these parameters on the transformer K-factor. More specifically, the theoretical model presented in the paper makes it possible to analyze the line source current harmonics to develop an accurate evaluation of the input current K-factor.

The theoretical model is verified using computer simulations of 5 hp, 100 hp, and 600 hp ASDs. Experimental verification results gathered from a 5 hp ASD system are also presented.

It is important to point out that single-phase operation caused by unbalanced voltage can seriously overload the diodes in the front-end rectifier stage. For example, the front-end diodes are already operating at their rated current levels when the ASD is delivering 50% rated power during single-phase rectifier operation [14]. Increasing the motor load above 50% under these input conditions creates risks of damage to these devices unless they are designed with extra margins in their current ratings. Since the focus of this paper is on the input current harmonics and resulting transformer K-factor rating, it will be assumed that the rectifier stage diodes have been selected with appropriate ratings to handle the increased currents during voltage unbalance operation.

II. Classification of Voltage Unbalance and Sags

Results from power quality surveys generally indicate that the most common voltage sags in three-phase power systems fall into the categories of type A, C and D [1], [7]. All three phase voltages drop in magnitude by the same amount for type A voltage sags.

On the other hand, the three phase voltages are not equal during either type C or D sags. Fig. 2 illustrates the three-phase voltage phasors under unbalanced conditions for types C and D sags. In this paper, the focus is on the effects of type D unbalance on the operation of a three-phase rectifier, although the analytical method presented here can be extended to study the effect of type C sags and unbalances as well. Detailed analysis and results for type C sags and unbalances can be found in [14].

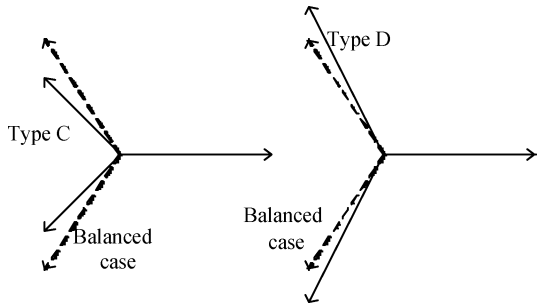

Fig. 2. Phasor diagrams of types C and D three-phase input voltage unbalances.

The severity of the voltage sag is defined through its "characteristic complex voltage," $\overline{V}$. The input phase voltage expressions for a type D sag can be expressed in terms of this characteristic complex voltage value as

$$\overline{V}_a = \overline{V} \quad [\text{pu}] \tag{1}$$

$$\overline{V}_b = -\frac{1}{2}\cdot\overline{V} - j\frac{\sqrt{3}}{2}\cdot\overline{F} \quad [\text{pu}] \tag{2}$$

$$\overline{V}_c = -\frac{1}{2}\cdot\overline{V} + j\frac{\sqrt{3}}{2}\cdot\overline{F} \quad [\text{pu}] \tag{3}$$

where $\overline{F}$ is known as the PN factor. Collected results from the field show that the amplitude of this PN factor $\overline{F}$ typically varies between 0.9 and 1.0 [1].

Although the classification based on the type of sag is useful in studying their effects on circuits, it is common to quantify the amount of unbalance using percentages. Applying the IEEE definition of phase-voltage unbalance in three-phase systems [15], the amount of voltage unbalance is expressed as

$$unbalance\% = \frac{|V_{avg} - V_\Phi|}{V_{avg}} * 100 \quad [\%] \tag{4}$$

$$V_{avg} = \frac{V_a + V_b + V_c}{3} \quad [\text{pu}] \tag{5}$$

where $unbalance\%$ represents the maximum phase voltage deviation from the average phase voltage amplitude, expressed in per cent. V_Φ is the maximum or minimum amplitude of the three input phase rms voltage amplitudes (V_a, V_b, V_c) while V_{avg} is the average voltage amplitude.

Having defined the particular type of sag to be studied, along with a measure for the amount of the sag, their effect on the operation of three phase passive diode bridge rectifier is presented further to evaluate worst-case operating conditions.

III. Theoretical Analysis of Worst Case Input Current Waveform Quality

A. Circuit Diagrams

Fig. 3 shows the schematic of a typical adjustable speed drive [16]. The three-phase ac input voltages are fed to a three-phase

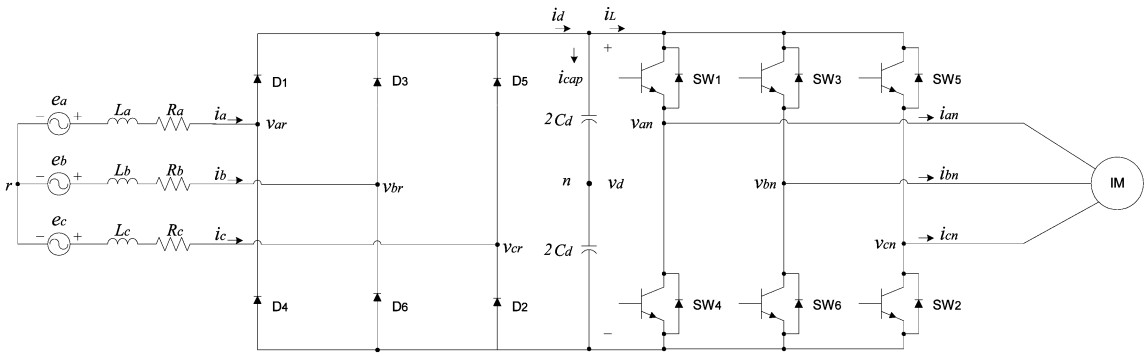

Fig. 3. Power circuit diagram of a typical ASD.

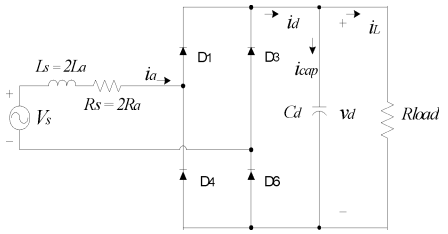

Fig. 4. Single-phase operation under input voltage unbalance and types C or D sag conditions.

diode (D_1-D_6) bridge rectifier through three ac line reactors L_a, L_b, and L_c that have series resistances R_a, R_b, and R_c, respectively. These impedances can be modeled to include the impedance of the ac line as well. The dc bus voltage is supported by dc bus capacitors represented by C_d. The PWM inverter uses IGBTs (SW_1-SW_6) to create three-phase ac voltage of variable frequency and magnitude that is delivered to the motor.

Under balanced line excitation conditions, the current waveforms drawn by the rectifier are symmetrical in all the three phases, although they may be rich in harmonics. The harmonic content of such waveforms is well known.

However, under types C and D voltage sag conditions, ASDs can easily transfer into the single-phase excitation conditions, even with a small amount of voltage imbalance. During types C and D voltage sags, the input line voltages have different amplitudes. The diodes in the front-end rectifier bridge only conduct to charge the dc bus capacitor bank when the input line-to-line voltage amplitude is higher than the dc bus voltage. As a result, the ASD enters single-phase operation when only four out of the six diodes conduct current during each cycle. The parameters affecting entry into single-phase operation will be discussed in the next subsection.

Under such single-phase operating conditions, the equivalent circuit for the three-phase rectifier can be reduced as shown in Fig. 4. Assuming that the input line impedances are balanced ($L_a = L_b = L_c$, $R_a = R_b = R_c$), then $L_s = 2 \times L_a$, $R_s = 2 \times R_a$ in Fig. 4. In the subsequent discussion and figures, V_s is the line-to-line voltage.

B. Boundary Conditions for Single Phase Conduction

It is important to identify the conditions when ASDs enter into single-phase operation during input voltage unbalance or sag events. This process can be rather complex because it involves interactions among all the following circuit quantities: the characteristics of the unbalance or sag events, input inductance, dc bus capacitance, and the load impedance.

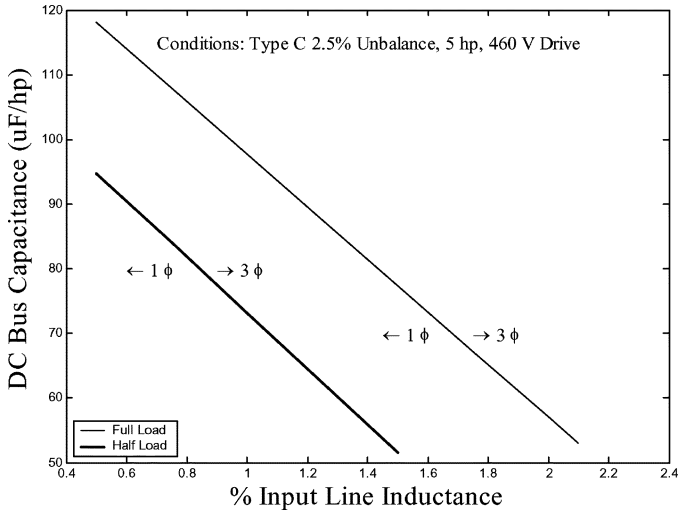

Fig. 5. Threshold boundaries between single- and three-phase operation for two load values (type C, 2.5% unbalance).

As an example, Fig. 5 provides the analytical results predicting the boundary conditions between three- and single-phase operation obtained using computer simulations for a 5 hp, 460 V ASD system. The voltage sag condition is type C with an rms unbalance of 2.5%. These results confirm that a small unbalance among the input voltages can result in single-phase excitation of the ASD.

Fig. 5 illustrates these trends: (a) Smaller line inductance or smaller dc bus capacitance lower the threshold for the ASD to enter into single-phase operation as the unbalance increases; and (b) a lighter load also encourages the ASD to transfer into single-phase operation with increases in unbalance. The boundary conditions for type D can be evaluated in the similar manner and exhibit similar trends.

C. Dynamic Solution of Input Currents

The equivalent circuit of the rectifier system under single-phase operating conditions with discontinuous conduction is illustrated in Fig. 4. Depending on the conduction state of the diodes, the circuit operation can be broken down further into four modes (a)-(d) as illustrated in Fig. 6. In mode (a), diodes

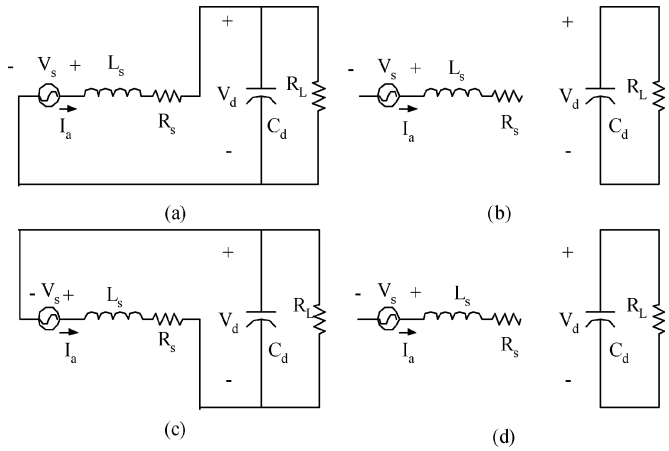

Fig. 6. Equivalent circuits of an ASD rectifier during single-phase operation during its four modes depending on the conduction state of the diodes.

D_1 and D_2 are conducting; in mode (c), diodes D_3 and D_4 are conducting. During modes (b) and (d), all of the diodes are in their off states. The circuit operation cyclically steps through these four modes (a)-(b)-(c)-(d)-(a)… in a sequential manner, driven by the periodic variation of the input ac voltage amplitude.

The input line current and the dc bus voltage react to the ac voltage amplitude and determine the instants at which the different operating modes begin and end. In particular, during modes (a) and (c), the system is governed by an energy exchange between the source, load, the inductor and the capacitor, and, hence, may be considered the power transfer interval. During modes (b) and (d), the energy stored in the capacitor is used to supply the load, corresponding to discharge intervals. Typical dc bus voltage and inductor current waveforms over an entire ac cycle are illustrated in Fig. 7. The power transfer interval may be defined to begin at the inception point (t_{in}), and end at the extinction point (t_{ex}).

In Fig. 4, when the pulsewidth-modulation (PWM) inverter is modeled as a resistive load, the dc bus current (i_d) and voltage (V_d) can be identified as state variables in a second-order system. As indicated in Fig. 6(a), circuit operation is governed by a second-order differential equation coupling the dynamics of the inductor current and the capacitor voltage, excited by the sinusoidal ac voltage waveform [16].

Figs. 6 and 7 show that the solution of the circuit operation needs to be developed for only one half cycle of the ac voltage waveform. The circuit solution developed for modes (a) and (b) can be readily extended to modes (c) and (d) through translations in time. During mode (b), the ac current is zero and the dc bus voltage follows a decaying exponential trajectory for which the time constant is defined by the load resistance and the dc bus capacitance. Therefore, the only remaining mode that needs to be solved is mode (a), as described below.

The dc bus voltage solution to the second-order differential equation for an under-damped system can be expressed as

$$V_d(t) = V_{pk}\{A\cdot e^{-t/\tau}\cdot\cos[\Omega(t-t_x)] + N\cdot\cos[\omega t-\phi)]\} \text{ [V]} \quad (6)$$

where τ is the equivalent damping time constant of the second-order system, ω is the ac excitation frequency, and Ω is

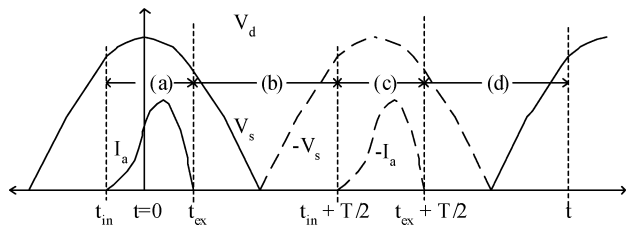

Fig. 7. Typical dc bus voltage and ac current waveforms during four operating modes of single-phase rectifier operation.

the equivalent damped resonant frequency of the second-order system. The first term in (6) represents the natural response of the second-order resonant circuit to a set of arbitrary initial conditions, and the second term in (6) represents the forced response of the circuit to the sinusoidal excitation. The values of A and t_x are determined to meet the initial conditions of the second-order circuit. The values of N and t_x are determined by solving the equivalent circuit at the excitation frequency. The resonant circuit quantities τ and Ω can be calculated as

$$\tau = \frac{2}{\frac{R_s}{L_s} + \frac{1}{R_L C_d}} \quad [\text{sec}] \quad (7)$$

$$\Omega = \sqrt{\frac{1+\frac{R_s}{R_L}}{L_s C_d} - \frac{1}{\tau^2}} \quad \left[\frac{\text{rad}}{\text{s}}\right] \quad (8)$$

The magnitude N and the phase delay ϕ caused by the forced excitation voltage acting on the voltage divider formed by the filter-load network can be determined as

$$N = \left| \frac{R_L \| \frac{1}{j\omega C_d}}{R_s + j\omega L_s + R_L \| \frac{1}{j\omega C_d}} \right| \quad (9)$$

$$\phi = \angle \left[\frac{R_L \| \frac{1}{j\omega C_d}}{R_s + j\omega L_s + R_L \| \frac{1}{j\omega C_d}} \right] \quad [\text{rad}] \quad (10)$$

For typical practical values of load resistance, line resistance, line reactance, and dc bus capacitance values as expressed in Fig. 5, the time constant τ is much larger than the half period of the ac waveform, and the damped resonant frequency of the second-order system is practically equal to the undamped resonant frequency of the LC circuit. Furthermore, the phase shift ϕ of the resonant network at the excitation frequency is practically zero. Under these conditions the following approximate solution can be developed:

$$V_d'(t) = V_{pk}\left[A\cdot\cos[\Omega'(t-t_x)] + N\cdot\cos\omega t\right] \quad [\text{V}] \quad (11)$$

$$\Omega' = \frac{1}{\sqrt{L_s C_d}} \quad \left[\frac{\text{rad}}{\text{s}}\right] \quad (12)$$

From examination of Fig. 7, it may be concluded that at the inception of mode (a), when $t = t_{in}$, the ac excitation voltage $V_s\cos(\omega t)$ is equal to the dc bus voltage. This forms one of the initial conditions to determine the amplitude A of the natural response, formulated as follows:

$$V_{pk}\cdot\cos\omega t_{in} = V_{pk}\left[A\cdot\cos[\Omega'(t_{in}-t_x)] + N\cdot\cos\omega t_{in}\right] \text{ [V]} \quad (13)$$

Furthermore, the inductor current is zero at the inception time instant. Thus, the capacitor current is equal and opposite to the

load current. This can be formulated as a second constraining initial condition as follows:

$$\frac{V_{pk}\cos\omega t_{in}}{\mathrm{R}_L} = V_{pk}\left[A\Omega' C_d \sin[\Omega'(t_{in}-t_x)] + N\omega C_d \sin\omega t_{in}\right] \text{ [A]} \quad (14)$$

Solving the trigonometric (13) and (14) together simultaneously, A and t_x are obtained as

$$A = \left|(1-N)\cos\omega t_{in} + \frac{j}{\Omega'}\left\{\frac{1}{R_L C_d}\cos\omega t_{in} - N\omega\sin\omega t_{in}\right\}\right| \quad (15)$$

$$t_x = \frac{1}{\Omega}\left[t_{in} - \angle\left((1-N)\cos\omega t_{in} + \frac{j}{\Omega'}\left\{\frac{1}{R_L C_d}\cos\omega t_{in} - N\omega\sin\omega t_{in}\right\}\right)\right] \text{ [sec]} \quad (16)$$

Using this expression, the solutions for the dc bus voltage V_d and current i_d for the under-damped second-order system can then be expressed as shown in (17) and (18) at the bottom of the page.

The closed-form expressions for the dc bus current i_d and voltage V_d can then be used to calculate key power quality indices including the total harmonic distortion of the input current and the transformer K-factor, as follows:

$$THD_i = \frac{\sqrt{\sum_{h\neq 1}^{h} I_h^2}}{I_1} * 100 \quad [\%] \quad (19)$$

$$K = \sum_{h=1}^{h=h_{\max}} I_h^2 \cdot h^2 \quad (20)$$

In the K-factor expression of (20), I_h is the rms current amplitude at harmonic order h represented in per unit of rated rms load current. More details about the K-factor can be found in UL 1561.

D. Theoretical Results

Applying the closed-form equations for the dc bus current i_d and voltage V_d from the previous section, detailed Fourier harmonic analysis of the input currents can be performed. The results are illustrated in more detail for a particular case consisting of 2.5% type D unbalance in the input voltage with 1% line inductance at 50% load. Modern ASDs available in the market have a typical dc bus capacitance between 75 and 360 μF/kW [10], or 56–268 μF/hp. A dc bus capacitance based on 66 μF/hp (i.e., 330 μF for the 5 hp ASD) is used in this analysis.

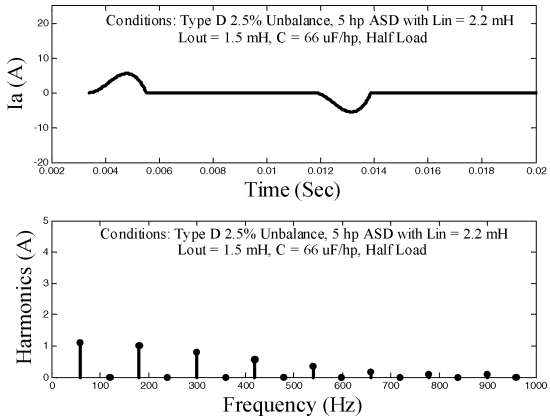

Fig. 8. A 5 hp input phase A current waveform and its harmonic spectrum during type D 2.5% unbalance conditions.

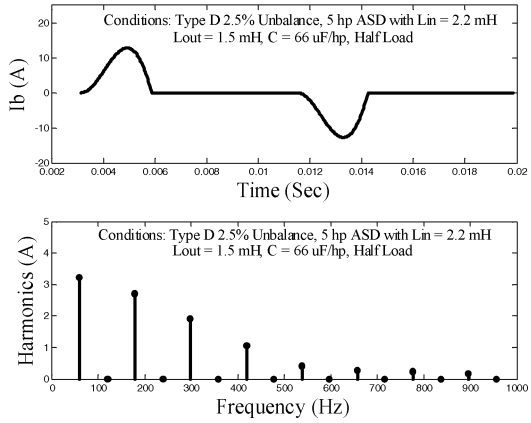

Fig. 9. A 5 hp input phase B current waveform and its harmonic spectrum for type D 2.5% unbalance conditions..

Figs. 8 and 9 show the input current waveforms in phases A and B and their harmonic spectra, respectively. The uncharacteristic triplen harmonics (3rd, 9th, etc.) are present under unbalanced input voltage conditions. Phases A and B under the type D unbalance are in single-phase conduction with unequal current amplitudes. The return path for the phase A and B currents is through phase C. There are two unequal peaks in the phase C current during each half cycle as will be apparent in both the simulation and experimental results.

Under these unbalanced operating conditions, the calculated input current total harmonic distortions (THD) values are 132.2% and 109.4% in phases A and B, respectively. The corresponding transformer K-factor values are 1.02 and 4.49.

In comparison, under balanced operating conditions, the three-phase bridge rectifier exhibits an input current THD of 58.1% [8]. Through computer simulation and analysis, the

$$V_d(t) = \begin{cases} V_{pk}[A\cos[\Omega(t-t_x)] + N\cos(\omega t)] & t_{in} < t < t_{ex} \\ V_d(t_{ex})\cdot e^{-(t-t_{ex})/C_{dc}R_L} & t_{ex} < t < t_{in} + \frac{T}{2} \end{cases} \text{ [V]} \quad (17)$$

$$i_d(t) = \begin{cases} 0, & 0 < t < t_{in} \\ -V_{pk}[A\Omega C_d \sin[\Omega(t-t_x)] + N\omega C_d \sin(\omega t)] + \frac{V_{pk}[A\cos[\Omega(t-t_x)] + N\cos(\omega t)]}{R_L}, & t_{in} \le t \le t_{ex} \\ 0, & t_{ex} < t < t_{in} + \frac{T}{2} \end{cases} \text{ [A]} \quad (18)$$

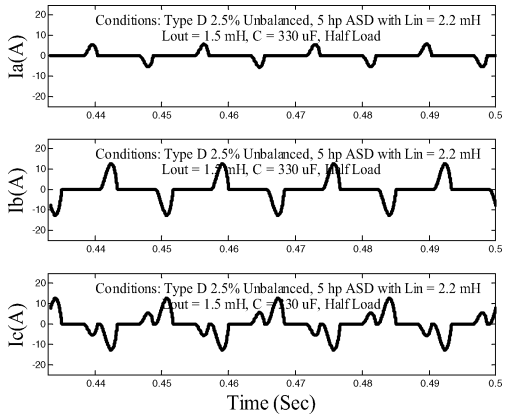

Fig. 10. A 5 hp ASD input phase current waveforms for Phase A, B, and C from top to bottom for type D 2.5% input voltage unbalance.

TABLE I
VARIOUS ASD SYSTEM INPUT CURRENT THD RESULTS COMPARISON. CONDITIONS: TYPE D, 2.5% INPUT VOLTAGE UNBALANCE, $L_a = 3\%$, 50% LOAD

THD_i	5 hp	100 hp	600 hp
Phase A	131.4%	94.32%	89.05%
Phase B	108.8%	93.83%	89.02%
Phase C	83.92%	73.62%	69.73%

input K-factor for the balanced case is 2.69 for all three phases. As indicated above, these power quality indices are degraded under input voltage unbalance and sag conditions.

IV. SIMULATION ANALYSIS

A detailed computer simulation of the system illustrated in Fig. 3 was developed in order to verify the analytical results and to evaluate the input current harmonic characteristics and the transformer K-factor for 5 hp, 100 hp, and 600 hp ASDs. Although the analytical models were developed on the basis of a resistive load, the simulation utilized the complete model of the inverter including the space vector pulse-width modulation (SVPWM) algorithm.

Computer simulation was carried out using the Simplorer [18] circuit simulator. The circuit parameters used in the simulation are $R_a = 10\ \mathrm{m}\Omega$, $L_a = 1\%$, 3%, and 5%, $C_d = 330\ \mu\mathrm{F}$, 3300 μF, and 19.8 mF for the 5 hp, 100 hp, and 600 hp systems, respectively. The input voltage unbalance amplitude is swept through 0.5%, 1%, 2%, 2.5%, and 5% for type D input voltage unbalance conditions.

A. Time-Domain Waveforms

Fig. 10 illustrates the three input phase current waveforms for the 5 hp ASD with a type D 2.5% input voltage unbalance at 50% load. With 2.2 mH input line inductance, ASD input phases A and B are in single-phase conduction operation (top two traces). The simulation waveforms agree with the theoretical results calculated in the last section. The phase C current provides the return path for both phases A and B. The THD and K-factor values for the three input phase currents are tabulated in Tables I and II.

Fig. 11 shows the input current harmonic spectra. It should be noted that current harmonic amplitudes are all expressed as

TABLE II
K-FACTOR RESULTS COMPARISON. CONDITIONS: TYPE D, 2.5% INPUT VOLTAGE UNBALANCE, $L_a = 3\%$, 50% LOAD

K-factor	5 hp	100 hp	600 hp
Phase A	1.05	3.79	2.91
Phase B	4.45	2.56	2.53
Phase C	5.48	5.37	4.40

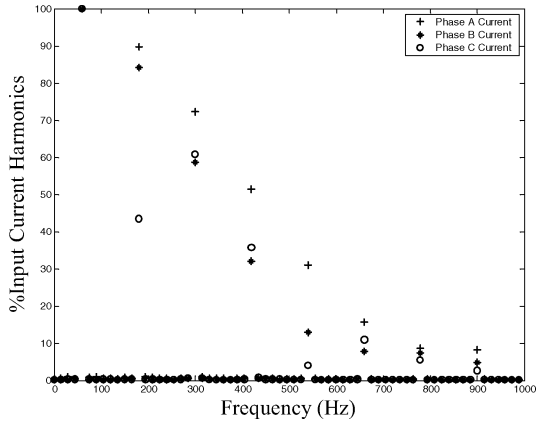

Fig. 11. A 5 hp ASD input phase current harmonic spectra for each of the three phases during type D 2.5% input voltage unbalance conditions.

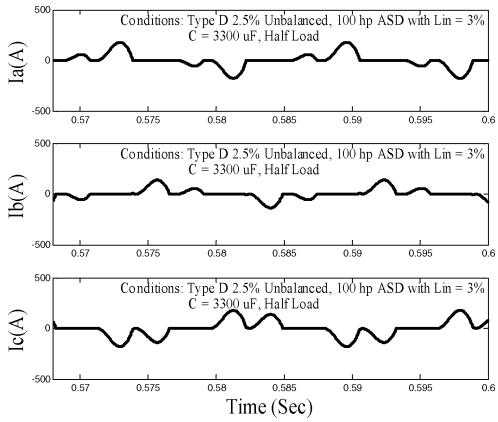

Fig. 12. A 100 hp ASD input phase current waveforms for Phase A, B, and C from top to bottom for type D 2.5% input voltage unbalance.

percentage values of the fundamental component in the same phase. The dominance of the third harmonic in all three phases can be clearly observed. The harmonic contents tend to be significantly higher for phases A and B which are operating in the single-phase conduction mode.

Fig. 12 illustrates the three ASD input phase current waveforms for a 100 hp, type D 2.5% input voltage unbalance at 50% load. With 3% input line inductance, phases A and B are near single-phase operation (top two traces). The THDs and K-factors for the three input phase currents are tabulated in Tables I and II.

Fig. 13 shows the input current harmonic spectra for the same operating conditions as in Fig. 12. Even though the 3rd harmonic component exists in all three phases, its peak value is less than that of the 5th harmonic component due to the fact that phases A and B have not completely entered the single-phase conduction mode.

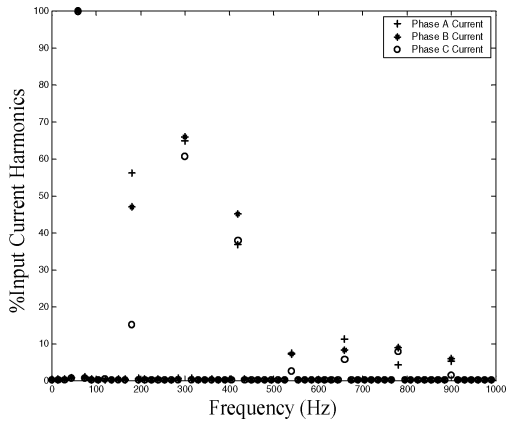

Fig. 13. A 100 hp ASD input phase current harmonic spectra for each of the three phases during type D 2.5% input voltage unbalance conditions.

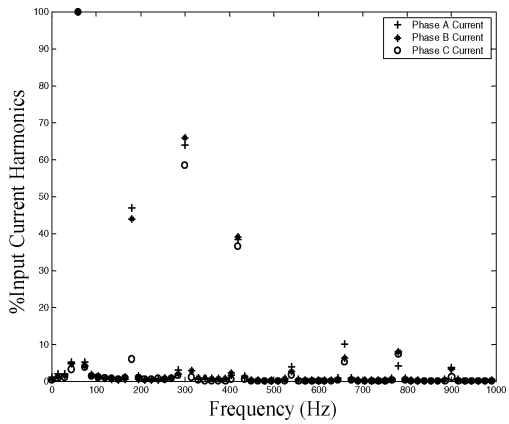

Fig. 15. A 600 hp ASD input phase current harmonic spectra for each of the three phases during type D 2.5% input voltage unbalance conditions.

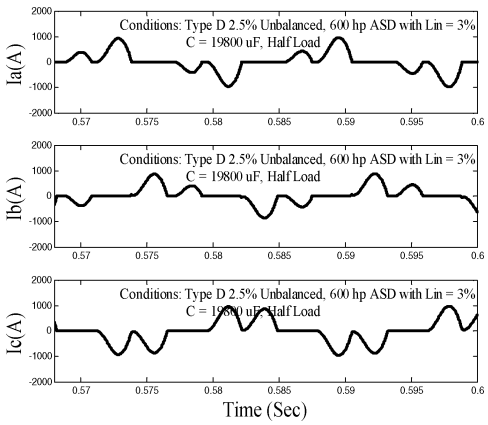

Fig. 14. A 600 hp ASD input phase current waveforms for Phase A, B, and C from top to bottom for type D 2.5% input voltage unbalance.

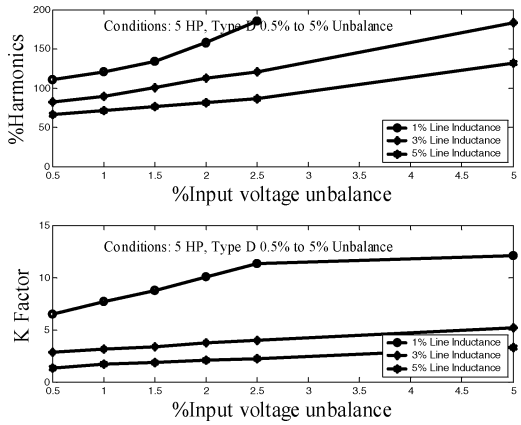

Fig. 16. Input phase current THD and K-factor versus input voltage unbalance and input inductance for a 5 hp ASD system.

Fig. 14 illustrates the three input phase current waveforms for a 600 hp, type D 2.5% input voltage unbalance at 50% load. With 3% input line inductance, phases A and B are no longer in single-phase operation (top two traces). The THDs and K-factors for the three phase currents are tabulated in Tables I and II.

Fig. 15 shows the input current harmonic spectra for the same conditions as in Fig. 14. The third harmonics exist in all three phases as long as the input voltages are unbalanced. The various harmonic values are lower than their counterparts in the 100 hp example, due partly to the fact that the 600 hp system has different line inductance and dc bus capacitance values. As a result, the dynamics of the system are changed according to the solutions in (9) and (10).

The three phase current THDs for 5 hp, 100 hp and 600 hp ASDs are summarized in Table I. Since the parameters of line impedance, dc bus capacitance and load conditions are different, the smaller hp ASD tends to have higher input current THDs. In all cases, the less continuity in phase C current results in a lower total harmonic distortion in that phase. The three phase currents have unequal RMS values, thus the K factors are not the same for all phases.

The transformer K-factors for 5 hp, 100 hp, and 600 hp ASDs are summarized in Table II. The three phase currents have unequal RMS values, thus the K-factors are not the same for all phases. The results show that the K-factor is not a function of power levels.

The studies in this paper not only apply to a single 100 hp or 600 hp ASD system, but are also valid for multiple ASDs totaling 100 hp or 600 hp in a power distribution network.

B. Trend Analysis

As type D input voltage unbalance is swept from 0.5% to 5%, the upper plot of Fig. 16 shows the highest input current THD values among the three input phases, with the input line inductance ranging from 1% to 5%, for a 5 hp ASD system. The highest current THD is always in phase A due to its severe discontinuity and lower amplitude. The phase A current finally extinguishes completely at 5% type D unbalance with 1% input inductance, while phases B and C are in single-phase conduction mode. These curves show that THD values tend to increase as the line inductance values decrease or the voltage unbalance percentage increases.

The lower plot of Fig. 16 shows the highest input distribution transformer K-factor value among the three phases as a function of the input voltage unbalance percentage for the 5 hp ASD system with three values of line inductance varying from 1% to 5%. The K-factor in each phase is different since the input voltage unbalance causes the input currents to become unbalanced. The K-factor is a strong function of input inductance

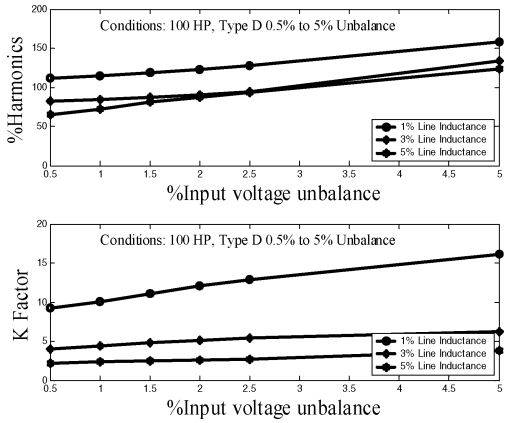

Fig. 17. Input phase current THD and K-factor versus input voltage unbalance and input inductance for a 100 hp ASD system.

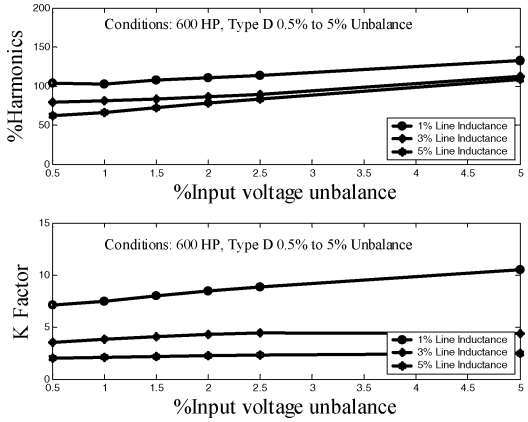

Fig. 18. Input phase current THD and K-factor versus input voltage unbalance and input inductance for a 600 hp ASD system.

values. The K-factor increases significantly as the input inductance value decreases.

As the type D input voltage unbalance is swept from 0.5% to 5%, the upper plot of Fig. 17 shows the highest input current THD value among the three input phases for a 100 hp ASD system, with the input line inductance ranging from 1% to 5%. The dc bus capacitance value is 3300 μF and the load is 50%. The gap between the input current THD values for the 3% and 5% line inductance traces is narrowed in comparison to the 5 hp case. The THD values with 1% input inductance are much higher.

The lower plot of Fig. 17 shows the highest K-factor value among the three input phases as a function of the input voltage unbalance percentage for the same 100 hp ASD system as the input line inductance varies from 1% to 5%. The K-factor values tend to increase for smaller input line inductance values. The K-factor is defined in such a way that it equals one for linear loads and it is as high as 16 in the studies here for the nonlinear ASD systems.

Fig. 18 shows the same two plots of input current THD and K-factor values as in Figs. 16 and 17 for the 600 hp ASD system. The 600 hp ASD parameters are the same as indicated earlier. The THD profiles for the 100 hp and 600 hp systems are very similar. Consistent with the results for the 5 hp and 600 hp

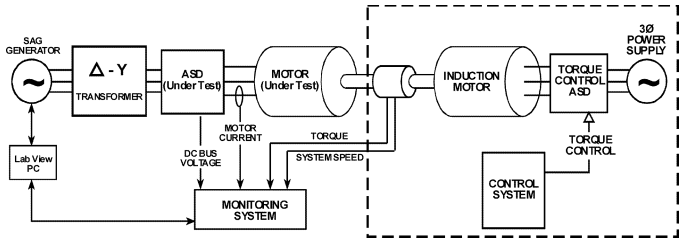

Fig. 19. Experimental test configuration.

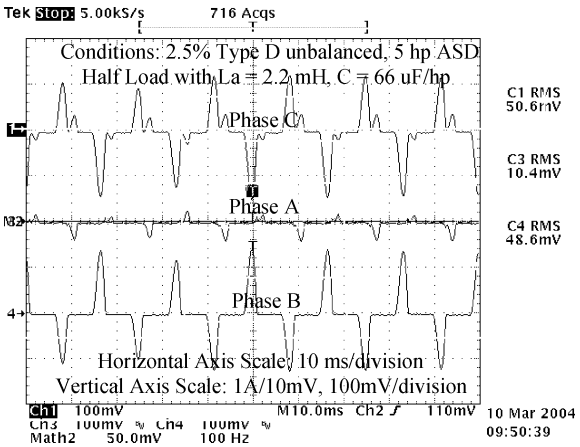

Fig. 20. Experimental waveforms of three input phase currents for a 5 hp ASD during type D 2.5% voltage unbalance conditions.

ASDs, the K-factor values are higher for smaller input line inductance case. Similarly, the K-factor values do not change significantly as the input voltage unbalance varies for the 3% and 5% line inductance cases.

V. Experimental Results

Within the range of the simulation conditions, the specific case consisting of a 2.2 mH input line inductance (1.5%) under 2.5% type D unbalanced input voltage conditions is verified experimentally using a 5 hp, 4-pole, 460 V, 60 Hz ASD and a dynamometer test bed. The test configuration is illustrated in Fig. 19, including a programmable voltage sag generator, a drive isolation transformer, the ASD under test, and a 5 hp induction machine. In addition, the dynamometer includes a load machine excited by a four-quadrant ASD, and a Labview-based computer system designed to provide data acquisition, monitoring, and control functions.

The 5 hp ASD system was operating under 50% load, as in the theoretical and simulation analysis. Fig. 20 provides the captured input three phase current waveforms under type D 2.5% input voltage unbalance conditions. As shown earlier in the theoretical and simulation analysis, phases A and B are in single-phase operation, while phase C provides the current return path for phases A and B currents.

The RMS values of phases A, B and C from the experiment current waveforms are 1.04 A, 4.86 A and 5.06 A, compared to 1.86 A, 4.79 A and 5.13 A in the simulation results for the 5 hp system under the same test conditions in Fig. 10. The agreement is generally very good, particularly for phases B and C.

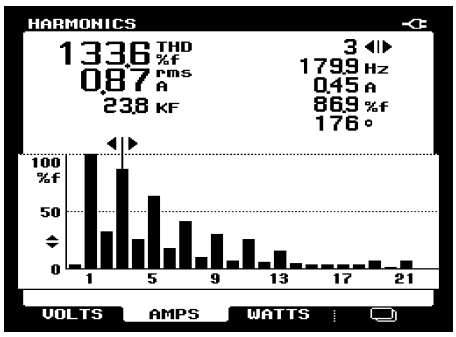

Fig. 21. Experimental spectrum of phase A input current and harmonic measurements for a 5 hp ASD during type D unbalance test.

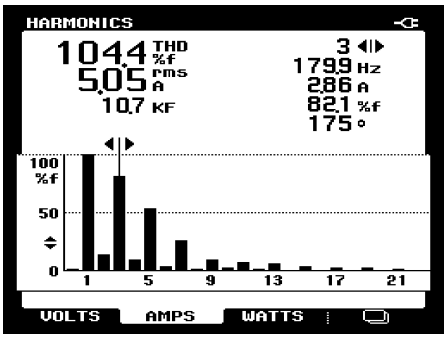

Fig. 22. Experimental spectrum of phase B input current and harmonic measurements for a 5 hp ASD during type D unbalance test.

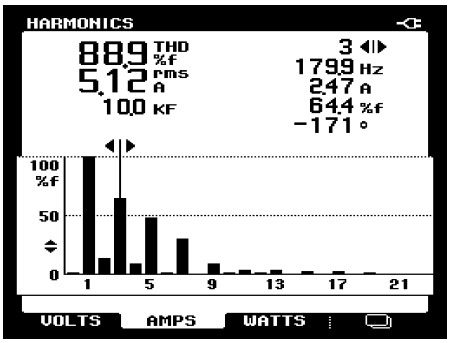

Fig. 23. Experimental spectrum of phase C input current and harmonic measurements for 5 hp ASD during type D unbalance test.

Figs. 21–23 present the harmonic spectra of the input currents and the total harmonic distortion (estimated using 21 harmonics) for phases A, B and C, respectively. The strong presence of the 3rd harmonic content in all three of the phase currents is clear from these spectra. Such uncharacteristic triplen harmonics can present problems in many field applications where only 5th and 7th harmonic filters are typically installed for power quality improvement.

A comparison of the input current THD obtained using theoretical analyzes, simulation results, and experimental measurements is presented in Table III. The measured input current THDs for the 5 hp ASD are in the good agreement with the theoretical analysis and the simulation results. No entry is made for phase C in the Theory column because it is not operating in true single-phase mode that was the basis for the theoretical calculations.

TABLE III
5 HP ASD SYSTEM INPUT CURRENT THD RESULTS COMPARISON. CONDITIONS: TYPE D, 2.5% INPUT VOLTAGE UNBALANCE, $L_a = 1.5\%$, 50% LOAD

THD_i	Theory	Simulation	Experiment
Phase A	132.2	131.4	133.6
Phase B	109.4	108.8	104.4
Phase C	-	83.9	88.9

Verification tests have not been performed for the 100 hp and 600 hp ASD systems. Nevertheless, the authors believe that the very good agreement between theoretical analysis, simulation, and experimental results for the 5 hp ASD provides a basis for confidence in the validity of the predicted results for the 100 hp and 600 hp ASD systems.

VI. CONCLUSIONS

Closed-form solutions for the ASD dc bus voltage and input ac line currents during unbalance or sag events have been used to critically evaluate the ASD performance in power distribution systems. The theoretical analysis in this paper is based on a practical ASD model with both finite line impedance and finite dc bus capacitance, avoiding simplifying assumptions of past investigations.

Complete ASD simulation models have been developed by implementing space vector pulse width modulation (SVPWM) for the inverter operation. Extensive simulations have been conducted for 5 hp, 100 hp and 600 hp ASDs in typical power distribution systems. Key effects on input current waveform qualities, harmonic distortion, and distribution transformer K-factors under input voltage unbalance and sag conditions have been investigated.

To verify the theoretical and simulation results, an experimental setup including a dynamometer and data acquisition system were established and the results have been presented for a 5 hp ASD system.

K-factor-rated transformers are units that have been designed with sufficient capacity to cope with the additional heating effect caused by the presence of harmonic currents. This paper has quantified the impact of voltage unbalance conditions on input current K-factor values in order to assist the selection of the proper transformers for cost and safety in ASD power distribution systems.

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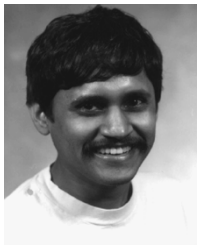

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