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Space charge limited conduction with exponential trap distribution in reduced graphene oxide sheets

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We elucidate on the low mobility and charge traps of the chemically reduced graphene oxide (RGO) sheets by measuring and analyzing temperature dependent current-voltage characteristics. The RGO sheets were assembled between source and drain electrodes via dielectrophoresis. At low bias voltage the conduction is Ohmic while at high bias voltage and low temperatures the conduction becomes space charge limited with an exponential distribution of traps. We estimate an average trap density of $1.75 \times 10^{16} \text{ cm}^{-3}$. Quantitative information about charge traps will help develop optimization strategies of passivating defects in order to fabricate high quality solution processed graphene devices. © 2010 American Institute of Physics. [doi:10.1063/1.3484956]

Nanostructures of graphene oxide (GO) have created a lot of attention as it provides a pathway to produce large quantities of graphene sheets in solution at low cost.^{1–13} The easy processibility of GO and compatibility with various substrates including plastics makes them an attractive candidate for high yield manufacturing of graphene based electronic devices. However, GO is an electrically insulating material consisting of a large number of C–O bonds. Removal of C–O bonds by chemical and/or thermal reduction technique produces reduced graphene oxide (RGO) sheets and allows one to restore the electrical properties. RGO sheets have been used for field effect transistors (FETs),^{3–9} chemical sensors,¹⁰ organic solar cells,¹¹ as well as transparent electrodes in photovoltaic devices.^{12,13} However, the electrical conductivity and field effect mobility values for RGO sheets are much inferior to that of pristine graphene. This has been attributed to a large amount of disorder present in the RGO sheets. Disorder in RGO sheets have mostly been characterized with temperature dependence of resistivity where variable range hopping and activated hopping have been observed.^{6–8} Such a study does not provide detailed information about the nature and density of charge traps in the system. A detailed knowledge of charge conduction and quantitative information about charge traps is important for further optimization of reduction techniques and synthetic strategies for increasing conductivity and mobility of RGO toward pristine graphene. Similar strategies have been successfully used for passivating defects in silicon to fabricate high quality complementary metal oxide semiconductor circuits.

In this paper we present measurements and analysis of temperature dependent current density (J)-voltage (V) characteristics to elucidate on the nature and density of charge traps in the RGO sheets. The GO sheets suspended in water were reduced chemically in the solution and then assembled between prefabricated gold source and drain electrodes via ac dielectrophoresis (DEP). We show that the J - V character-

istic of the RGO devices measured at different temperatures (295 to 77 K) follow power law behavior, $J \propto V^m$. At low bias, the conduction is Ohmic with $m=1$, while at higher bias voltages m increases from 2 to 3 with reducing temperature signifying space charge limited conduction (SCLC) with a transition from trap free (TF-SCLC) regime at room temperature to exponentially distributed trap (EDT-SCLC) regime at low temperatures. We estimate an average trap density of $1.75 \times 10^{16} \text{ cm}^{-3}$ for our samples.

RGO sheets were synthesized through a chemical reduction of GO in solution prepared by modified Hummers method.¹⁴ Oxidized graphite in water was ultrasonicated to achieve GO monolayer sheets followed by centrifugation for 30 min at 3000 rpm to remove any unexfoliated oxidized graphite. The pH of GO dispersion in water (0.1 mg/mL) was adjusted to 11 using a 5% ammonia aqueous solution. 15 μL of hydrazine solution (35% in N,N-dimethylformamide) was then added and the mixture was heated at 95–100 °C for 1 h. X-ray photoelectron spectroscopy spectra show effective reduction in GO (see Ref. 15). Devices were fabricated on heavily doped silicon (Si) substrates capped with a thermally grown 250 nm thick SiO₂ layer. Source and drain electrode patterns with a channel length of 500 nm and width of 500 nm were defined by electron beam lithography and thermal deposition of 5 nm Cr and 20 nm Au followed by lift off.

The RGO sheets were assembled between the source and drain electrodes via DEP. Figure 1(a) shows a cartoon of the DEP setup. Details of the assembly were presented in our previous publication.⁹ In brief, a small drop of RGO solution was placed onto the electrodes pattern. An ac voltage of approximately $3V_{p-p}$ at 1 MHz was applied for 20–30 s after which the solution droplet was blown off by nitrogen gas. Figure 1(b) shows tapping-mode atomic force microscope (AFM) image of a representative devices with the height analysis shown in Fig. 1(c). It can be seen that the thickness varies from 2 to 8 nm in the channel indicating that up to eight layers of RGO sheets have been assembled. The devices were then annealed in Ar/H₂ gas at 200 °C for an

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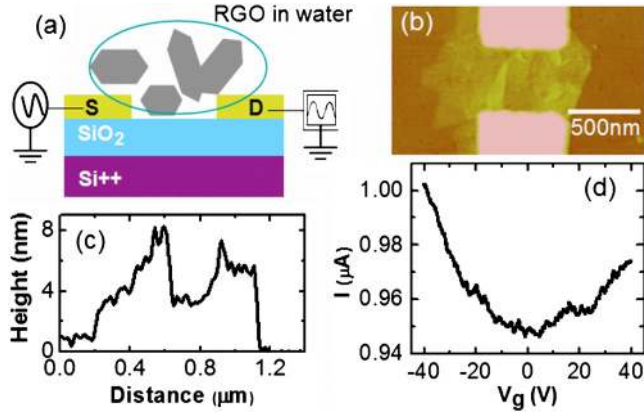


FIG. 1. (Color online) (a) Cartoon of DEP assembly setup. (b) Tapping-mode AFM of a RGO device assembled via DEP. Scale bar represents 500 nm. (c) Height profile of the AFM image shown in Fig. 1(b). (d) Room temperature transfer characteristic of device A.

hour, and loaded into a variable temperature cryostat after bonding. Temperature dependent electronic transport measurements from 295 to 77 K were performed using a Keithley 2400 source-meter, and a current preamplifier (DL 1211) capable of measuring subpicoampere signal interfaced with LABVIEW program. A total of nine devices were investigated.

Figure 1(d) shows the room temperature transfer characteristics of a representative RGO device (device A) where the current (I) is plotted as a function of gate voltage (V_g) measured in vacuum. The gate voltage was scanned from -40 to $+40$ V with a fixed source-drain voltage of $V=0.5$ V. The device shows an ambipolar FET behavior while. The room temperature hole mobility and the carrier concentration were calculated as $0.71 \text{ cm}^2/\text{V s}$ and $12 \times 10^{12} \text{ cm}^{-2}$, respectively. The FET properties are similar to other studies reported previously.³⁻⁹ However, recent report suggests that the mobility can be significantly higher when the size of RGO is big and reduction is done at very high temperature.^{16,17}

Figures 2(a) and 2(b) show the I - V characteristics at various temperatures measured from -5 to 5 V with $V_g=0$ for device A. The magnitude of the applied bias was limited to 5 V to avoid electrical breakdown of the RGO devices. The I - V curves are highly symmetric at all temperatures. In addition, the I - V curve became increasingly nonlinear with decreasing temperature. The nonlinearity in I - V curves in disordered semiconductor systems has been explained using (i) Schottky barrier (SB) between metal electrode and semiconductor, (ii) Fowler-Nordheim (FN) tunneling, and (iii) SCLC. In general, the I - V curve of a metal-semiconductor-metal junction should be highly asymmetric if the SB is dominated. However, our I - V curves are highly symmetric [see Fig. 2(b)] giving evidence that charge transport is not dominated by SB. Additionally, the attempt to fit our data with the SB was not successful (not shown here). FN tunneling can be ruled out as in FN model,¹⁸ the I - V curves are independent of temperature while our I - V curves are highly sensitive to temperature.

We now discuss SCLC mechanism. SCLC occurs in low mobility semiconductors when injected charge density exceeds the intrinsic free carrier density of the material. Analysis of the J - V characteristics using the SCLC model is one of the experimental methods for the detection of charge trap states in disordered semiconductors. In the ab-

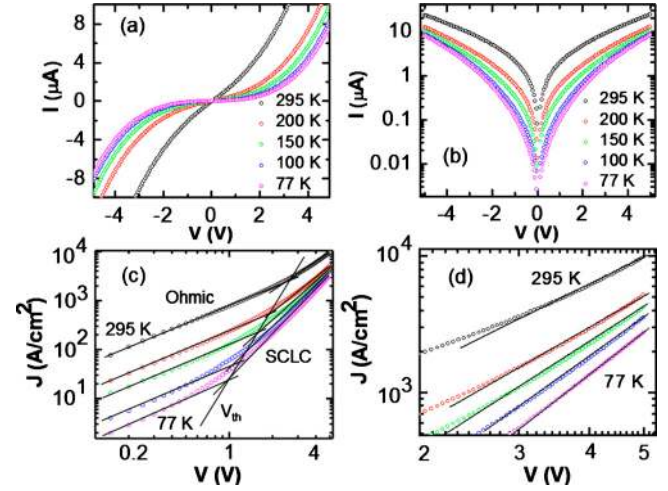


FIG. 2. (Color online) (a) Current-Voltage (I - V) characteristics at different temperatures for device A. (b) I - V curves at different temperatures plotted in semi log scale to clearly show highly symmetric nature of the curves. (c) Current density (J) vs V plotted in a log-log scale for different temperatures. The symbols are the experimental points while the solid lines are fits to $J \propto V^m$. Two regions are separated by V_{th} . For $V < V_{th}$, $m=1$ and the conduction is Ohmic. $V > V_{th}$ the conduction is due to SCLC with exponentially distributed trap states. (d) Expanded view of the SCLC regime. For clarity, J at 77 K was divided by 1.2.

sence of any trap states or when trap states do not dominate the transport, the J - V characteristics are described using, $J=9\epsilon_0\epsilon_r\mu V^2/8d^3$ where ϵ_0 is the permittivity of free space, ϵ_r the dielectric constant of the RGO, μ is the charge carrier mobility, and d is the spacing between electrodes.¹⁹ However, in presence of trap states that are exponentially distributed in energy, the J - V relationship is given by $J=(\mu N_v/q^{l-1})[(2l+1)/(l+1)]^{1/l}\{(\epsilon\epsilon_0/N_t)[l/(l+1)]\}^{1/(V^{l+1}/d^{2l+1})}$ where, l is an exponent and should be greater than 1, q is the electronic charge, N_v is effective density of states, and N_t is the trap density.²⁰ By plotting J and V in log-log scale one can determine the value of exponent m . For trap free (TF-SCLC) regime, $m=2$ while for exponentially distributed trap (EDT-SCLC) regime $m=l+1 > 2$.

Fig. 2(c) shows J versus V curves at different temperature in a log-log scale for sample A. The dotted symbols are the experimental data points and the solid lines are a fit to $J \propto V^m$. At low voltages, m equals to 1 at all temperatures signifying Ohmic conduction. However, at higher voltages, m deviates from 1. V_{th} , the onset voltage where $\log J$ - $\log V$ curves begin to inflect to higher slope region, shifts to lower voltage with decreasing temperature. For $V > V_{th}$, $m=2$ at room temperature implying TF-SCLC regime. However, as the temperature is reduced, the value of m for $V > V_{th}$ is increased to 2.3 at 200 K, 2.6 at 150 K, 2.8 at 100 K, and 3 at 77 K. The J - V curves for higher values of V are more clearly shown in Fig. 2(d). For these temperatures, the conduction is governed by traps that are exponentially distributed in energy (EDT-SCLC).

A transition from TF-SCLC regime at room temperature to EDT-SCLC regime at low temperature can occur for the following reason: At room temperature, the free carrier density is higher than the trap density. However, as the temperature is reduced, free carrier density is also reduced and the trap states started to dominate by localizing charge carriers and we enter EDT-SCLC regime with $m > 2$.

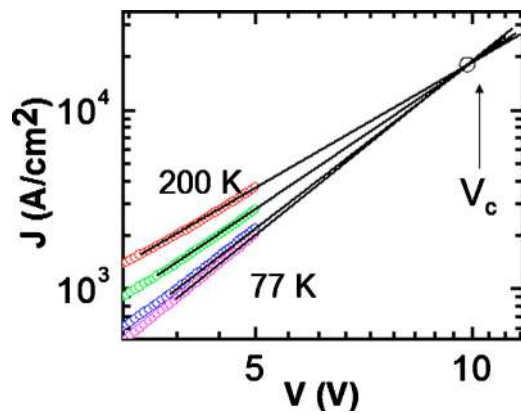


FIG. 3. (Color online) Extrapolation of the J - V curves at low temperatures plotted in log-log scale for device A. From this plot, we determine the temperature independent crossover voltage $V_c = 10$ V.

More quantitative information about traps can be obtained by extrapolating J - V curves in voltage. If charge traps are distributed in energy, they will be gradually filled with increasing electric field at all temperatures and at a certain critical voltage, all traps will be filled. According to Kumar *et al.*²¹ this critical voltage is independent of temperature and is given by $V_c = qN_t d^2 / 2\epsilon_r \epsilon_0$. By extrapolating the J - V curves we can obtain values for V_c and calculate trap density N_t . In Fig. 3, we extrapolate the log J and log V characteristic at higher bias voltages for all temperatures except room temperature. The $V_c = 10$ V was found for device A. In order to calculate the trap density from V_c , we need to know the dielectric constant (ϵ_r) of chemically RGO. The value of ϵ_r can be calculated by using; $\epsilon_r = n^2 - k^2$, where n and k are refractive index and extinction coefficient of RGO film, respectively. Using the values of n and k in the thermally reduced GO,²² we calculate $\epsilon_r = 3.5$. Using this value, we obtain trap density $N_t = 1.54 \times 10^{16}$ cm⁻³ for A.

Similar EDT-SCLC regime at low temperatures was observed in all nine samples that we have measured. In Ref. 15 (Table I), we summarize all measured RGO devices where we tabulate room temperature hole mobility, V_c and N_t values. All measured devices show similar trap density. The average trap density was about 1.75×10^{16} cm⁻³.

An exponential distribution of trap in energies is expected for the traps originating from surface defects and structural disorders.²³ When GO is produced via oxidation, some C-C bonds can get broken creating vacancies.²⁴ During the reduction process, carbon can also get removed from the GO backbone.²⁵ Although, this has been theoretically shown for thermal reduction cases, however, such study for chemical reduction cases are yet to be done. In addition, line defects such as wrinkles and folding of RGO sheet also create defects.² Because of the presence of the large number of trap states, charge in the gate would induce charge in the traps rather than free charge carrier in the semiconducting RGO sheets causing a low mobility in these sheets. Our study suggests that a large number of trap states exists in RGO and call for more theoretical and experimental investigations to understand how the trap states are created and how can they be minimized.

In conclusion, we elucidated on the low mobility and density of charge traps in RGO sheets by measuring and analyzing temperature dependent current-voltage characteris-

tics. The GO sheets suspended in water were reduced chemically in the solution and then assembled between prefabricated gold source and drain electrodes via ac DEP. We show that at low bias voltage the conduction is Ohmic while at high bias voltage the conduction becomes SCLC. At room temperature, the conduction is governed by trap free SCLC while at a lower temperature it is dominated by traps that are exponentially distributed in energy. We estimated an average trap density of 1.75×10^{16} cm⁻³. Quantitative studies of charge traps using SCLC presented in this work will facilitate further development of strategies for the chemical modification of RGO surfaces to passivate traps and thereby improve the carrier transport by providing quantifying evidences of the developed strategies of passivating defects in order to fabricate high quality solution processed graphene devices.

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