Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages

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Abstract: A pulse width modulation (PWM) scheme for multilevel inverters is proposed. The proposed PWM scheme generates the inverter leg switching times, from the sampled reference phase voltage amplitudes and centres the switching times for the middle vectors, in a sampling interval, as in the case of conventional space vector PWM (SVPWM). The SVPWM scheme, presented for multilevel inverters, can also work in the overmodulation range, using only the sampled amplitudes of reference phase voltages. The present PWM technique does not involve any sector identification and considerably reduces the computation time when compared to the conventional space vector PWM technique. The present PWM signal generation scheme can be used for any multilevel inverter configuration. A five-level inverter configuration, using an open-ended winding induction motor drive, is used to verify the SVPWM generation scheme experimentally.

1 Introduction

The two most widely used PWM schemes for multilevel inverters are the carrier-based sine-triangle PWM (SPWM) technique and the space vector PWM (SVPWM) technique. These modulation techniques have been extensively studied and compared for the performance parameters with two-level inverters [1, 2]. The SPWM schemes are more flexible and simpler to implement, but the maximum peak of the fundamental component in the output voltage is limited to 50% of the DC link voltage [2], and the extension of the SPWM schemes into the over-modulation range is difficult. In SVPWM schemes, a reference space vector is sampled at regular intervals to determine the inverter switching vectors and their time durations, in a sampling interval. The SVPWM scheme gives a more fundamental voltage and better harmonic performance compared to the SPWM schemes [3–5]. The maximum peak of the fundamental component in the output voltage obtained with space vector modulation is 15% greater than with the sine-triangle modulation scheme [2, 3]. But the conventional SVPWM scheme requires sector identification and look-up tables to determine the timings for various switching vectors of the inverter, in all the sectors [3, 4]. This makes the implementation of the SVPWM scheme quite complicated. A SVPWM scheme, extending the modulation range into the overmodulation range, has been presented [6, 7], in which extensive offline computations and look-up tables are required, to determine the modified reference vector, in the overmodulation range, extending up to six-step operation. It has been shown that, for two-level inverters, a SVPWM-like performance can be obtained with a SPWM scheme by adding a common mode voltage of suitable magnitude, to the sinusoidal reference phase voltage [4, 5]. A simplified method, to determine the correct offset times for centreing the time durations of the middle inverter vectors, in a sampling interval, is presented [8], for the two-level inverter. The inverter leg switching times are calculated directly from the sampled amplitudes of the reference three-phase voltages with considerable reduction in the computation time [8].

The SPWM technique, when applied to multilevel inverters, uses a number of level-shifted carrier waves to compare with the reference phase voltage signals [9]. The SVPWM for multilevel inverters [10, 11] involves mapping of the outer sectors to an inner subhexagon sector, to determine the switching time duration, for various inverter vectors. Then the switching inverter vectors corresponding to the actual sector are switched, for the time durations calculated from the mapped inner sectors. It is obvious that such a scheme, in multilevel inverters, will be very complex, as a large number of sectors and inverter vectors are involved. This will also considerably increase the computation time.

A modulation scheme is presented in [12], where a fixed common mode voltage, is added to the reference phase voltage throughout the modulation range. It has been shown [13] that this common mode addition will not result in a SVPWM-like performance, as it will not centre the middle inverter vectors in a sampling interval. The common mode voltage to be added in the reference phase voltages, to achieve SVPWM-like performance, is a function of the modulation index for multilevel inverters [13]. A SVPWM scheme based on the above principle has been presented [14], where the switching time for the inverter legs is directly determined from sampled phase voltage amplitudes. This technique reduces the computation time considerably more than the conventional SVPWM techniques do, but it involves region identifications based on modulation indices. While this SVPWM scheme works well for a three-level PWM generation, it cannot be extended to multilevel

inverters of levels higher than three, as the region identification becomes more complicated. A carrier-based PWM scheme has been presented [15], where sinusoidal references are added with a proper offset voltage before being compared with carriers, to achieve the performance of a SVPWM. The offset voltage computation is based on a modulus function depending on the DC link voltage, number of levels and the phase voltage amplitudes. The implementation details and the operation of the proposed method in the overmodulation region remain unaddressed.

The objective of this paper is to present an implementation scheme for PWM signal generation for multilevel inverters, similar to the SVPWM scheme, for the entire range of modulation indices including overmodulation. The PWM switching times for the inverter legs are directly derived from the sampled amplitudes of the reference phase voltages. The SVPWM switching pattern generation is not realised with offset voltage computation from a modulus function [15]. A simple way of adding a time offset to the inverter-gating signal, to generate the SVPWM pattern, from only the sampled amplitudes of reference phase voltages, is explained. The proposed SVPWM signal generation does not involve checks for region identification, as in the SVPWM scheme presented in [14]. Also, the algorithm does not require either sector identification or look-up tables for switching vector determination as are required in the conventional multilevel SVPWM schemes [10, 11]. Thus the scheme is computationally efficient when compared to conventional multilevel SVPWM schemes, making it superior for real-time implementation. The proposed SVPWM algorithm can easily be extended to any multilevel inverter configurations. For experimental verification of the proposed SVPWM scheme, we are using a five-level inverter configuration with an open-ended winding induction motor [12].

2 Proposed SVPWM in linear modulation range

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other [1]. To obtain the maximum possible peak amplitude of the fundamental phase voltage, in linear modulation, a common mode voltage, $V_{offset1}$, is added to the reference phase voltages [5, 12], where the magnitude of $V_{offset1}$ is given by

$$V_{offset1} = -(V_{\max} + V_{\min})/2 \tag{1}$$

In (1), $V_{\max}$ is the maximum magnitude of the three sampled reference phase voltages, while $V_{\min}$ is the minimum magnitude of the three sampled reference phase voltages, in a sampling interval. The addition of the common mode voltage, $V_{offset1}$, results in the active inverter switching vectors being centred in a sampling interval, making the SPWM technique equivalent to the SVPWM technique [3]. Equation (1) is based on the fact that, in a sampling interval, the reference phase which has lowest magnitude (termed the *min-phase*) crosses the triangular carrier first, and causes the first transition in the inverter switching state. While the reference phase, which has the maximum magnitude (termed the *max-phase*), crosses the carrier last and causes the last switching transition in the inverter switching states in a two-level SVPWM scheme [5, 13]. Thus the switching periods of the active vectors can be determined from the (*max-phase* and *min-phase*) sampled reference phase voltage amplitudes in a two-level inverter scheme [8]. The SPWM technique, for multilevel inverters, involves comparing the reference phase voltage signals with a number of symmetrical level-shifted carrier waves for PWM generation [9]. It has been shown that for an n-level inverter, $n-1$ level-shifted carrier waves are required for comparison with the sinusoidal references [9]. Because of the level-shifted multicarriers (Fig. 1), the first crossing (termed the *first-cross*) of the reference phase voltage cannot always be the *min-phase*. Similarly, the last crossing (termed the *third-cross*) of the reference phase voltage cannot always be the *max-phase*. Thus the offset voltage computation, based on (1) is not sufficient to centre the middle inverter switching vectors, in a multilevel PWM scheme during a sampling period T_s (Fig. 2). In this paper, a simple technique to determine the offset voltage (to be added to the reference phase voltage for PWM generation for the entire modulation range) is presented, based only on the sampled amplitudes of the reference phase voltages. The idea behind the proposed scheme is to determine the sampled reference phase, from the three sampled reference phases, which crosses the triangular first (*first-cross*) and the reference phase which crosses the triangular carrier last (*third-cross*). Once the first-cross phase and third-cross phase are identified, the principles of offset calculation of (1), for the two-level inverter, can easily be adapted for the multilevel SVPWM generation scheme. The proposed

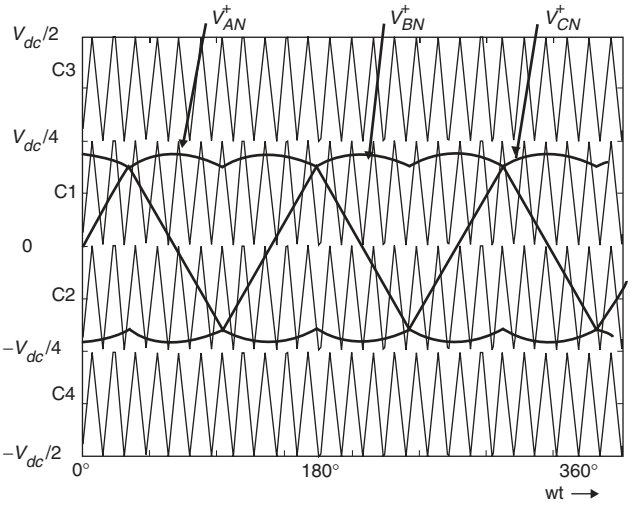


Fig. 1 *Modified reference voltages and triangular carriers for a five-level PWM scheme*

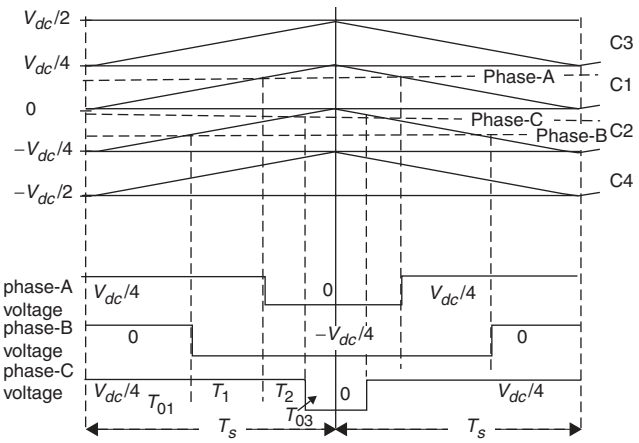


Fig. 2 *Inverter switching vectors and their switching time durations during sampling interval T_S*
reference voltages are within the inner carrier region, $M<0.433$

SVPWM technique presents a simple way to determine the time instants at which the three reference phases cross the triangular carriers. These time instants are sorted to find the offset voltage to be added to the reference phase voltages for SVPWM generation for multilevel inverters for the entire linear modulation range, so that the middle inverter switching vectors are centred (during a sampling interval), as in the case of the conventional two-level SPWM scheme.

2.1 Determination of the offset voltage to generate the inverter leg switching times for a five-level inverter

Figure 1 shows the reference voltage and four triangular carriers used for PWM generation for a five-level inverter. The modified reference phase voltages are given by

$$V^*_{XN} = V_{XN} + V_{offset1}, \quad X = A, B, C \tag{2}$$

where V_{AN}, V_{BN} and V_{CN} are the sampled amplitudes of three reference phase voltages during the current sampling interval and $V_{offset1}$ is calculated from (1).

The reference phase voltages are equally spaced between the four carriers as shown in Fig. 1, for a five-level inverter. For modulation indices less than 0.433 (half of the maximum modulation index in the linear range of modulation for a five-level inverter), the reference phase voltage spans inner two carriers. For modulation indices higher than 0.433, the reference phase voltages expand into the outer carrier regions (the modulation index, M, is defined as the ratio of magnitude of the equivalent reference voltage space vector, generated by the three reference phase voltages, to the DC link voltage). The addition of $V_{offset1}$, obtained from (1), to the reference phase voltage ensures that the modified reference voltages always remain within the carrier regions throught the linear modulation range (maximum modulation index in the linear modulation range is 0.866) [3].

The reference phase voltages cross the triangular carriers at different instants in a sampling period T_s (Fig. 1). Each time a reference phase voltage crosses the triangular carrier it causes a change in the inverter state. The phase voltage variations and their time durations are shown in Fig. 2. The sampling time interval T_s, can be divided into four time intervals T_{01}, T_1, T_2 and T_{03}. T_{01} and T_{03} are defined as the time durations for the start and end inverter switching vectors respectively, in a sampling time interval T_s. T_1 and T_2 are defined as the time durations for the middle inverter switching vectors, in a sampling time interval T_s. It should be noted from Fig. 2 that the middle switching vectors are not centred in a sampling interval T_s. So an additional offset (offset2) needs to be added to the reference phase voltages of Fig. 1, so that the middle inverter switching vectors can be centred in a sampling interval, similar to a two-level SVPWM [3].

The time duration, at which the A-phase crosses the triangular carrier, is defined as T_{a_cross} (Fig. 3). Similarly, the time durations, when the B-phase and C-phase cross the triangular carrier, are defined as T_{b_cross} and T_{c_cross}, respectively. Figure 3 shows a sampling interval when the A-phase is in the carrier region C1 while the B-phase and C-phase are in carrier region C2. As shown in Fig. 3, the time duration, T_{a_cross}, (measured from the start of the sampling interval) at which the A-phase crosses the triangular carrier is directly proportional to the phase voltage amplitudes, V^*_{AN}. The time duration, T_{b_cross}, at which the B-phase crosses the triangular carrier, is proportional to $(V^*_{BN} + V_{dc}/4)$ and the time duration, T_{c_cross}, at which the C-phase crosses the triangular carrier, is proportional to

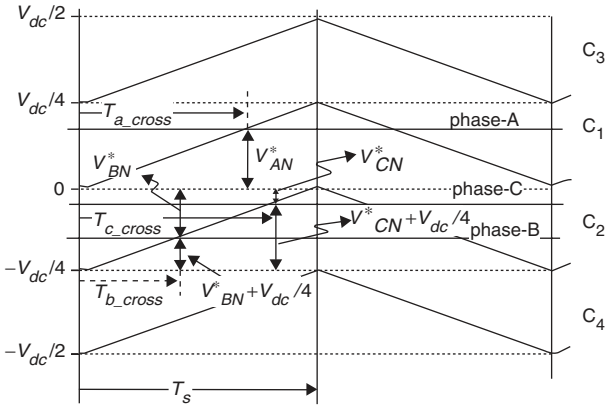


Fig. 3 *Determination of the T_{a_cross}, T_{b_cross} and T_{c_cross} during switching interval T_S*
reference voltages span the inner carrier region, $M<0.433$

$(V^*_{CN} + V_{dc}/4)$. Therefore

$$\begin{aligned} T_{a\_cross} &= V^*_{AN} \times \frac{T_s}{V_{dc}/4} = T^*_{as} \\ T_{b\_cross} &= (V^*_{BN} + V_{dc}/4) \times \frac{T_s}{V_{dc}/4} = T^*_{bs} + T_s \\ T_{c\_cross} &= (V^*_{CN} + V_{dc}/4) \times \frac{T_s}{V_{dc}/4} = T^*_{cs} + T_s \end{aligned} \tag{3}$$

where T^*_{as}, $T^*_{bs}$and $T^*_{cs}$are the time equivalents of the phase voltage magnitudes. The proportionality between the time equivalents and corresponding voltage magnitudes is defined as follows [8]:

$$\begin{aligned} (V_{dc}/4)/T_s &= V^*_{AN}/T^*_{as} \\ (V_{dc}/4)/T_s &= V^*_{BN}/T^*_{bs} \\ (V_{dc}/4)/T_s &= V^*_{CN}/T^*_{cs} \\ (V_{dc}/4)/T_s &= V_{offset1}/T_{offset1} \end{aligned} \tag{4}$$

Figure 4 shows the situation, where the reference phase voltages span the entire carrier region, for a five-level inverter scheme. The time durations, at which the reference phase voltages cross the carrier can be similarly determined. As shown in Fig. 4, T_{a_cross} is proportional to $(V^*_{AN} - V_{dc}/4)$. Whereas T_{b_cross} is proportional to $(V^*_{BN} + V_{dc}/2)$and T_{c_cross} is proportional to $(V^*_{CN} + V_{dc}/4)$. Therefore, from (4)

$$\begin{aligned} T_{a\_cross} &= (V^*_{AN} - V_{dc}/4) \times \left(\frac{T_s}{V_{dc}/4}\right) = T^*_{as} - T_s \\ T_{b\_cross} &= (V^*_{BN} + V_{dc}/2) \times \left(\frac{T_s}{V_{dc}/4}\right) = T^*_{bs} + (2 * T_s) \\ T_{c\_cross} &= (V^*_{CN} + V_{dc}/4) \times \left(\frac{T_s}{V_{dc}/4}\right) = T^*_{cs} + T_s \end{aligned} \tag{5}$$

Thus the time durations, at which the phase voltages cross the triangular carrier regions, for a five-level inverter, can be summarised as shown in Table 1. In the present work, the T_{a_cross}, T_{b_cross} and T_{c_cross} time durations obtained above are used to centre the middle switching vectors, as in the case of two-level inverters, in a sampling interval T_s [8]. The time duration, at which the reference phases cross the triangular carriers for the first time, is defined as T_{first_cross}. Similarly, the time durations, at which the reference phases cross the triangular carriers for the second and third time, are defined as, T_{second_cross} and T_{third_cross}, respectively, in a

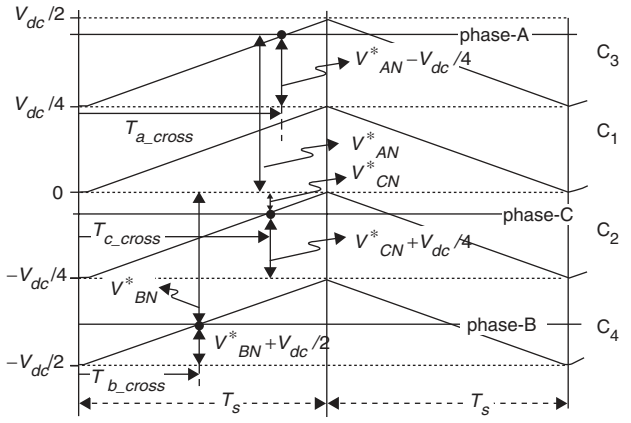


Fig. 4 *Determination of the T_{a_cross}, T_{b_cross} and T_{c_cross} during switching interval T_S (reference voltages span the entire carrier region, $0.433 < M < 0.866$)*

Table 1: The time durations T_{a_cross}, T_{b_cross} and T_{c_cross} in four carrier regions for five-level inverter

Carrier region	$T_{x\_cross}, x = a, b, c$
C3	$T^*_{xs} - T_s$
C1	T^*_{xs}
C2	$T^*_{xs} + T_s$
C4	$T^*_{xs} + (2^* T_s)$

sampling interval T_s.

$$T_{first\_cross} = \min(T_{x\_cross}),\ T_{\sec ond\_cross} = mid(T_{x\_cross}),\\ T_{third\_cross} = \max(T_{x\_cross}),\quad x = a, b, c \tag{6}$$

The time durations, T_{first_cross}, T_{second_cross} and T_{third_cross}, directly decide the switching times for the different inverter voltage vectors, forming a triangular sector, during one sampling interval T_s. The time durations for the start and end vectors, are $T_{01} = T_{first\_cross}$, $T_{03} = T_s - T_{third\_cross}$, respectively (Fig. 2). The middle vectors are centred by adding a time offset, $T_{offset2}$ to T_{first_cross}, T_{second_cross} and T_{third_cross}. The time offset, $T_{offset2}$ is determined as follows. The time duration for the middle inverter switching vectors, T_{middle}, is given by:

$$T_{middle} = T_{third\_cross} - T_{first\_cross} \tag{7a}$$

The time duration of the start and end vector is

$$T_0 = T_s - T_{middle} \tag{7b}$$

Thus the time duration of the start vector is given by

$$T_0/2 = T_{first\_cross} + T_{offset2}$$

Therefore

$$T_{offset2} = T_0/2 - T_{first\_cross} \tag{7c}$$

The addition of the time, $T_{offset2}$ to T_{a_cross}, T_{b_cross} and T_{c_cross} gives the inverter leg switching times T_{ga}, T_{gb} and T_{gc} for phases A, B and C, respectively.

$$T_{ga} = T_{a\_cross} + T_{offset2}\\ T_{gb} = T_{b\_cross} + T_{offset2}\\ T_{gc} = T_{c\_cross} + T_{offset2} \tag{8}$$

The traces of different timing signals, for the proposed PWM scheme, are shown in Figs. 5–7, for a five-level PWM generation. The traces of T_{a_cross} for various modulation indices are shown in Fig. 5. The traces of T_{first_cross}, T_{second_cross} and T_{third_cross} are shown in Fig. 3*a* while the traces of $T_{g\ first\_cross}$, $T_{g\ second\_cross}$ and $T_{g\ third\_cross}$ are shown in Fig. 6*b*. It can be seen from Fig. 6*b*, that the time durations for the start vector ($T_{g\ first\_cross}$) and for the end vector ($T_s - T_{g\ third\_cross}$) are equal. Thus the middle vectors are always centred, in a sampling time interval T_s. The plots of the time equivalent of the modified reference phase voltage,

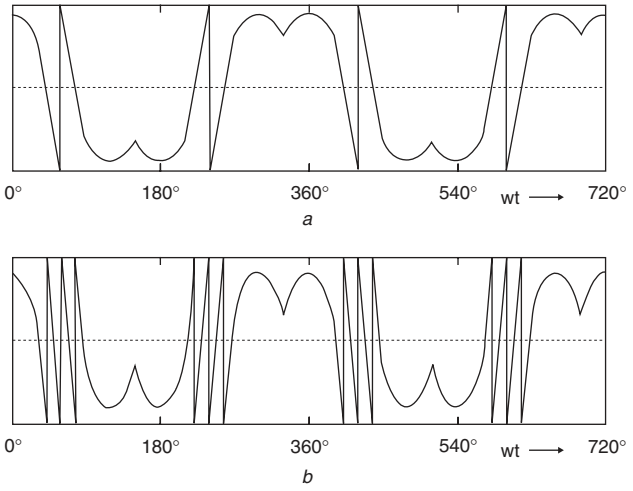


Fig. 5 *Trace of T_{a_cross} for modulation indexes 0.41 and 0.83*

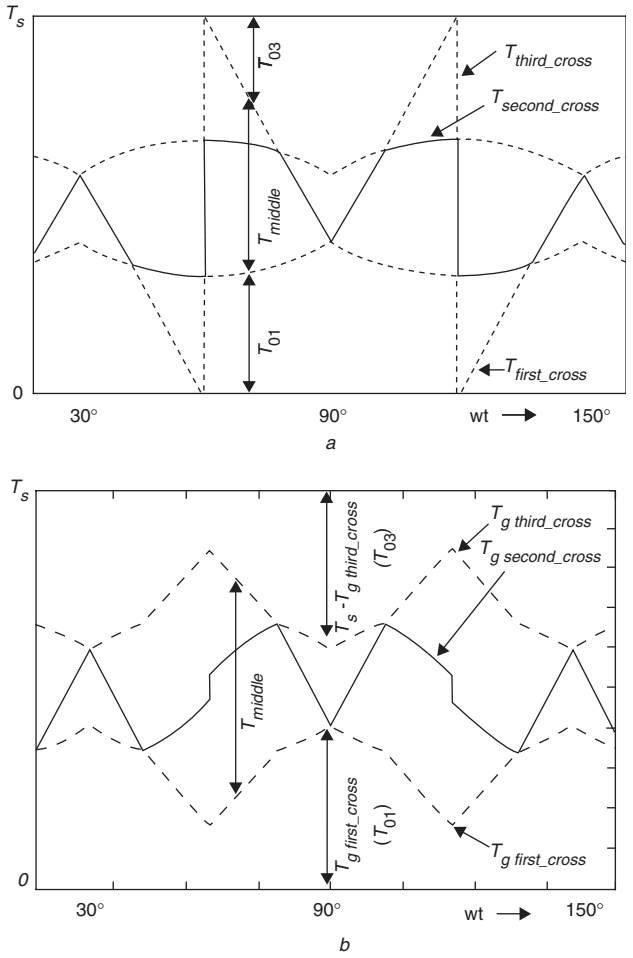


Fig. 6 *Traces of T_{first_cross}, T_{second_cross} and T_{third_cross}*
a non-centred time duration for middle vectors
b centred time duration for middle vectors, after addition of required offset, *T_offset2*

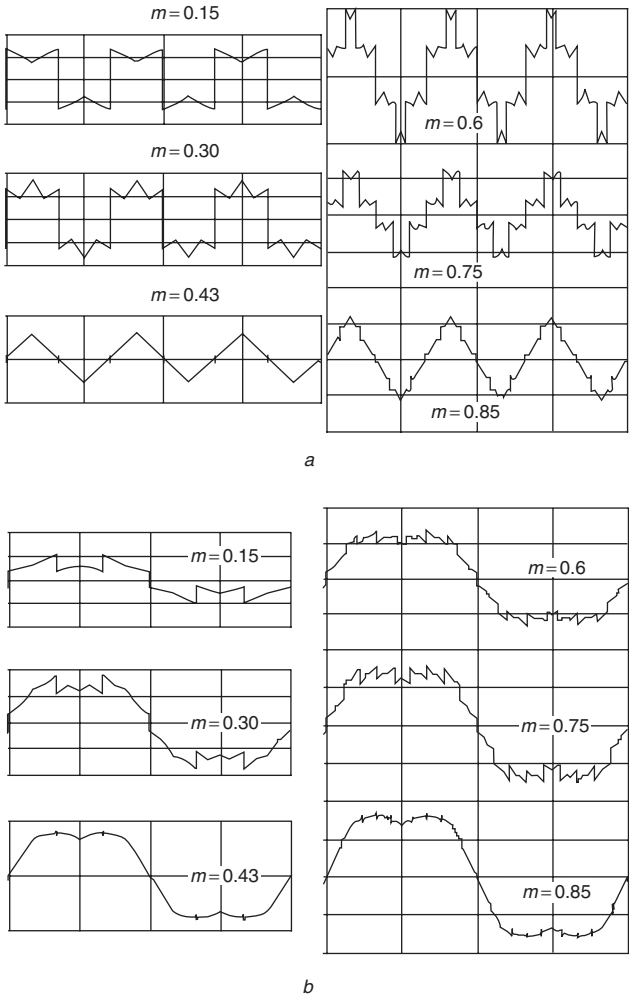


Fig. 7 *Modulation indices*
a profile of $T_{offset1} + T_{offset2}$ for different modulation indices
b profile of $T^*_{as} + T_{offset2}$ for different modulation indices

$T_{offset1} + T_{offset2}$, for various modulation indices, are shown in Fig. 7*a*. The corresponding traces of the total offset, $T^*_{as} + T_{offset2}$, added to the sinusoidal reference phase voltage to make the SPWM equivalent to the SVPWM, are shown in Fig. 7*b*.

2.2 Generalisation of the proposed SVPWM scheme for an n level PWM

The SVPWM, proposed for a five-level inverter, in the last Section, can be easily extended to any *n*-level PWM generation. In the SPWM scheme for an *n* level inverter, the reference signals are compared with $n-1$ level shifted carriers [9]. The triangular carriers and the reference signals, for an *n*-level PWM scheme are shown in Fig. 8*a*, for *n* is odd, and in Fig. 8*b*, for *n* is even. The $(n-1)$ triangular carriers are compared with reference phase voltages as shown in Figs. 8*a* and 8*b*. A carrier index, *I,* is defined to designate the carrier regions in which the reference phase voltages lie during the sampling interval under consideration. The indexing of *I* is as shown in Fig. 8*a* when *n* is odd. The carrier index *I* for the top carrier is 1, and it increases in steps of 1 towards the bottom carriers. The carrier index *I* for the lowest carrier is equal to (*n*–1).

During a sampling interval, the carrier indices, *Ia*, *Ib* and *Ic* (which can be from 1 to $n-1$), for A, B and C phases, respectively, are determined depending on the carrier region in which the respective phase voltage lies. The determination of the time durations, T_{a_cross}, T_{b_cross} and T_{c_cross} (as shown

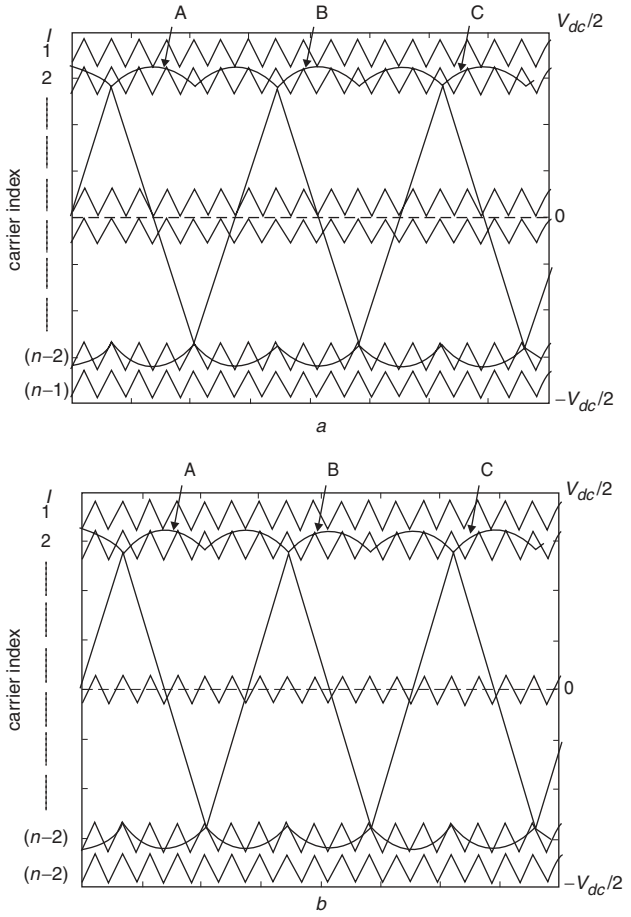


Fig. 8 *Triangular carriers and reference signals*
a *n*-level PWM scheme where *n* is odd
b *n*-level PWM scheme where *n* is even

in Table 1), when *n* is odd, can be generalised as

$$\begin{aligned} T_{a\_cross} &= T^*_{as} + ((I_a - (n-1)/2) * T_s) \\ T_{b\_cross} &= T^*_{bs} + ((I_b - (n-1)/2) * T_s) \\ T_{c\_cross} &= T^*_{cs} + ((I_c - (n-1)/2) * T_s) \end{aligned} \tag{9}$$

When *n* is even, the triangular carriers and the reference phase voltages, are as shown in Fig. 8*b*. In this case, the reference phase voltages are centred on the middle triangular carrier. The determination of T_{a_cross}, T_{b_cross} and T_{c_cross} can be generalised as,

$$\begin{aligned} T_{a\_cross} &= (T_s/2) + T^*_{as} + ((I_a - (n/2)) * T_s) \\ T_{b\_cross} &= (T_s/2) + T^*_{bs} + ((I_b - (n/2)) * T_s) \\ T_{c\_cross} &= (T_s/2) + T^*_{cs} + ((I_c - (n/2)) * T_s) \end{aligned} \tag{10}$$

Then the inverter leg switching times for (*n*-level inverter) each phase can be determined in the similar way, as given by (6)–(8) for the five-level inverter, in Section 2.1.

3 Proposed SVPWM signal generation in over-modulation

The extension of the SVPWM schemes, into the over-modulation range, for a two-level inverter requires extensive offline computations to achieve the output voltage as a linear function of the modulation index [7, 8]. The emphasis of SVPWM schemes, presented in [7, 8], is to obtain the transition, from the linear modulation range to the six-step mode, in a linear way. The computation time increases, because of the co-ordinate transformations and look-up

tables involved in practical implementations, making real-time implementation of these schemes quite complicated [7, 8]. An overmodulation scheme for two-level inverters, proposed in [16], for current controlled voltage source inverters, is simpler in implementation compared to over-modulation schemes [7, 8]. In this paper, an overmodulation scheme is proposed for multilevel inverters, based on the principles outlined in [16], which retains the simplicity of implementation as in the case of linear modulation, presented in the previous Sections. The proposed over-modulation scheme is very simple to implement and can be used for current controlled multilevel inverter-fed drive schemes.

3.1 Principle of SVPWM signal generation in the overmodulation region

In overmodulation, the middle inverter vectors are switched for the entire T_s interval. In the overmodulation scheme proposed in [16], the inverter voltage vector, which is switched for a longer time duration (T_1 or T_2, whichever is greater) is switched for the same time duration while the other vector is switched for the rest of the time interval T_s. If T_1 or T_2 is greater than T_s, only that particular vector is switched for the entire T_s duration [16]. Figure 9*a* shows the four sampling instants A–D on the trajectory of the reference space vector, which is moving outside the hexagon boundary, for a five-level inverter. Based on the magnitudes of T_1, T_2 and T_s the modified reference vector for the respective sampling instants is mapped on the hexagon boundary as shown by A', B', C' and D' in Fig. 9*a*. The sampling instants, A–D, correspond to the four regions $X1$, $X2$, $X3$ and $X4$ (depending on the magnitude T_1, T_2 and T_s), in Fig. 9*b*. The different conditions, to identify the various regions and switching time durations, for the actual inverter vectors, Vx and Vy (Fig. 9*b*) for the different regions, are summarised in Table 2.

3.2 Determination of inverter leg switching times in overmodulation from the sampled amplitudes of reference phase voltages

The proposed overmodulation scheme, based on the sampled amplitudes of the reference phase voltages, is similar to the linear SVPWM scheme presented in previous Sections. When the inverter operates in overmodulation T_{middle} is greater than T_s. This condition is used to detect the overmodulation condition. Figure 10 shows the profiles of T_{first_cross}, T_{second_cross} and T_{third_cross}, for the overmodulation condition, for a five-level inverter. The region A-A', of Fig. 10, is expanded and shown in Fig. 11. The time duration for the inverter switching vector, Vx is $(T_{second\_cross} - T_{first\_cross})$ and for the inverter switching vector, Vy is $(T_{third\_cross} - T_{second\_cross})$ as shown in Fig. 11. $T_{g\ first\_cross}$, $T_{g\ second\_cross}$ and $T_{g\ third\_cross}$ are the inverter leg switching times (obtained by adding the offset voltage to T_{first_cross}, T_{second_cross} and T_{third_cross}) for the phases, which cross the carriers for the first, second and third time, respectively. As only the middle vectors are switched during the sampling interval T_s, it is clear that $T_{g\ first\_cross} = 0$ and $T_{g\ third\_cross} = T_s$, in the over-modulation range. A simple algorithm is described below to determine $T_{g\ second\_cross}$ from T_{second_cross} by adding an offset $T_{offset2}$ such that the inverter voltage vector to be applied for longer duration (in any of the four regions, $X1$, $X2$, $X3$ and $X4$), is switched for the same time duration while the other vector is switched for rest of the duration in the sampling time interval T_s.

In region $X2$ (Figs. 9*b* and 11) $T_{third\_cross} - T_{second\_cross}$ is greater than $T_{second\_cross} - T_{first\_cross}$ and less than T_S, the

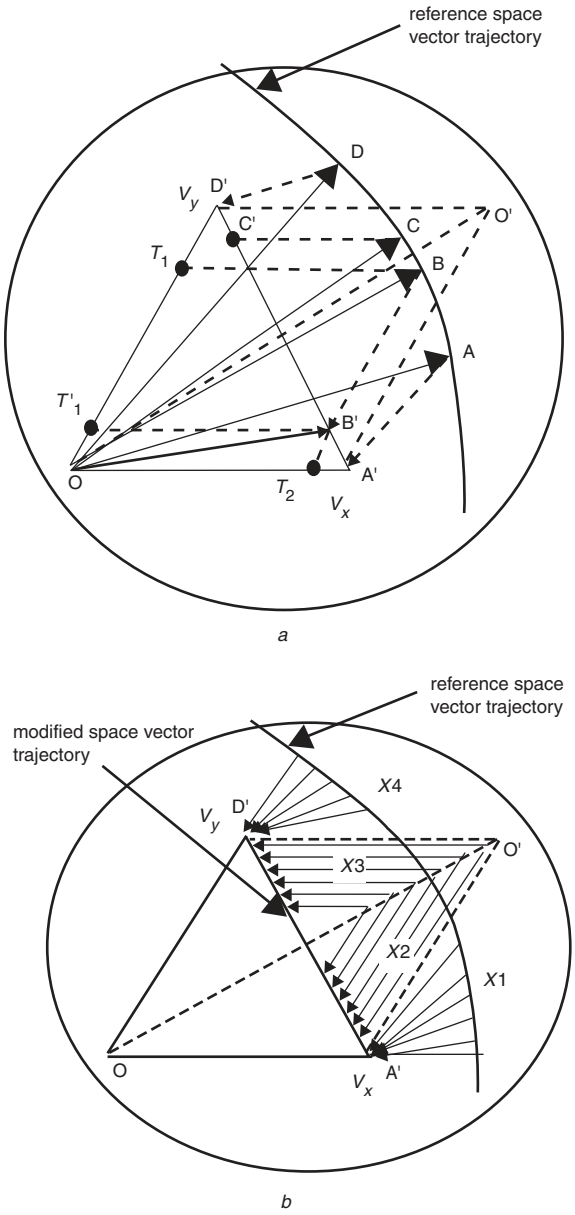


Fig. 9 *Mapping on periphery of hexagon*
a Mapping of reference space vector on outer periphery of hexagon
b Four different regions describing different ways of mapping on periphery of hexagon

Table 2: Actual switching time duration for overmodulation for various regions

Region	Condition	Switching time durations for inverter vectors	
		Vx	*Vy*
*X*1	$T_2 < T_s < T_1$	T_1	not switched
X2	$T_2 < T_1$, $(T_1 + T_2) > T_s$	T_1	$T_s - T_1$
X3	$T_2 > T_1$, $(T_1 + T_2) > T_s$	$T_s - T_2$	T_2
X4	$T_2 > T_s > T_1$	not switched	T_2

inverter switching vector, Vy is retained for same duration $T_{third\_cross} - T_{second\_cross}$, and the inverter switching vector Vx is applied for rest of the sampling interval T_s. From Fig. 12

$$T_{offset2} = T_s - T_{third\_cross} \tag{11}$$

Therefore in region $X2$, $T_{g\ second\_cross} = T_{second\_cross} + T_{offset2}$.

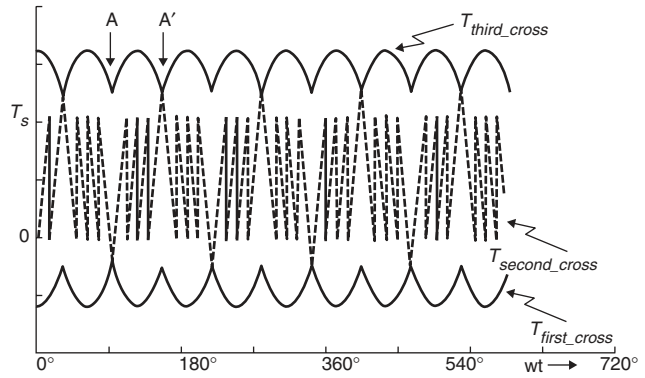


Fig. 10 *Profile of T_{first_cross}, T_{second_cross} and T_{third_cross}, when inverter operates in overmodulation*

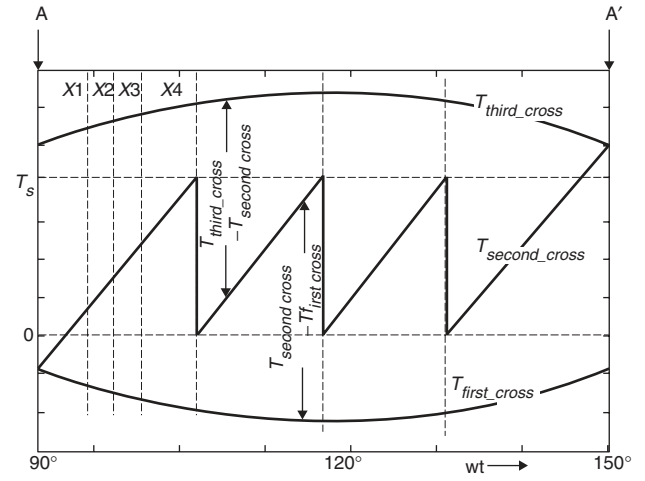


Fig. 11 *Time duration $(T_{second\_cross} - T_{first\_cross})$ and $(T_{third\_cross} - T_{second\_cross})$ for time duration A-A′ of Fig. 7a*

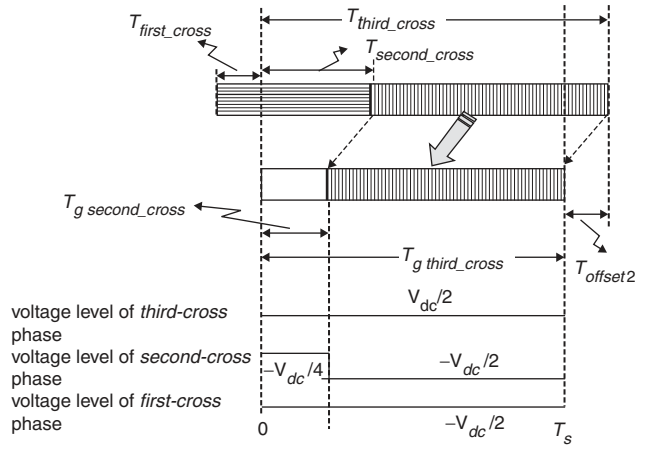


Fig. 12 *Principle of inverter switching time calculation in overmodulation*
$(T_{second\_cross} - T_{first\_cross}) < (T_{third\_cross} - T_{second\_cross})$, corresponding to regions X_1 and X_2 of Fig. 9*b*)

If $T_{third\_cross} - T_{second\_cross}$ is greater than T_s (corresponding to region $X1$ in Figs. 9*b* and 11), the inverter-switching vector, Vx, is switched for the entire sampling interval T_s. Therefore in region, $X1$, $T_{g\_second\_cross} = 0$.

In region $X3$, $T_{second\_cross} - T_{first\_cross}$ is greater than $T_{third\_cross} - T_{second\_cross}$ but less than T_s, and the inverter switching vector Vy is retained for duration

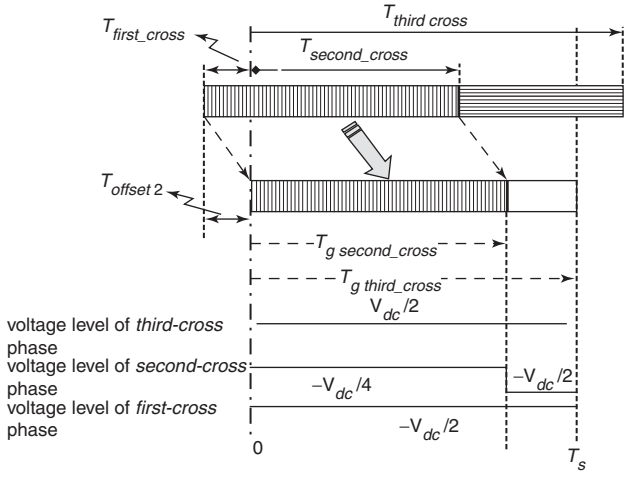


Fig. 13 *Principle of inverter switching time calculation in overmodulation*
$(T_{second\_cross} - T_{first\_cross}) > (T_{third\_cross} - T_{second\_cross})$, corresponding to region X_3 and X_4 of Fig. 9*b*

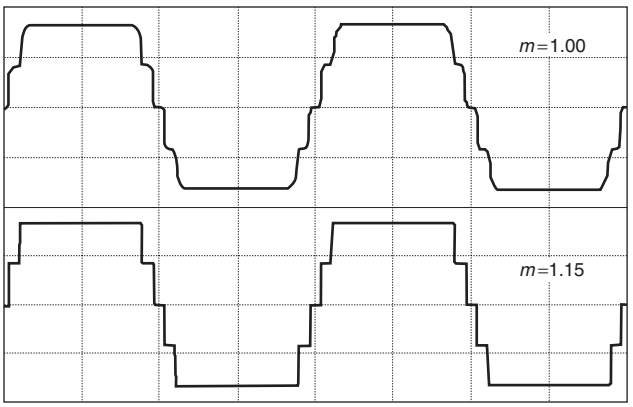


Fig. 14 *Profile of $T^*_{as} + T_{offset2}$ for different modulation indices in overmodulation*

$T_{second\_cross} - T_{first\_cross}$, and inverter switching vector Vx is applied for the rest of the duration. From Fig. 13, $T_{g\_second\_cross} = T_{second\_cross} + T_{offset2}$.

If $T_{second\_cross} - T_{first\_cross}$ is greater than T_s itself (corresponding to region $X4$ in Fig. 9*b*), the inverter-switching vector Vy is switched for the entire T_s duration. Therefore $T_{g\_second\_cross} = T_s$.

The implementation is greatly simplified and subsequent switching times outside other sectors, for inverter legs, can be directly obtained as described above. $T_{g\,first\_cross}$, $T_{g\_second\_cross}$ and $T_{g\_third\_cross}$ time durations can be associated appropriately with the A,B,C legs of the inverter (T_{ga}, T_{gb} and T_{gc}) if monitoring establishes which phase has crossed the carriers for the first, second and for third time during the particular sampling period. The traces of $T^*_{as} + T_{offset2}$ for various modulation indices in the overmodulation region are shown in Fig. 14. The proposed algorithm is presented in the Appendix (Section 7.1).

4 Experimental verification of the proposed SVPWM technique

The proposed SVPWM scheme is implemented using a TMS320F240 DSP controller for a 1.5 kW three-phase induction motor drive with V/f control for different modulation indices covering the entire speed range. A

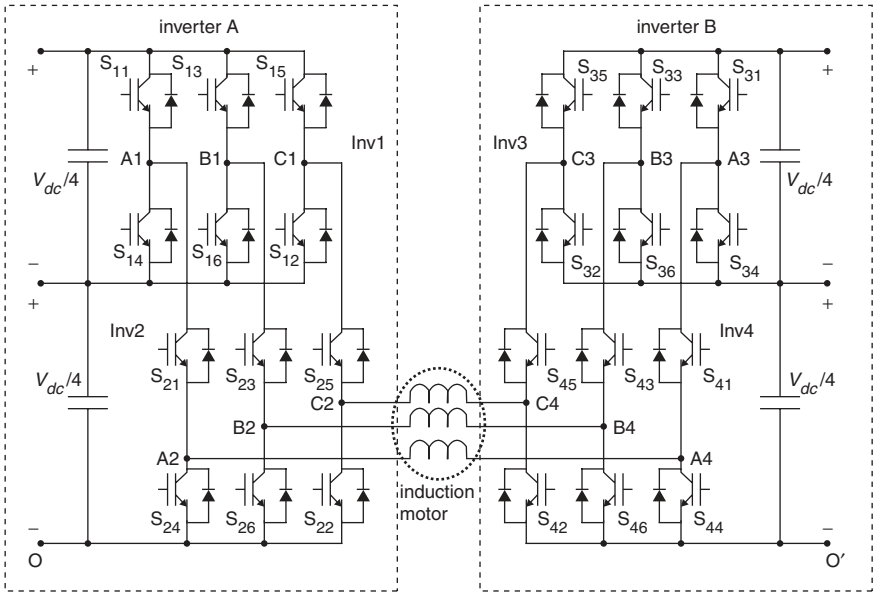


Fig. 15 *Five-level inverter configuration formed by cascading two three-level inverters*

five-level inverter configuration with open-end winding induction motor drive is used for experimental verification of the proposed algorithm throughout the range of modulation (Fig. 15). The induction motor parameters are given in the Appendix (Section 7.2).

4.1 Five-level inverter configuration

The five-level inverter configuration is achieved by cascading two three-level inverters from both ends for an open-ended winding induction motor as shown in Fig. 15. Such a configuration will result in output phase voltages across the induction motor phase windings, equivalent to a five-level conventional neutral point clamped inverter [12]. The open-ended winding configuration of the three-phase induction motor makes it possible to feed the voltages from both ends of the motor winding. The three-level inverters, inverter-A and inverter-B, are realised by cascading two two-level inverters [17]. The phase voltage across the phase winding of induction motor V_{A2A4} can be either $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$, $-V_{dc}/2$ depending upon the switching states of the three-level inverters (inverter-A and inverter-B) [12]. The combinations of inverter-A and inverter-B pole voltages and the resulting phase voltage across the winding of the induction motor are shown in Table 3. Similarly, the levels for other phase windings, B2B4 and C2C4, can also be determined [12]. A five-level space vector diagram, as shown in Fig. 16, represents the resultant space vector combinations and their locations. The resultant hexagon can be seen as formed of four layers: layer 1, innermost layer; layer 2, next outer layer; layer 3, layer outside layer 2; and layer 4, outermost layer. The corresponding levels of voltage across the phase winding are as shown in Table 3.

Table 3: Pole voltages of inverter-A and inverter-B and resulting phase voltage across phase winding of motor

Pole voltage of phase-A of inverter-A, V_{A20}	Pole voltage of phase-A of inverter-B, V_{A40}	Phase voltage across the winding of induction motor, V_{A2A4}	Phase voltage Level
$V_{dc}/2$	0	$+V_{dc}/2$	4
$V_{dc}/4$	0	$+V_{dc}/4$	3
0	0	0	2
0	$V_{dc}/4$	$-V_{dc}/4$	1
0	$V_{dc}/2$	$-V_{dc}/2$	0

4.2 Deriving the gate signals for inverter phases

The inverter leg switching times, (T_{ga}, T_{gb} and T_{gc}) are used to generate the PWM signals for A,B,C phases, respectively. The PWM signals for three phases are generated using fully compared units of DSP. During the sampling time interval, T_s, the five-level inverter legs switch between two adjacent voltage levels. The phase voltage levels in which the inverter leg switches depend on the carrier in which the modified reference phase voltages, V_{AN}, V_{BN} and V_{CN} lie. The level information is obtained from the carrier index, I. The carrier index, Ia, Ib and Ic for three phases is taken from the DSP I/O ports. For example, depending on the values of carrier index, I for phase-A the output pins A3 and A2 are made high or low as per Table 4.

The decoding of these signal along with PWM_A, signals is done using PALCE22V10. The gate signals for different switches are generated using PALCE22V10 as shown in Table 5 for phase-A. The gate signals for different switches of B and C phases are similarly generated using PWM and carrier index, I for the respective phases.

4.3 Experimental results

The modulation index is varied from the low modulation index to the overmodulation region covering all layers of the five-level inverter configuration. The DC link voltage of 100 V is used for each inverter. The experimental results are presented in Figs. 17–22. Figure 17 shows pole voltages, V_{A20} and V_{A40}, when the modulation index is 0.15. This corresponds to layer 1 operation (three-level mode) of the five-level inverter. Figure 17*b* shows the corresponding phase-A voltage and phase current when the motor is at no load. Figure 17*c* shows the ($T^*_{as}+T_{offset2}$) and ($T_{offset1}+T_{offset2}$) offset waveform (DAC output). The total offset ($T_{offset1}+T_{offset2}$) and ($T^*_{as}+T_{offset2}$) waveforms are in agreement with the simulated waveforms shown in Fig. 14.

The pole voltage waveforms for inverter-A (V_{A20}) and inverter-B (V_{A40}) for modulation index 0.3 (i.e. when the reference space vector is in layer-2) are shown in Fig. 18*a*.

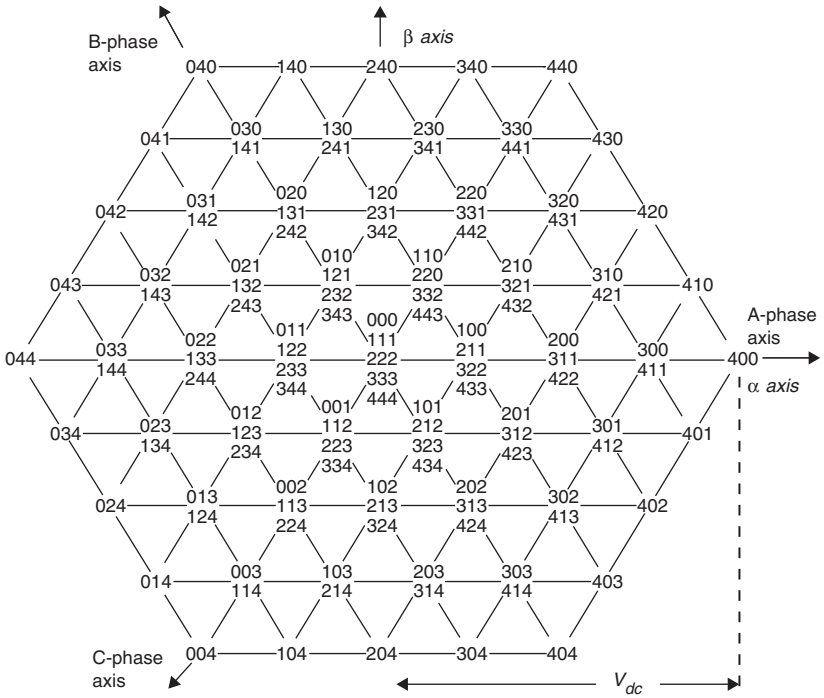


Fig. 16 *Five-level inverter states resulting into different inverter vector locations*

Table 4: Digital output from DSP I/O ports for various values of the carrier index, *I*

Carrier index, Ia	A3	A2
1	1	1
2	1	0
3	0	1
4	0	0

The phase-A current and the resultant phase voltage across phase-A winding of the induction motor are shown in Fig. 18*b*. The $(T^*_{as} + T_{offset2})$ waveform and offset time, $(T_{offset1} + T_{offset2})$ waveforms are shown in Fig. 18*c* (DAC output). These wave shapes are similar to simulated waveforms shown in Fig. 14.

The pole voltages V_{A20} and V_{A40}, when the modulation index is 0.6 (layer-3 operation) is shown in Fig. 19*a*. The corresponding phase voltage V_{A2A4} and phase-A current when the motor is at no load are shown in Fig. 19*b*. Figure 19*c* shows the $(T^*_{as} + T_{offset2})$ and $(T_{offset1} + T_{offset2})$ offset waveforms (DAC output). The total offset $(T_{offset1} + T_{offset2})$ and $(T^*_{as} + T_{offset2})$ waveforms are agreement with corresponding simulated waveforms shown in Fig. 14.

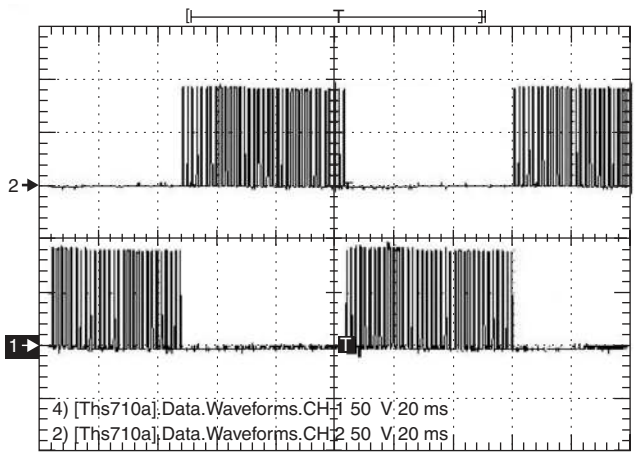
Similarly, the pole voltage waveforms, when the reference space vector is in the outer layer (modulation index = 0.85), are shown in Fig. 20*a*. The resultant phase voltage and phase current are shown in Fig. 20*b*. Figure 20*c* shows the $(T^*_{as} + T_{offset2})$ and $(T_{offset1} + T_{offset2})$ offset waveforms (DAC output). The total offset $(T_{offset1} + T_{offset2})$ and $(T^*_{as} + T_{offset2})$ waveforms match with the simulated waveforms shown in Fig. 14 for a modulation index of 0.83. Figure 21*a* shows pole voltages V_{A20} and V_{A40}, when the modulation index is 1.15. This corresponds to an overmodulation operation of the five-level inverter. Figure 21*b* shows the corresponding phase voltage V_{A2A4} and phase-A current when the motor is at no load. The motor is tested for speed reversal operation to test the performance of the PWM scheme in dynamic conditions. Figure 22 shows the phase-A current waveform when the motor is running in the forward direction and a speed reversal command is given.

5 Conclusions

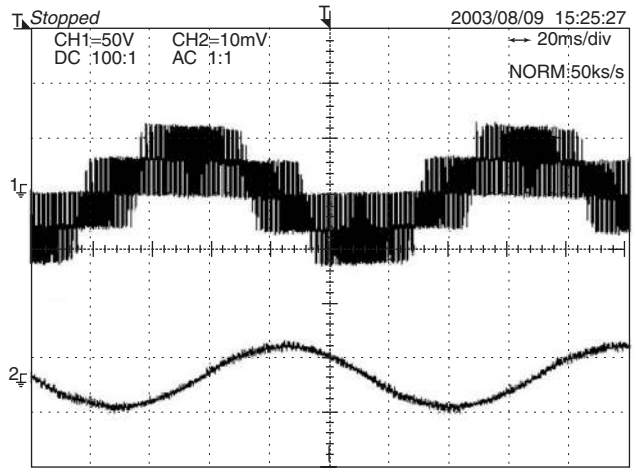
A voltage modulation scheme of the SVPWM has been presented for multilevel inverters. The centring of the middle inverter switching vectors of the SVPWM is achieved by the addition of an offset time signal to the inverter gating signals, derived from the sampled amplitudes

Table 5: Decoding table for leg A of five-level inverter

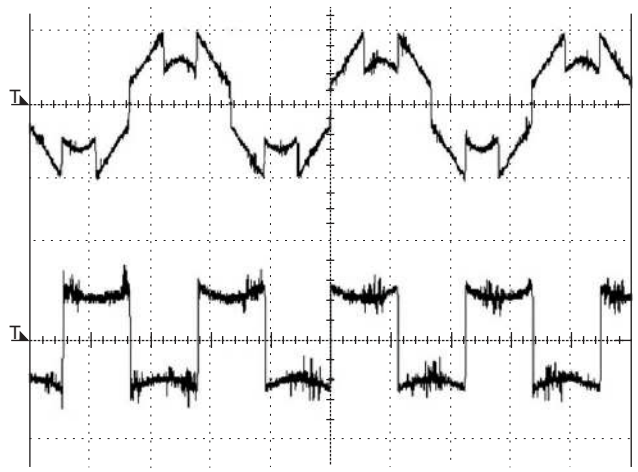
A3	A2	PWM_A	Voltage level	S11	S14	S21	S24	S31	S34	S41	S44
1	1	1	$V_{dc}/2$	1	0	1	0	0	1	0	1
		0	$V_{dc}/4$	0	1	1	0	0	1	0	1
1	0	1	$V_{dc}/4$	0	1	1	0	0	1	0	1
		0	0	0	1	0	1	0	1	0	1
0	1	1	0	0	1	0	1	0	1	0	1
		0	$-V_{dc}/4$	0	1	0	1	0	1	1	0
0	0	1	$-V_{dc}/4$	0	1	0	1	0	1	1	0
		0	$-V_{dc}/2$	0	1	0	1	1	0	1	0



a

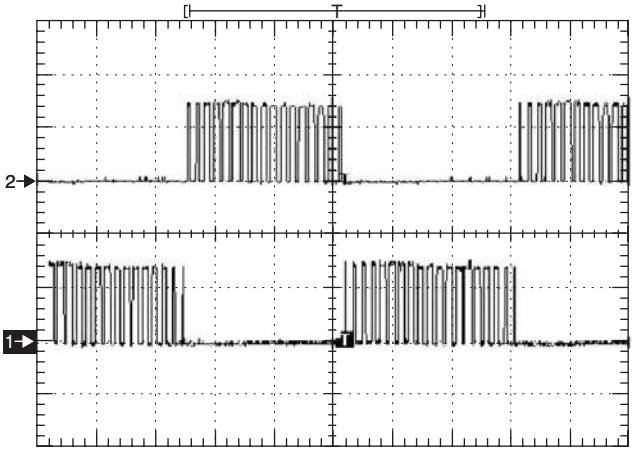


b

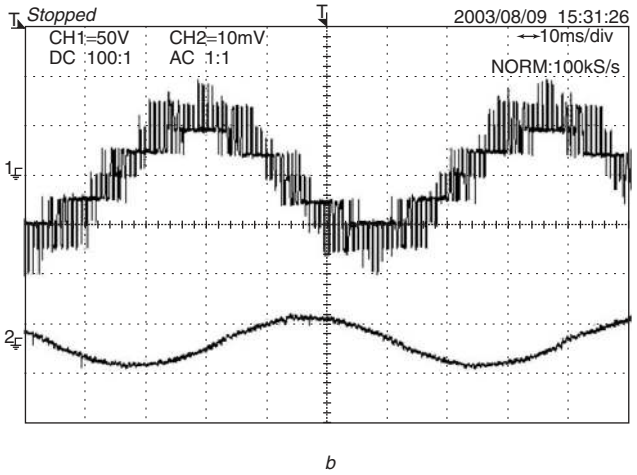


c

Fig. 17 *Modulation index 0.15 (layer 1 operation)*
a Pole voltage waveforms. upper trace: V_{A20}: *X*-axis: 1 div = 20 ms, *Y*-axis: 1 div = 50 V
Lower trace: V_{A40}: *X*-axis: 1 div = 20 ms, *Y*-axis: 1 div = 50 V
b Phase-A voltage and phase-A current waveforms. upper trace: V_{A2A4}: *X*-axis: 1 div = 20 ms, *Y*-axis: 1 div = 50 V Lower trace: I_A: *X*-axis: 1 div = 20 ms, *Y*-axis: 1 div = 2A
c Plot of $T_{AS} + T_{offset2}$ and offset time $T_{offset1} + T_{offset2}$ DAC output



a



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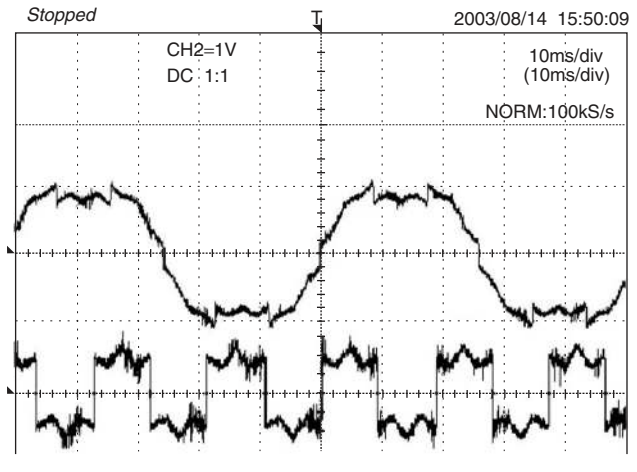
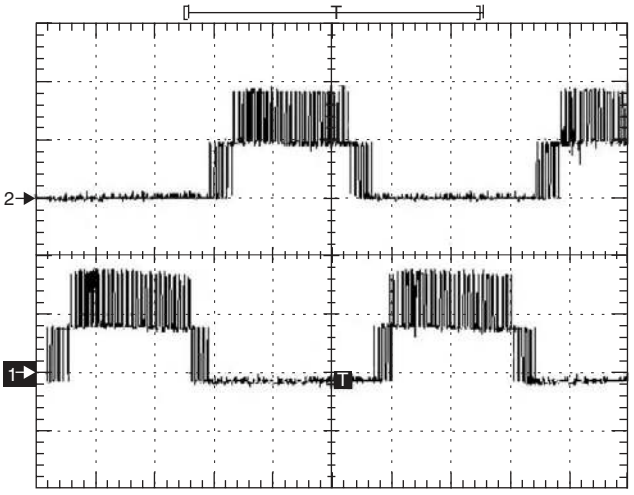


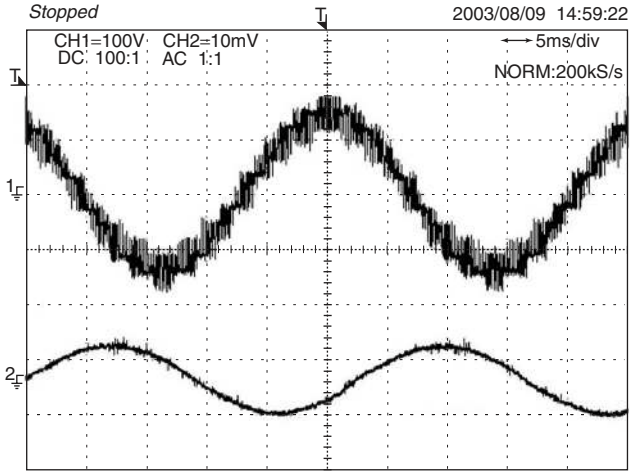
c

Fig. 18 *Modulation index 0.3 (layer 2 operation)*
a Pole voltage waveforms
upper trace: V_{A20}: *X*-axis: 1 div = 10 ms, *Y*-axis: 1 div = 50 V
lower trace: V_{A40}: *X*-axis: 1 div = 10 ms, *Y*-axis: 1 div = 50 V
upper Trace: V_{A20}, lower trace: V_{A40},
b Phase-A voltage and Phase-A current waveforms
upper trace: V_{A2A4}: *X*-axis: 1 div = 10 ms, *Y*-axis: 1 div = 50 V
lower trace: I_A: *X*-axis: 1 div = 10 ms, *Y*-axis: 1 div = 2A
c Plot of $T_{AS} + T_{offset2}$ and offset time $T_{offset1} + T_{offset2}$ for DAC output

of the reference phase voltages. The proposed SVPWM scheme covers the entire modulation range, including the overmodulation region. The PWM technique, presented in this paper, does not need, any sector identification, as is required in conventional SVPWM schemes. Complicated calculations for inverter switching vector times and look-up tables for selecting the inverter switching vectors are also avoided in the proposed scheme. This reduces the



a



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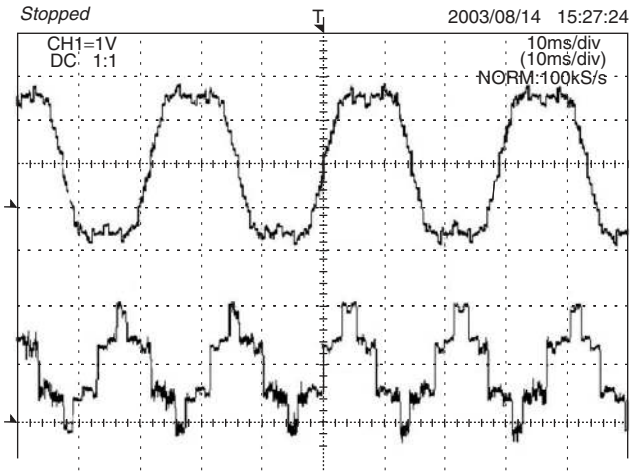
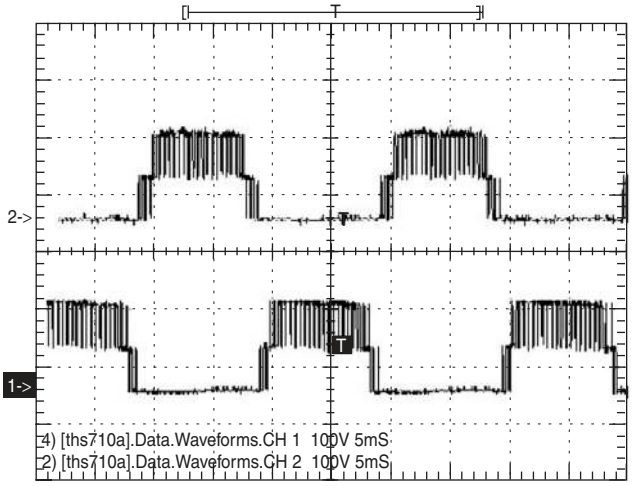


c

Fig. 19 *Modulation index 0.6 (layer 3 operation)*
a Pole voltage waveforms
upper Trace: V_{A20}: *X*-axis: 1div = 5 ms, *Y*-axis: 1 div = 100 V
lower trace: V_{A40}: *X*-axis: 1div = 5 ms, *Y*-axis: 1 div = 100V
b Phase-A voltage and phase-A current waveforms
upper trace: V_{A2A4}: *X*-axis: 1 div = 5 ms, *Y*-axis: 1 div = 100 V
lower trace: I_A: *X*-axis: 1 div = 5 ms, *Y*-axis: 1 div = 2 A
c Plot of $T_{AS}+T_{offset2}$ and offset time $T_{offset1}+T_{offset2}$ for DAC output



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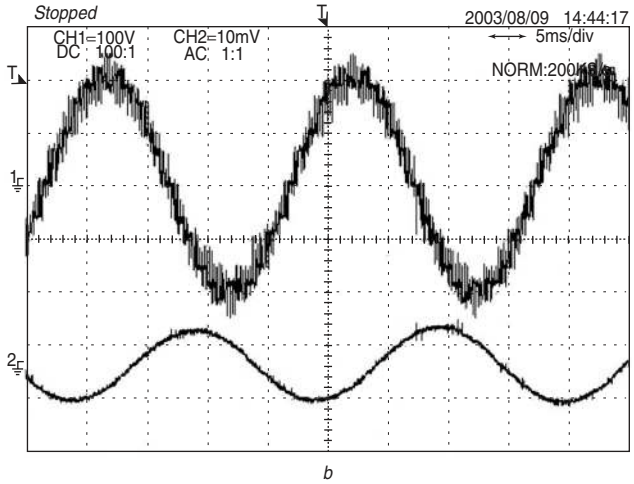

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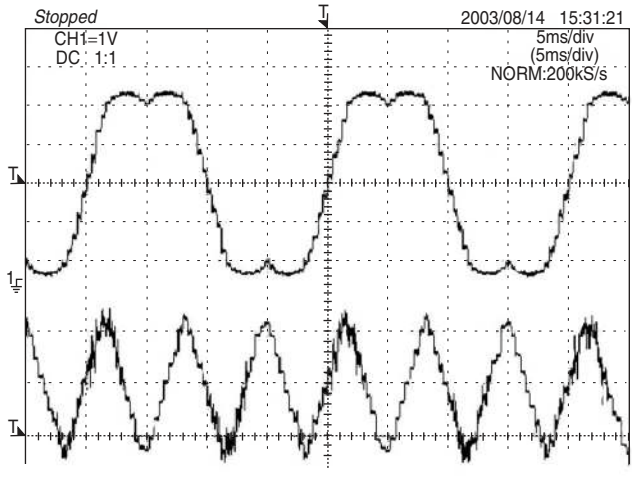

c

Fig. 20 *Modulation index 0.85 (layer 4 operation)*
a Pole voltage waveforms
upper trace: V_{A20}: *X*-axis: 1 div = 5 ms, *Y*-axis: 1 div = 100 V
lower trace: V_{A40}: *X*-axis: 1 div = 5 ms, *Y*-axis: 1 div = 100 V
b Phase-A voltage and phase-A current waveforms
upper trace: V_{A2A4}: *X*-axis: 1 div = 5 ms, *Y*-axis: 1 div = 100 V
lower trace: I_A: *X*-axis: 1 div = 5 ms, *Y*-axis: 1 div = 2 A
c Plot of $T_{AS}+T_{offset2}$ and offset time $T_{offset1}+T_{offset2}$, DAC output

computation time, required to determine the switching times for inverter legs, making the algorithm suitable for real-time implementation. The proposed SVPWM signal generation can be applied to any multilevel inverter configurations. In the present study, a five-level inverter drive with open-ended winding induction motor is used for experimental verification of the proposed technique, and the experimental results validate the proposed algorithm.

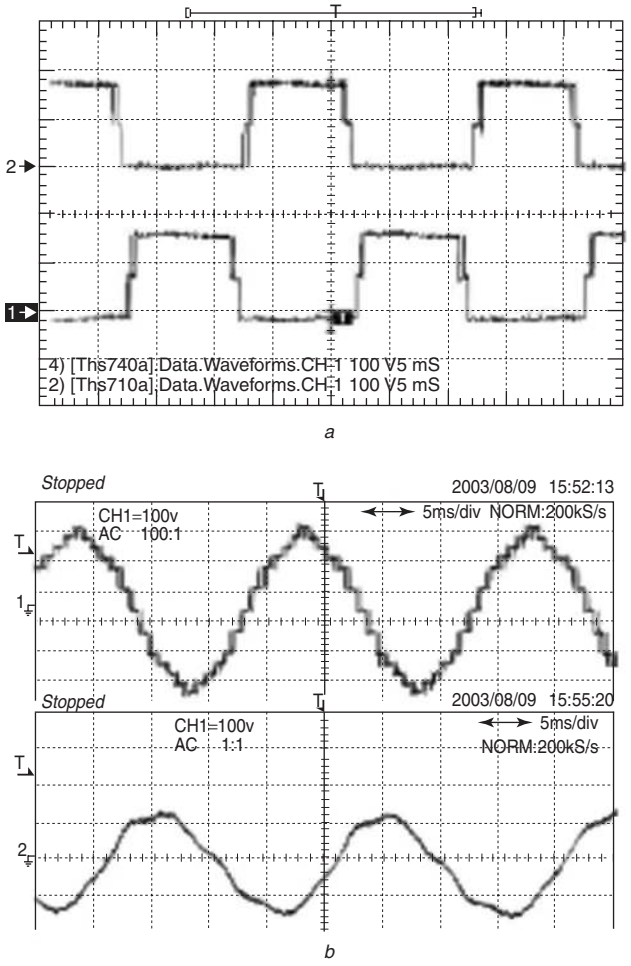

Fig. 21 *Modulation index 1.15 (overmodulation operation)*
a Pole voltage waveforms
upper trace: V_{A20}: *X*-axis: 1 div = 5 ms, *Y*-axis: 1 div = 100 V
lower trace: V_{A40}: *X*-axis: 1 div = 55 ms, *Y*-axis: 1 div = 100 V
b Phase-A voltage and phase-A current
upper trace: V_{A2A4}: *X*-axis: 1 div = 5 ms, *Y*-axis: 1 div = 100 V
lower trace: I_A: *X*-axis: 1 div = 5 ms, *Y*-axis: 1 div = 2 A

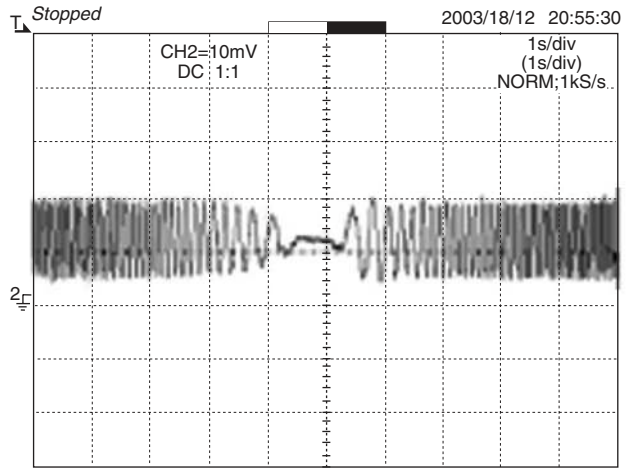

Fig. 22 *Phase-A current waveform for speed reversal from 40 Hz to −40 Hz*
modulation index 0.70
X-axis: 1 div = 1 s
Y-axis: 1 div = 2 A

6 Acknowledgement

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8 Appendixes

8.1 Algorithm for inverter leg switching time calculation for a n-level Inverter scheme

(1) Read the sampled amplitudes of V_{AN}, V_{BN} and V_{CN} for the current sampling interval.

(2) Determine the time equivalents of phase voltages, i.e. T_{as}, T_{bs}andT_{cs}

$$T_{as} = V_{AN} \times \frac{T_s}{V_{dc}/(n-1)},$$

$$T_{bs} = V_{BN} \times \frac{T_s}{V_{dc}/(n-1)}$$

$$T_{cs} = V_{CN} \times \frac{T_s}{V_{dc}/(n-1)}$$

where n is the number of levels.

(3) Find $T_{offset1}$ as $T_{offset1} = -(T_{\max} + T_{\min})/2$, where $T_{\max}$, $T_{\min}$ are the maximum and minimum of T_{as}, T_{bs} and T_{cs}.

(4) Determine T_{as}^{*}, T_{bs}^{*} and T_{cs}^{*} as $T_{as}^{*} = T_{as} + T_{offset1}$, $T_{bs}^{*} = T_{bs} + T_{offset1}$, $T_{cs}^{*} = T_{cs} + T_{offset1}$

(5) Determine the carrier indices *Ia, Ib* and *Ic* for A, B and C phases, respectively.

(6) Determine T_{a_cross}, T_{b_cross} and T_{c_cross} from (9) if n is odd or from (10) if n is even.

(7) Sort T_{a_cross}, T_{b_cross} and T_{c_cross} to determine T_{first_cross}, T_{second_cross} and T_{third_cross}.

The maximum of T_{a_cross}, T_{b_cross} and T_{c_cross} is T_{third_cross}.

The minimum of T_{a_cross}, T_{b_cross} and T_{c_cross} is T_{first_cross}.

And the remaining one is T_{second_cross}.

(8) Assign *first_cross_phase*, *second_cross_phase* and *third_cross_phase* according to the phase which determines T_{first_cross}, T_{second_cross} and T_{third_cross}.

(9) If $(T_{third\_cross} - T_{first\_cross}) > T_s$, go to step (13)

(10) Calculate $T_{offset2}$ as

$$T_{middle} = T_{third\_cross} - T_{first\_cross}$$
$$T_0 = T_s - T_{middle}$$

therefore $T_{offset2} = T_0/2 - T_{first\_cross}$

(11) Determine (T_{ga}, T_{gb} and T_{gc})

$$T_{ga} = T_{a\_cross} + T_{offset2,}$$
$$T_{gb} = T_{b\_cross} + T_{offset2,}$$
$$T_{gc} = T_{c\_cross} + T_{offset2}$$

(12) Go to step (1).

(13) Overmodulation

$$\text{If} \quad (T_{\_third\_cross} - T_{\_second\_cross}) < (T_{\_second\_cross} - T_{\_first\_cross})$$
$$T_{offset2} = -T_{\_first\_cross}, \quad \text{else}$$
$$T_{offset2} = T_s - T_{\_third\_cross}$$

(14) $T_{g\_first\_cross} = 0$, $T_{g\_second\_cross} = T_{g\_second\_cross} + T_{offset2}$ $T_{g\_third\_cross} = T_s$

(15) If $T_{g\_second\_cross} < 0$, $T_{g\_second\_cross} = 0$

(16) If $T_{g\_second\_cross} > T_s$, $T_{g\_second\_cross} = T_s$

(17) Determine T_{ga}, T_{gb}, T_{gc} by equating $T_{g\_first\_cross}$, $T_{g\_second\_cross}$ and $T_{g\_third\_cross}$ to T_{ga}, T_{gb} and T_{gc} depending on the phase, which determines first cross, second cross and third cross during the sampling interval.

(18) Go to step (1).

8.2 Induction motor parameters

Three-phase, rating = 1.5 kW

rated frequency = 50 Hz

Poles = 4

Rated voltage = 230 V

$Rs = 2.08\,\Omega$

$Rr = 1.19\,\Omega$

$Xs = 2.26\,\Omega$

$Xr = 2.26\,\Omega$

$M = 2.15\,\Omega$