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Spatially controlled electrostatic doping in graphene *p-i-n* junction for hybrid silicon photodiode

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Sufficiently large depletion region for photocarrier generation and separation is a key factor for two-dimensional material optoelectronic devices, but only a few device configurations have been explored for a deterministic control over the space charge region area in graphene with convincing scalability. Here we investigate a graphene-silicon *p-i-n* photodiode defined in a foundry processed planar photonic crystal waveguide structure, achieving visible—near-infrared, zero-bias, and ultrafast photodetection. Graphene is electrically contacting to the wide intrinsic region of silicon and extended to the *p* an *n* doped region, functioning as the primary photocarrier conducting channel for electronic gain. Graphene significantly improves the device speed through ultrafast out-of-plane interfacial carrier transfer and the following in-plane built-in electric field assisted carrier collection. More than 50 dB converted signal-to-noise ratio at 40 GHz has been demonstrated under zero bias voltage, the quantum efficiency could be further amplified by hot carrier gain on graphene-i Si interface and avalanche process on graphene-doped Si interface. With the device architecture fully defined by nanomanufactured substrate, this work demonstrates post-fabrication-free two-dimensional material active silicon photonic devices.

INTRODUCTION

Hybrid integration of a lower bandgap material on a large-scale silicon (Si) photonic circuit is demanded for the active components of today's optical interconnect systems.[1] The traditional Si photonics devices have the principle drawbacks, such as the low efficiency, limited bandwidth, and lack of on-chip laser.[2] Epitaxial growth of germanium or direct bonding of III–V materials on Si has been shown to be a promising route, but the high crystal quality in an active region demands a delicate control of material growth and integration technologies.[3–10] Atomic thin graphene (G), with zero bandgap and mechanically strong in-plane structure, can be easily transferred onto Si nanophotonic platform while maintaining high crystalline quality. Among various optoelectronic applications of G,[11–19] integrated G photodetectors, based on simple G-metal contacts, revealed many intriguing physics[20–26] and demonstrated highly competitive performance.[27–32] However, the built-in electrical field, which is responsible for the efficient separation of the photo-generated carriers, only exists in tens of nanometers near the G-metal contact. The absence of in-plane electric field in the bulk G region, where most of the electron–hole pairs are generated, leads to the dominant photothermal or bolometric photoelectronic response with poor on-off ratio (<1).[33,34] Dual back gate design for achieving G *p-n* junction has been reported, which provides high flexibility of controlling the intrinsic region width as well as tuning the voltage drop between the dual gates and thus the lateral built-in electric field. A responsivity of 35 mA/W was achieved at zero-bias conditions, with a 3-dB cutoff frequency of 65 GHz. However, this structure

requires sophisticated fabrication processes on the transferred G, thus not back-end-of-line fabrication compatible.[35] G contact engineering is highly desired for achieving high-speed signal integrity and scalability of the hybrid active photonic circuits.[36–39] G-semiconductor Schottky junctions exhibit exceptional photocurrent gain up to ~10^8 electrons per photon[23] and low dark current leakage. The responsivity of 4 A/W at 1300 nm and 1.1 A/W at 3200 nm is demonstrated based on hot carrier tunneling in G double-layer heterostructures.[40] However, the device speed has shown nanosecond scale, limited by the slow carrier diffusion process in non-depleted semiconductor materials.[23,40–43] Here we report a scalable device configuration of an in-plane G *p-i-n* junction utilizing the advantages of the two types of contact. The carriers confined in the limited density of states in G can be depleted through the two-dimensional junction of the hybrid device. The drift current dominant carrier transportation, both in Si and G, is key for simultaneously addressing the device's efficiency, signal integrity, and RF bandwidth.[44] The demonstrated device exhibits a responsivity of 11 mA/W at 1550 nm under zero bias with a response time of 15 ps. The converted 40 GHz photoelectric signal with 5 Hz bandwidth shows a high electrical signal-to-noise ratio of 52.9 dB.

RESULTS

The cross-sectional schematic of the lateral *p-i-n* junction with monolayer G coverage is depicted in Fig. 1a. The subwavelength photonic crystal (PhC) waveguide defined the intrinsic region

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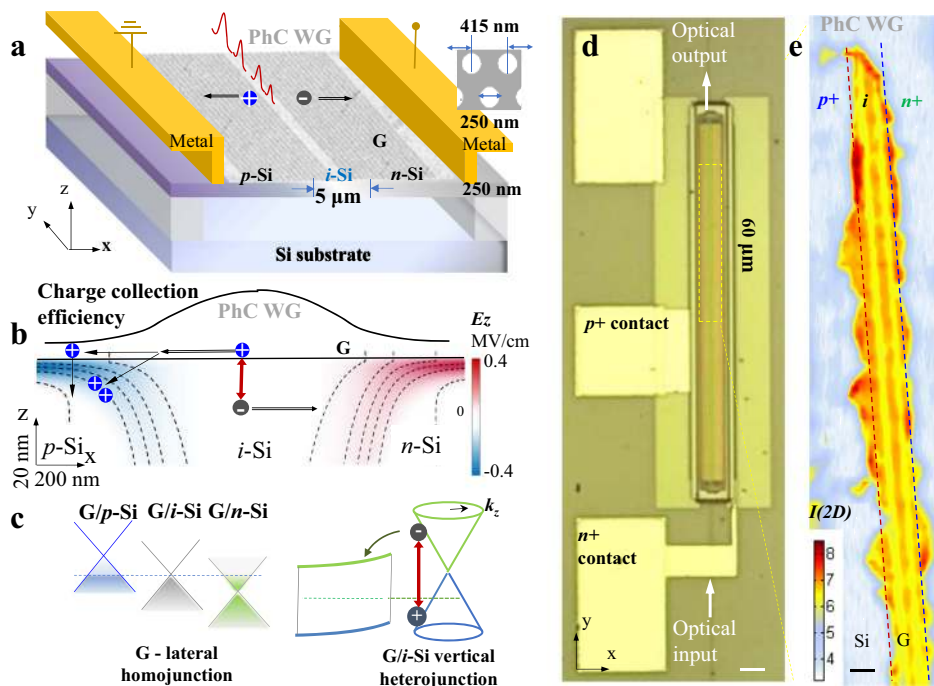Tiantian Li et al.

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Fig. 1 Efficient carrier separation in Van der Waals contacted graphene-silicon *p-i-n* junction. **a** A schematic diagram to show the graphene-CMOS photonic crystal waveguide integration. The metal electrodes contact to the *p* and *n* sides of silicon membrane through Graphene, contacting onto the silicon photonic crystal membrane, is electrically isolated from the metal electrodes. Inset: lattice constant and hole diameter of photonic crystal design. **b** Vertical electric field near the graphene-silicon interface. Arrows indicate the moving direction of carriers driven by the built-in electric field. The charge collection efficiency peaks around the center of the graphene layer. **c** The quasi fermi level of the lateral homojunction and the optical absorption mechanism for photon energy in the infrared range, with charge carrier collection by Schottky barriers. **d** Top view of the device. Scale bar: 20 μm. **e** Raman 2D peak mapping of isolated piece of single layer graphene on the intrinsic part of suspended silicon *p-i-n* junction. The two bars in the middle part reflects the substrate waveguides design. Scale bar: 3 μm

confines photons in 250 nm thick Si membrane, which is evanescently coupled to the directly contacted G layer. The photonic crytal structure is used to enhance the photoresponsivity.[45] G fully covers the intrinsic region and directly contacts both the *p*- and *n*-doped regions of Si. Aluminum electrodes, through etched oxide vias, form an Ohmic contact to the heavily doped regions of Si, and are isolated from G. The convergence of different work functions in the *p* and *n* regions produce an in-plane built-in electric field within both G and Si (Supplementary Materials I). In absence of an external bias, the built-in electric field in G can be introduced just by asymmetric source and drain contacts. The hybrid vertical-lateral junction allows effective charge collection within the device architecture with separate regions of photon absorption and carrier conduction/amplification (Fig. 1b). The photo-excited electro-hole pairs are efficiently separated by the built-in electric field. The charge collection peaks occur in the center of the G layer. While the Si layer thickness (250 nm) is only 5% of its width (5 μm), most of the photo-generated carriers are transferred to the G layer before reaching the *p*- or *n*-doped Si region. Under the bias voltage, carrier multiplication would take place along the G material and the graphene–silicon (G–Si) interface. Schematic energy diagrams of the vertical and lateral junctions are shown in Fig. 1c. The electrostatic doping from the silicon homojunction induces the Fermi-level shift in G, which is negative on *n*-Si, and positive on *p*-Si. The built-in electric field across the lateral *p-i-n* junction if formed along the G plane due to the different substrates inducing a Fermi-level difference in the G. Figure 1c also depicts the optical absorption mechanism for photon energy in the infrared (IR) range, with charge carrier collection through the vertical Schottky junction. The sufficiently long space charge region in the G *p-i-n* junction is achieved by direct contact between the Si *p-i-n* junction and the G material, which is essential for increasing the

photoresponse. The sufficient depletion region provides high flexibility for optical waveguide design with minimal overlap between waveguide mode and the lossy electrodes. The hot carriers generated in G with an energy higher than the Schottky barrier can be emitted into Si.[46] The top view of the CMOS processed active device layout is shown in Fig. 1d. The Raman *2D* peak intensity mapping illustrates the 60 μm long G coverage on the PhC waveguide (Fig. 1e).

Lateral carrier transportation along G *p-i-n* junction

For further studying of the carrier transport in the hybrid space charge region, micro photocurrent mapping is conducted across the *p-i-n* junction with the 532 nm 797 nW pump as shown in Fig. 2a. The normal incident laser has a spot size of ≈0.6 μm, with electrical current readout by matched probes on a scanning photocurrent microscopy setup (Supplementary Material II). The scanning photocurrent mapping is used to characterize the in-plane carrier transportation. In the intrinsic region, G dominates the photocarrier conduction. This is first observed from the symmetric photocurrent profile on the G covered section (red circles in Fig. 2a). In contrast to monolithic Si, the lower mobility of holes compared to the electrons shifts the photocurrent peak to the *p*-doped region (blue squares in Fig. 2a). Secondly, the G-dominated photocurrent transport is observed from the extended space charge region of ≈7.5 μm. The majority carrier determines the photocarrier conduction in the intrinsic region of the homojunction, with lateral charge collection (η_{L_pin}) empirically fitted by $e^{-(X-X_e)^2/L_e^2 - (X-X_h)^2/L_h^2}$. $L_{e/h}$ is the mean free path for the electrons/holes in the intrinsic region. X is the spatial location of the laser along the *p-i-n* junction, with $X_{e/h}$ defined as borders of the intrinsic region to *n/p* doped regions. At the highly doped part of the junction, as shown in Fig. 2a, the photocurrent decays
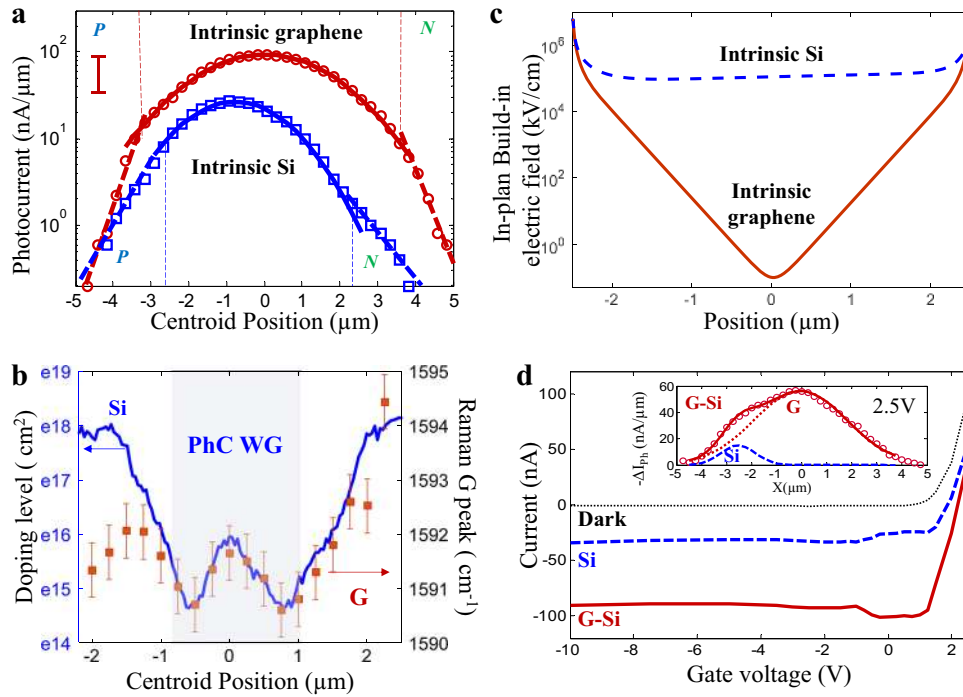
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Fig. 2 Photocurrent transportation in graphene *p-i-n* junction. **a** Scanning photocurrent microscopy across the silicon *p-i-n* junction with (red circles) and without (blue open squares) graphene, under 532 nm 797 nW pump excitation without gate nor external bias. Solid/dashed lines are Gaussian/exponential fits. The peak position of the photocurrent profile in the intrinsic region is determined by the mean free path of minority carriers. **b** Surface conductivity scan across the G–Si junction, with the position of the Raman *G* peak of graphene and substrate silicon doping level. The electrostatically formed homojunction in graphene is achieved through directly contacting to a silicon *p-i-n* junction. **c** The calculated built-in electric field along the *p-i-n* junction (*E_x*), for monolithic silicon device (dashed blue curve) and graphene supported by silicon *p-i-n* junction. **d** Current–gate voltage characteristics in dark (dotted black curve), as the laser spot on intrinsic silicon without (dashed blue curve) and with graphene coverage (red solid curve). Inset: the photocurrent map across the G–Si *p-i-n* junction at 2.5 V gate voltage. The convoluted profile (empty circles are experiments, and the red curve is Gaussian fit) can be decomposed into graphene (dashed red curve) and silicon (blue dashed curve) contributions

exponentially, with the decay constant determined by the minority carrier diffusion length.[47,48] Through curve fitting the model to the measured photocurrent profile in the intrinsic region, we found (1) the intrinsic region in the hybrid structure expands from 5 µm to 7.5 µm; (2) the diffusion length of the holes in the hybrid structure increases roughly from 2 to 3.5 µm comparing to the monolithic one (Supplementary Materials IV). A detailed collection of the carrier separation and characterization of the G homojunction is provided in Supplementary Materials IV & V. The doping profile of the substrate Si *p-i-n* junction is measured by electrical field microscopy (converted to an absolute value of doping concentration shown as a blue solid curve in Fig. 2b). The substrate-induced electrostatic doping in G is characterized by the Raman *G* peak wavenumber (solid red squares) (Fig. 2b).[46] The charge-induced doping variation leads to the formation of the built-in electric field of G contacting to the substrate Si *p-i-n* junction as shown in Fig. 2c. With fixed bias on *p* and *n* contacts, we also measured the back-gate dependent photon and dark current, composed of both Si and G responses (Fig. 2d). We found our device has a back-gate threshold voltage of 1.5 V and dark current is negligible below this voltage. The photocurrent profile is illustrated in the inset of Fig. 2d (red open circles), which can be decomposed into the Si transport component (blue dashed curve) and the G component (red dashed curve).

Figure 3a shows the measured photocurrent mapping across the G *p-i-n* junction from the wavelength of 442–832 nm. The photocurrent in the PhC waveguide region of the hybrid junction can be fitted well by our empirically model and verify the independence of the excitation wavelength for η_{L_pin} around the region of $X \approx 0$. The visible—near-infrared (NIR) enhancement of

the G-mediated external quantum efficiency (EQE), the ratio of incident photons to converted electrons, is described in Fig. 3b. In this heterostructure, Si is the absorber for the visible light. Efficient carrier transfer from Si to G is enabled by their band alignment (Fig. 1c). The overall EQE of the junction described below provides good corroboration with our experimental data (see also Fig. 3b):

$$EQE_{G-Si} = \left[A_{Si}(\lambda, I) \frac{G_0 R_{G-Si}}{R_{G-Si} + R_{Rec}} + A_G(I) F_e(\lambda, T_e) \right] \eta_{L\_pin}(x) \qquad (1)$$

EQE_{G-Si} is the product of the photocarrier generation efficiency of the vertical junction (in square bracket) and charge collection efficiency (CCE) of the lateral *p-i-n* junction (η_{L_pin}). Photocarrier generation efficiency is contributed by both the silicon slab (the first part) and the G layer (the second part). The silicon contribution is the product of the Si PhC slab absorptance (A_{Si}), possible gain (G_0) from the carrier transfer and impact ionization from Si to G,[49] and interfacial charge transfer efficiency of $R_{G-Si}/(R_{G-Si} + R_{Rec})$. R_{G-Si} is the built-in electric field enhanced interfacial charge transfer rate from Si to G. R_{Rec} is the surface dominant recombination rate in Si PhC. The charge transfer efficiency depicts the efficiency of the charge contributing to the photocurrent compared to all of the generated charge. The photothermionic (PTI) current[50] from G is the product of the G photon absorbance (A_G) and thermionic emission efficiency of the photo excited hot carriers from G to Si (modified Fowler's factor, F_e).[51] We first characterize the η_{L_pin} through comparing the visible band photocurrent of the monolithic and hybrid devices (Supplementary Materials IV and V). The characterized η_{L_pin} near the PhC waveguide region (in the middle of the intrinsic region of *p-i-n* junction) is then used to study the sub-bandgap PTI current in

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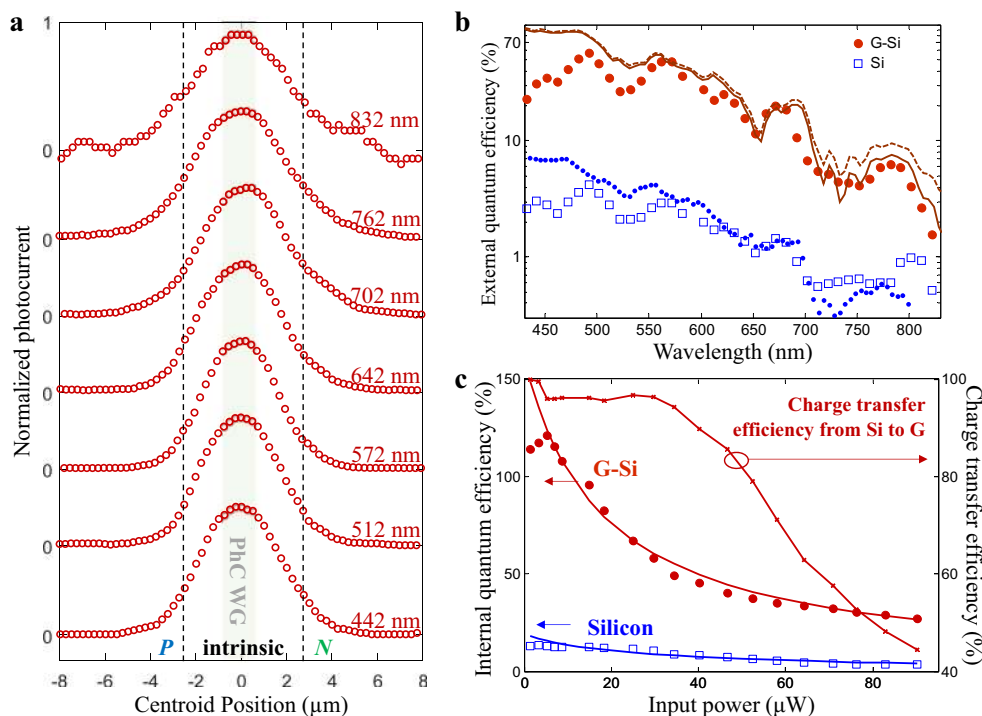Tiantian Li et al.

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Fig. 3 Wavelength and power dependence of photocurrent map. **a** Measured Photocurrent map across the graphene *p-i-n* junction from visible to near infrared wavelengths. The shadowed grey area highlights the PhC waveguide region. **b** Measured peak external quantum efficiency (EQE) versus wavelength for peak photocurrent of the graphene covered (red solid circles) and silicon part (blue empty squares) of the lateral junction. The spatial photocurrent profile is the same as shown in Fig. 2a. The absorption spectrum of 250 nm thick silicon photonic crystal structure is plotted in red solid curve. Single layer graphene would add 2% absorption (brown dashed curve). The dotted blue line is the theoretical prediction of EQE of intrinsic silicon photonic crystals without absorption. **c** Quantum efficiency for vertical junction of graphene-intrinsic silicon (brown solid circles), compared to the monolithic structure (blue empty squares). The internal emission efficiency from intrinsic silicon to graphene is plotted in the solid dot curve. The efficiency decreases at high optical power due to current saturation in graphene

G–Si junction, with pulsed NIR light excitation launched in-plane through PhC waveguide.

With Si as the dominant absorber in visible band, the photocurrent mapping profile is symmetric independent of the wavelength, indicating the G dominant carrier transportation across the hybrid *p-i-n* junction (Fig. 3a). An ≈10× enhancement of the EQE is observed comparing the hybrid to the monolithic device (Fig. 3b), as it benefits from the rapid photocarrier separation in vertical G–Si junction. The EQE spectra in the PhC waveguide region shows wavelength dependent oscillations, which originate from Fabry-Perot reflections in the air gap between suspended Si membrane and the bulk Si substrate. The spectra match finite-difference-time-domain simulations of the Si photonic crystal absorption are shown in the brown curves of Fig. 3b, with (dashed curve) and without (solid curve) contributions from G absorption. The incident power is kept below 1 µW throughout the spectral response calibration.

The built-in vertical electric field and the atomically abrupt heterojunction allows for efficient carrier separation of photo-excited electron–hole pairs. The transferred hot carriers across the abrupt heterojunction might be favorable for carrier multiplica-tion. The highest internal quantum efficiency (IQE) of the hybrid G silicon junction is 120% (Fig. 3c). Interfacial charge transfer efficiency describes the charge transfer efficiency on the G-*i* Si interface, which saturates at high optical power (Supplementary Materials IV). Charge transfer efficiency could be calculated as N_G/N_{Si}, where N_{Si} is the number of carriers generated per second in G Si hybrid structure, similar to the monolithic device; N_G is the number of transferred carriers from silicon into G layer per second. The calculated highest charge transfer efficiency shown in Fig. 3c is ~95%. Assisted by the vertical built-in electric field, the interfacial charge transfer rate ($R_{G–Si}$) is estimated to be about 100 GHz, which is similar to the values reported in literature.[52] The local recombination (R_{Rec}) of 20 GHz is much slower than $R_{G–Si}$[53] (details in Supplementary Materials IV). Considering the carriers transport time (with velocity of ~10^6 m/s across the intrinsic region of 5 µm), the response time is estimated to be 15 ps. A hydrofluoric dip is used to remove the native oxide on Si right before the G transferring to ensure the electrical contact on the interface (Materials and methods). The hydrogen-terminated crystalline Si surface in direct contact with G is demonstrated to be absent of Fermi-level pinning near the interface.[54] At low power input, ultrafast out-of-plane carrier separation leads to dominant G carrier transportation.

PTI response in vertical G–Si junction

The sub-bandgap photocurrent generation is driven by the one photon absorption induced PTI effect in G material, described by the second term in the square bracket in Eq. (1).[50] The ultrafast hot carrier dynamics in G has been studied with metal contacts or G double-layer heterostructure.[40,55] Here, we focus on PTI on G-*i* Si heterojunction. Photothermal excited hot carriers in the G and the subsequent interfacial hot carrier emission on the Schottky junction lead to a strong wavelength dependence of the photocurrent (Fig. 4a). With a good understanding of in-plan and out-of-plane carrier transportation, the photoabsorption mechanism of the NIR light can be distinguished for separate studies. For NIR light below the Si bandgap but above the barrier threshold of the Schottky junction, G is the dominant absorber through interband transitions. The out-of-plane photocarriers are collected by Si through emission of photoexcited hot carriers
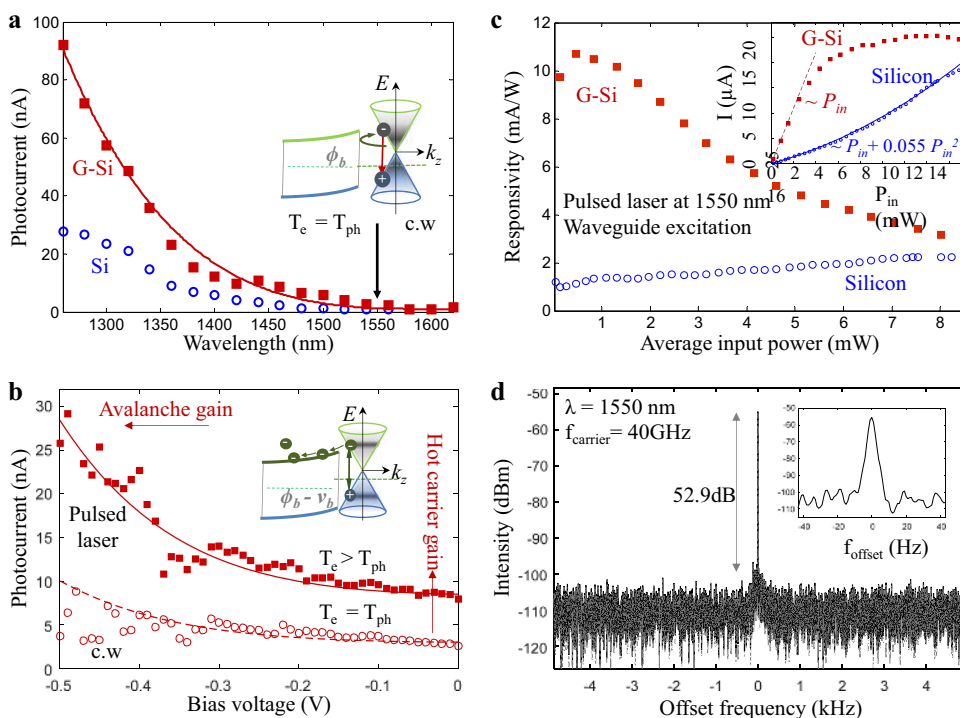
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Fig. 4 Photo-thermionic (PTI) effect in vertical graphene-silicon heterojunction. **a** Low power C.W. photocurrent spectrum of PTI process. Red squares and blue circles represent hybrid and monolithic devices. **b** Reverse bias voltage-dependent photocurrent characteristics for graphene–Si p-i-n junction under C.W. laser (empty circles) and subpicosecond pulsed laser (solid squares) illumination centered at 1550 nm. Inset: band diagram of PTI on graphene–Si interface and avalanche gain in Si. **c** Responsivity versus laser pulse power for silicon (red squares) and graphene (blue empty dots) samples with zero bias. The pulsed laser propagating in intrinsic region (PhC waveguide) is centered at 1550 nm. Inset: Photocurrent versus input power for devices with (red squares) and without (empty blue circles) graphene with in-plane excitation under zero bias. The dashed line is a linear relationship to the hybrid device, showing PTI dominant process at 1550 nm. The blue curve is a polynomial fit to the silicon device. **d** Microwave spectrum of the converted photoelectric signal with a center frequency of 40 GHz. Inset: the zoom-in spectrum of the center peak, with 5 Hz bandwidth and electrical signal-to-noise ratio of 52.9 dB

across the Schottky barrier.[51,56] As only the photocarriers with energy above the Schottky barrier height (ϕ_b) can be emitted to silicon, F_e in Eq. (1) exhibits strong wavelength dependence, and the NIR photocurrent spectrum (red squares in Fig. 4a) can be fitted by the model $F_e = C (\hbar\omega - \phi_b)^p$ (Solid red curve in Fig. 4a). Here C is a constant, $\hbar$ is the reduced Plank constant, ω is the frequency of incident light. $p = 3$ for Si. ϕ_b is the Schottky barrier height of G and Si ($\phi_b = \phi_{b0} - \Delta E(T_e)$), and can be reduced through hot carrier effect in G ($\Delta E(T_e)$). Under low power continuous-wave (C.W.) excitation, the Schottky barrier ϕ_{b0} is measured to be 0.76 eV through curve fitting (solid red curve in Fig. 4a). The one photon absorption in G with subsequent carrier emission on G–Si interface generates photocurrent spectrum distinguished from bare Si region (blue curve in Fig. 4a). Since atomic layer thin G has a thickness thinner than the mean free path of electron–electron scattering, the incident photons with energy above ϕ_b can effectively generate PTI carriers with sufficient kinetic energy to be transferred into Si, similar to the internal photo-emission process.[56,57] As the photon energy at 1550 nm is close to the Schottky barrier, most of the PTI carriers do not have enough energy to transfer into Si with low power C.W. excitation (inset of Fig. 4a).

Pulsed laser excitation with higher peak power increases the thermal energy of the electron gas, and thus reducing the effective ϕ_b (Fig. 4b). The pulse duration of the excitation laser is shorter than the carrier lifetime in G, allowing hot carriers with higher electronic temperature (T_e) to play a role in the photocurrent, before reaching the thermal equilibrium with the carbon lattice through the electron–phonon scattering. The peak power effectively coupled onto G can be up to 10 kW cm^{-2}, leading to estimated transient T_e of 600 K.[50] Higher T_e increases

the portion of the hot carriers that can effectively emit into G to Si (Inset of Fig. 4b). The extra hot carrier contribution with pulsed laser excitation leads to a 3.2× enhancement of photocurrent (correspondent to $\Delta E(T_e) = 24.5$ meV), compared to C.W. light with the same wavelength and average power (Supplementary Materials VII). Photocurrent enhancement factor from the pulsed laser is weakly dependent on the reverse bias, indicating hot carrier generation and amplification are independent processes in the multi-junction device. The reverse bias enhanced built-in electric field on G-doped Si can lead to possible avalanche gain (Fig. 4b). The avalanche mechanism can be attributed to the carrier multiplication process in G-p Si interface. The carrier multiplication in biased G is less likely, as the lateral built-in electric field is much weaker than the vertical G-doped Si interface (further discussed in Supplementary Materials VII). The reverse bias dependent photocurrent lineshape can be fitted by the avalanche multiplication model of $M = 1/(1 - (V_R/V_{BD})^k)$.[30] The breakdown voltage (V_{BD}) and the power coefficient k are fitted to be −0.63 V and 3.2 respectively. $M = 4.18$ is achieved as V_R set at −0.5 V bias.

To better understand the photon absorption mechanism, we compare the power dependent photocurrent between monolithic and hybrid devices (Fig. 4c). The inset of Fig. 4c distinguishes one-photon absorption in G hybrid device (solid red squares) from multi-photon absorption in Si devices (open blue circles). The dashed red line is the linear fit for a hybrid sample at low optical power. The responsivity in the linear region is characterized to be 11 mA/W (EQE$_{G–Si}$ = 8.8%). At higher incident power (more than 1 MW cm^{-2}), the photocurrent reaches the current saturation threshold in G. An opposite trend of power dependence is observed in monolithic Si devices, where the two-photon absorption leads to enhanced responsivity at higher incident

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Table 1. Performance matrix of graphene-based photodetectors at room temperature

Device configuration	Scalability/fabrication	IQE	SNR	Response time	SCR in G
G-metal heterojunction[36]	N/EX	87% (NIR)	0.64 dB	3 ps[a]	–
Graphene-WSe$_2$ heterojunction[27]	N/EX	>70% (759 nm)	2.2 dB	5.5 ps[b]	VJ
G-metal heterojunction[29]	Y/CVD		16 dB	13.1 ps[a]	–
G-metal heterojunction[28]	Y/CVD	60% (1550 nm)	25 dB	24 ps[a]	–
G p-n homojunction[35]	N/EX	High	>25 dB	15 ps[a]	80 nm
G/Si p-i-n heterojunction (this work)	Y/CVD	18% (1550 nm) 120% (532 nm)	52.6 dB	15 ps[a]	>5 μm
Si p-i-n homojunction (control sample)	Y	NA	High	60 p 60 ps[b]	–
Ge/Si SACM APD[4]	Y	16% (1300 nm)	20 dB	80 ps[b]	–
G-Si heterojunction[60]	Y/CVD	65% (Visible)	High	1 ms[b]	VJ

G graphene, *Si* silicon, *SNR* signal-to-noise ratio, *SCR* space charge region, *EX* exfoliation, *CVD* chemical vapor deposition, Graphene absorption mechanism is meant for near-infrared light, *VJ* vertical junction, *NIR* near-infrared
[a]RC constant limited
[b]Carrier transit time limited

power ($0.055\ P_{in}^2 + P_{in}$, where P_{in} is the input power). The polynomial relation (solid blue curve in the insert of Fig. 4c) represents the collective photoresponse from two-photon absorption in Si (the first term) and linear absorption through mid-gap defect states in Si (the second term).

Through the 4.18 avalanche gain of our device and the slow light effect in photonic crystal structure (≈4 times[45]), the 60 μm long hybrid PhC waveguide is promising to achieve the photoresponsivity of 183.92 mA/W ($11 \times 4.18 \times 4$ mA/W), given the η_{L_pin} of 20% near the waveguide region (estimated from Fig. 3a). Through reducing the intrinsic region width to 1 μm, η_{L_pin} can be improved to be 89% according to the model. Numerical calculation show that approximately 24% of the optical power is absorbed by the G layer along the 60 μm long waveguide.[58] The interfacial IQE at the 1550 nm is derived to be 18%.

The RF bandwidth of more than 50 GHz is estimated from the sum of charge transfer time on the heterojunction and the 12 ps resistance-capacitance constant.[59] The estimated RF bandwidth is verified through the measured S21 (Fig. 4d), where the 3-dB cut-off frequency is well beyond the 40 GHz instrumental limit.[59] With 40 GHz modulation on the 1550 nm incident light, the converted RF signal only has 5 Hz linewidth of the carrier and 52.9 dB signal to noise ratio (SNR) as shown in the inset of Fig. 4d. The devices have low noise floor given the zero-dark current at zero bias operation. Compared to other G photodetectors, the PTI effect in vertical junction, in combination with low noise carrier transportation along the lateral p-i-n junction, lead to the highest SNR (Table 1) with zero bias operation. Higher responsivity and operation speed can be easily achieved in other structures, as the photothermal or bolometric effect leads to light intensity dependent resistance change in G. However, the on-off ratio stays poor without effective separation of carriers.[28,36] In the visible wavelength, the G–Si p-i-n heterojunction demonstrated a much higher efficiency comparing with the G-WSe$_2$ heterojunction (70%)[27] and G–Si heterojunction (65%).[60] The additional avalanche process enables additional gain in our devices. The working principle is similar to the conventional separate absorption, charge, and multiplication (SACM) APD structure,[4] where the separation of photocarrier generation and avalanche process can maintain the high SNR with extra gain at reverse bias.

DISCUSSION

We demonstrated waveguide integrated G–Si p-i-n junctions with low dark current, efficient photocarrier transport and ultrafast response. Vertical type-I band alignment between G and Si enable a broad space charge region for efficient carrier separation and

drift-current dominant carrier transportation in the two-dimensional junction. EQE of Si is improved on average eight times over the visible band, through efficient separation both across and along the hybrid vertical and lateral G–Si heterojunctions. The interfacial IQE of 120% has been realized at visible wavelengths with silicon as the absorber. In the NIR region, $EQE_{G–Si}$ of 8.8% (IQE of 18%) can be further improved through junction design, slow light enhancement and avalanche gain. The ultrafast response time promises the RF bandwidth of the device to be larger than 50 GHz. Under zero bias operation, the converted 40 GHz RF signal has only 5 Hz linewidth and more than 50 dB SNR.

METHODS

Device fabrication

The horizontal/lateral p-i-n diode configuration in Si membrane is fabricated in CMOS foundry by ion implantation: boron for p-type (5×10^{18} cm^{-3}, mobility 70.8 cm^2/V-s, resistivity 8.8 mΩ cm) and phosphorus for n-type (5×10^{18} cm^{-3}, mobility 115 cm^2/V-s, resistivity 5.4 mΩ cm). The intrinsic region is lightly p-doped (10^{16} cm^{-3}, mobility 1184 cm^2/V-s, resistivity 0.53 Ω cm). The surface roughness of the Si is on the scale of angstrom meter. The photonic crystal structure is defined by 248 nm deep-ultraviolet photolithography, followed by reactive ion etching to produce the hole radius of 124 ± 2 nm, with a lattice constant of 415 nm. Next, an oxide cover layer is deposited for the metal insulation. Vertical vias in the top oxide layer are patterned and etched for the contact regions, followed by standard aluminum metallization for direct contact to the heavily doped Si regions. The metallization is electrically isolated from the G layer. Chemical vapor deposition (CVD) G is grown on copper foils and transferred onto substrates using standard processing procedures. Dilute hydrofluoric acid dip is used right before the G transferring, to remove the surface oxide and achieve direct contact between G and Si photonic crystal membrane. After the G transfer, the samples are exposed to air several months throughout the measurement and still function well. Any extra native oxide thickness of non-G-covered exposed region is probed by Fourier transform infrared spectroscopy and compared to the regions covered by G.

Optical measurements

In photocurrent mapping, a supercontinuum laser source (NKT photonics) covering the whole visible bandwidth is used to characterize the photocurrent and EQE. The sample is mounted on a confocal optical microscope with a two-axis scanning mirror, with power and wavelength control (Supplementary Materials II). Vertical (z-axis) out-of-plane coupling to the sample is used for the supercontinuum photocurrent measurements. The wavelength dependent loss of the mirrors and objective are well calibrated for deriving the effective optical power coupled onto the chip. The laser spot size is less than 1 μm. Raman spectra were collected by

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coupling the light scattered from the sample to an inVia Raman spectrometer through a ×100 objective (Renishaw). For measuring the hot carrier effect at telecommunication bandwidth, a pulsed laser (0.5 ps duration, 20 kW cm^{-2}, 10 MHz repetition rate) and C.W. laser with the same average power and center wavelength (1550 nm) are coupled into the PhC region for comparison (Fig. 4b).

Numerical simulations

A three-dimensional finite-difference-time-domain method was used to calculate the light absorption in the Si photonic crystal membrane suspended on a Si substrate. The vertical spatial resolution was set at 1 nm.

AUTHOR CONTRIBUTIONS

T. Li and T.G. performed the experiment, analyzed the data and wrote the manuscript. D.M. performed the small signal analysis and modeling for the RF response. T.G. designed the silicon nanophotonic layout under the guidance of C.W. W. H.H., Y.D., and Z.H. performed the high-speed testing. R.G., T. Low performed the numerical simulations of electrostatic field distribution, and T.G. performed optical simulations. N.W.P. and J.H. prepared CVD G sample. G.Q.L. fabricated the silicon photonic devices.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-018-0080-4).

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