SPICE Compact Modeling of Bipolar/Unipolar Memristor Switching Governed by Electrical Thresholds

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***Abstract*—In this work we propose a physical memristor/resistive switching device SPICE compact model, that is able to accurately fit both unipolar/bipolar devices settling to its current-voltage relationship. The proposed model is capable of reproducing essential device characteristics such as multilevel storage, temperature dependence, cycle/event handling and even the evolution of variability/parameter degradation with time. The developed compact model has been validated against two physical devices, fitting unipolar and bipolar switching. With no requirement of Verilog-A code, LTSpice and Spectre simulations reproduce distinctive phenomena such as the preforming state, voltage/cycle dependent random telegraph noise and device degradation.**

***Index Terms*—Memristor, RRAM, ReRAM, Variability, RTN, Degradation, SPICE, Compact Model, Multi-level, Circuit Simulation, Temperature**

I. Introduction

Resistive switching (memristor) technologies are a promising part of next-generation nonvolatile memory. Their low power consumption, high density, fast operation and great endurance, as well as the integration capabilities with standard CMOS circuitry put memristive technologies under the spotlight. However, resistive random access memory (ReRAM or RRAM) is only one of the several applications where memristor technology has promising applications. Memristor based reconfigurable hardware, material-implication logic design or *neuromemristive* systems -neuromorphic computing using memristors- provide a solid alternative for standard CMOS circuits.

Close attention has been given to the fabrication of smaller, faster and more reliable resistive switching devices, using both oxide and semiconductor materials. Furthermore, major efforts have been made to characterize and correctly model those devices' behavior, depending on the properties of the materials and their fabrication conditions.

Previous works [1], [2] have accurately studied and reviewed the electrical behavior of memristor devices, gathering information of their internal dynamic processes for the design of a compact model. This is important because the creation of subcircuit compact components ready to be used by SPICE-like circuit simulators is a key issue for resistive switching based architecture design, since the trade-off between accuracy and simulation length becomes a critical factor when a large number of cells are computed within crossbars or substantial neural networks.

Considering the memristor as a two terminal device, insight into a model description can be found through two different approaches. Physical compact models rely on the description of current-voltage relationships together with their dependence on a given set of internal variables (conductive filament geometry, dopant volume elongation, ion migration probability, tunneling distances, etc.) matching the characteristics of a specific physical device. Depending on the grade of complexity, physical approaches include a broad variety of models, from the simpler and more flexible ones that are more inaccurate [3]–[5], to the more accurate but complex ones able to model the physical behavior with high precision [6]–[10]. The compendiums [1], [2] describe in more detail examples of both accurate and inaccurate models. Consequently, physical models that match different devices generally present accuracy problems, while complex approaches, with a suitable fitting of the physical component behavior, can fit only a narrow set of devices. Additionally, as the associated computational load increases with the model complexity, the trade-off between speed and accuracy restricts the use of some of the models. Moreover, in some cases the high non-linearity of the model behavior requires extremely short simulation time steps, cluttering the transient computation, and occasionally leading to convergence problems related to hard-switching conditions [1].

On the other hand, phenomenological compact models focus on fitting the electrical magnitude relationships, and describing their evolution using mathematical variables which are not necessarily related to the physical variables. Phenomenological approaches obtain a broad flexibility regarding the range of described devices [1]. More recent solutions update and improve earlier versions such as [11]–[13], standing as a powerful solution for general modeling, and an effective application to neuromorphic computing [14].

In this work we present a novel solution based on the independent modeling of the device conduction mechanisms and device state. The proposed model fully relies on physical magnitudes and their inter-relations, defining the tuple electri-

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TABLE I
MODEL COMPARISON AGAINST BEST WELL KNOWN MODELS

Model	Physical or Phenomenological	Require Verilog-A	Bipolar or Unipolar	Variability & Degradation	State Magnitude	Multilevel Aware	Pristine State Aware
Proposed	Physical	No	Both	Static and dynamic	Consumed Energy	Explicit	Yes
Several Universities [7], [8], [10]	Physical	Yes	Bipolar	Static	CF elongation	CF mplicit	No
Yakopcic's [11], [14]	Phenomenological	No	Both	Static	Auxiliar	Adaptable	No
Biolek's and Dopant Drift [3], [5], [6]	Physical	No	Bipolar	No	Dopant area length	No	No
TEAM's [13], [15]	Physical	Yes	Bipolar	No	Dopant area length	Adaptable	No

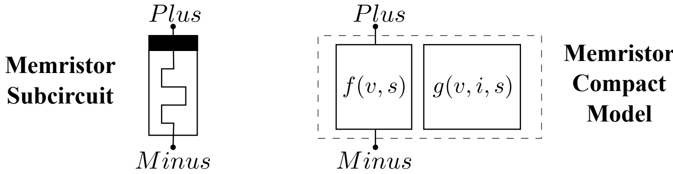


Fig. 1. Proposed Compact Modeling Design: bi-port component independently handling conduction module (left) and state module (right).

cal and resistive switching behavior.

While voltage and current thresholds are supported, the state modeling bases the device switching on electrical charge, flux or energy thresholds. It is applicable to both bipolar and unipolar devices, widening the range of devices that can be described, and therefore the proposed approach rivals in flexibility with the most suitable phenomenological approaches [11], [14]. In turn the conduction module accurately fits the conduction mechanisms of the physical component.

Fully compatible with SPICE simulators, the presented model does not require implementation in Verilog-A or CMI to accurately match physical components. Although components written in Verilog-A or CMI allow more complex schemes to be emulated, they have a major drawback: widely used SPICE simulators do not allow Verilog-A or CMI code execution, restricting its simulation on several platforms.

The main contributions of the proposed model are as follows:

- Accurate modeling of dynamic resistance cleanly mimicking physical device response.
- Effective switching behavior for bipolar/unipolar devices.
- Availability of cycle and switching event count information for all time, becoming a resource for additional characteristics such as variability.
- Variability awareness.
- Provision of variability dynamics and resistive state retention handling, defining how the device degrades through time/cycle stress.
- Explicit support for multi-level storage. Unlike CF based models [7], [8], [10], the explicit definition of multiple states allows more detailed level descriptions. This also allows the modeling of *Pristine State* -the initial *High Resistive State (HRS)* prior any electroforming-.
- The full source code for those bipolar and unipolar devices, together with additional materials can be found at http://vlsi.die.upm.es/memristor_spice_model.

Table I summarizes the key characteristics of the proposed model comparing it against the best well known compact models presented in literature.

The paper is structured as follows. First, we present the proposed memristor model. Section III describes the variability handling methods included within the modeling. The simulation results fitting two different physical devices are shown in Section IV. Some concluding remarks can be found in Section V. Finally, Appendix A includes `LTSPICE` source code describing a multilevel bipolar memristor.

II. PROPOSED MODEL

The proposed model is composed of two different subcomponents which allow matching to the device behavior (Figure 1). The *Conduction Module*, addressing the memristor component interface through the ports *Plus* and *Minus*, models the dynamic resistance; in turn, the *State Module* handles the device state.

The component behavior is defined by the transient signal set, composed of the input voltage $v(t)$, the current flowing through the device $i(t)$, and the device state vector $s(t)$. This vector contains all the information related to cycle count, switching thresholds, energy and resistance state. In this paper we will simplify the notation of the electrical and state equations, and their dependence on time will become implicit: consequently, as an example, $v(t)$ will be denoted as v.

The equations describing the signal relation of the different submodules can be written using the generalized system

$$\begin{aligned} i &= f(v,s) \\ \dot{s} &= g(v,i,s). \end{aligned} \tag{1}$$

This equation system matches most devices' behavior [1], and thereby both physical and phenomenological models specify f and g functions to define how the model runs.

A. Conduction Module Modeling

The Conduction Module is responsible for the computation of the current which flows through the device. This depends on the voltage and the memristor state. Denoting the first component of the state vector $s^{(1)}$ as the discrete value referring the device level, within our proposed model the current function

$$i = f(v,s) \tag{2}$$

takes the form, for different N conduction levels,

$$i = \begin{cases} f_1(v,s) & \text{if } s^{(1)} = s_1 \\ f_2(v,s) & \text{if } s^{(1)} = s_2 \\ \dots & \\ f_N(v,s) & \text{if } s^{(1)} = s_N. \end{cases} \tag{3}$$

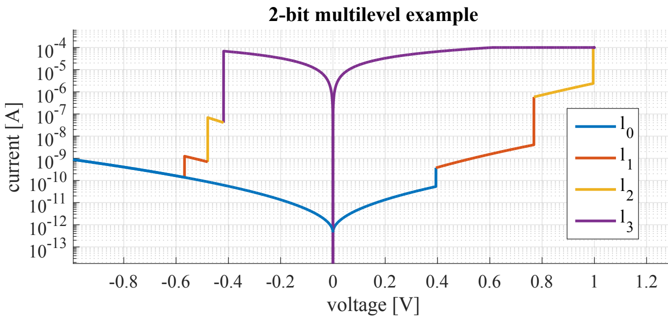


Fig. 2. Example of a simulated 2 bit multilevel device, with three different Schottky (l_0, l_1 and l_2) and one ohmic conduction schemes (l_3).

This approach, completely covering the device state design space, allows multilevel device modeling such as [16]. Figure 2 shows an example of a simulated 2 bit multilevel memristor using the proposed scheme. The bipolar device experiences three partial *SET* events followed by their corresponding partial *RESETs*. Compared against different approaches with no explicit multi-level definition (Table I), the proposed model eases tuning of each level's conduction properties, including degradation and variability. As an example, the Schottky characteristics exhibited in Figure 2 were captured with no effort.

For a device with two-resistance levels and no pristine state description, equation (3) gets simplified to the basic system

$$i = \begin{cases} f_{on}(v,s) & \text{if } s^{(1)} = s_{on} \\ f_{off}(v,s) & \text{if } s^{(1)} = s_{off} \end{cases} \quad (4)$$

where f_{on} and f_{off} are the low and high resistance state currents, respectively.

The state currents f_j are modeled using different methods depending on the specific device. As an example, low resistance state dependence on voltage is usually simplified to a single resistance with temperature dependence in both oxide-based [7], [8], [17] and semiconductor based devices [18]. However, the model accepts different schemes to be used, such as an in-series diode-resistance approach, improving the simulation accuracy [19].

Even though some works model the involved conduction mechanisms of the higher resistance states using diode-resistance schemes [9], in most cases the voltage-current relation is described by basic conduction processes like the ones described in Table II. Modeling such processes using behavioral current/voltage sources allows us to accurately mimic the device behavior. Some devices require complex schemes where not only individual conduction process take place but concurrent processes occur [17]. Our model fully covers this requirement allowing multi-contribution schemes, where distinct current sources contribute to define the global one.

In case the device conduction process is not defined by an analytical function, or further measurement data is required, we could model the varying resistance of the device as a behavioral resistor. The behavioral resistor value is determined by an auxiliary function defined using the circuit simulator *user defined functions* syntax [25]. Taking advantage of the

TABLE II
EXAMPLES OF CONDUCTION PROCESSES COMPATIBLE WITH SPICE-LIKE BEHAVIORAL SOURCES

Process	**Expression**
Trap Assisted [20]	$J \propto a_1 \left(\frac{V}{d}\right)^{a_2}$
Generalized Tunneling Temperature Dependent (II) [7], [8]	$J \propto exp\left(\frac{-g}{g_0}\right) sinh\left(\frac{V}{kTV_1}\right)$
Tunneling [6]	$J \propto \mathscr{E}^2 exp\Big[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar\mathscr{E}}\Big]$
Schottky Thermionic [17], [18], [21]	$J = A^{**}T^2 exp\Big[-\frac{q\left(\phi_B - \sqrt{\frac{q\mathscr{E}}{4\pi\epsilon}}\right)}{kT}\Big]$
Poole-Frenkel [22], [23]	$J \propto \mathscr{E}\Big[-\frac{q\left(\phi_B - \sqrt{\frac{q\mathscr{E}}{\pi\epsilon}}\right)}{kT}\Big]$
Ohmic [17], [18], [24]	$J \propto \mathscr{E} exp\Big[-\frac{\Delta E_{ac}}{kT}\Big]$
Space-charge-limited [24]	$J \propto \frac{9\epsilon\mu V^2}{8d^3}$
QPC [2]	$I = \frac{2e}{h}\left\{eV + \frac{ln}{\alpha}\left[\frac{1+exp\left(\alpha(\phi_B-\beta eV)\right)}{1+exp\left(\alpha(\phi_B+(1-\beta)eV)\right)}\right]\right\}$

V and d are the voltage applied between the electrodes and the insulator thickness respectively.
$\mathscr{E}$ refers to the electric field, A^{**} stands for the effective Richardson constant.
g, g_0, V_0, V_1 is the gap distance and matching parameters.
ϕ is the materials barrier height, while ϵ is the insulator permitivity.
ΔE_{ac} is the activation energy of electrons.
α and β are parameters related to barrier thickness and fraction of dropped voltage respectively.

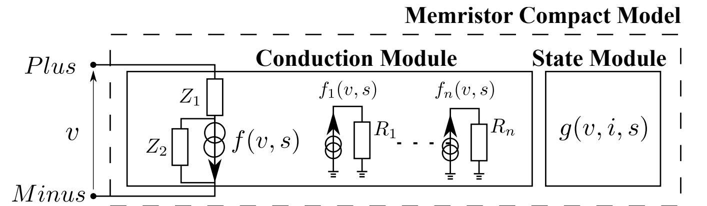


Fig. 3. N-state conduction module scheme using behavioral sources.

SPICE simulator capabilities, the behavioral resistor may refer a piecewise (*PWL*) function defining the voltage and state dependent resistance based on previous voltage-current measurements that build up the pairs $v_i - r_i$.

Summarizing, our proposed model accepts individual/cumulative conduction schemes with which it models the current flow at multilevel states for different devices/technologies. The general subcircuit of a memristor device with N different resistive levels modeled using N independent current behavioral sources is shown in Figure 3. This approach allows us to include additional helpful effects such as the compliance current or control sentences shown in [1]. An example of a constraint current source modeling an N state device using the approach described in Figure 3 would be represented by

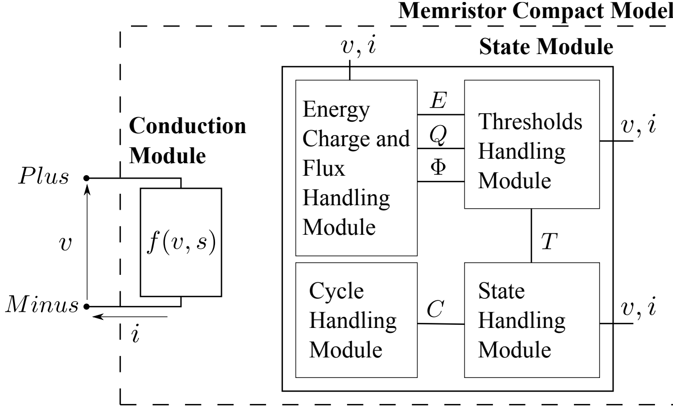


Fig. 4. Proposed Device State Handler Module.

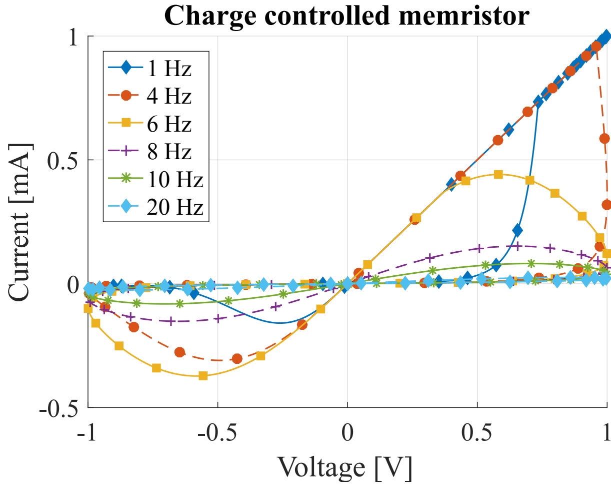


Fig. 5. Characteristic hysteresis loops of a charge controlled memristor fed with different sine voltages. The compact model was built following the scheme shown in Figure 4, using a charge handling module to control the device state.

the following equation:

$$i(v, s) = max(-cI, min(cI, f_j(v, s))). \quad (5)$$

Here, the current through the device is limited by the compliance current parameter cI.

In the same manner, the scheme shown in Figure 3 allows parasitic-overshoot effects [7], [17], [26] modeling. To that end, parasitic impedances Z_1 and Z_2 are attached in series and parallel to the global current source.

B. State Module Modeling

Several works propose models whose behavior depends on voltage or current thresholds that trigger different mechanisms unleashing a state change in the device [1], [11], [13].

In this work we propose an extension of this concept, broadening the threshold mechanisms that define the switching. Figure 4 describes the components the *State Handler Module* is composed of. Basically, the device state will depend on the previous state and the device electrical inputs.

This scheme is compatible with the simple approach of voltage/current boundary threshold, leaving the magnitudes energy, charge and flux out of the threshold management and using instant voltages and currents to trigger the switching mechanisms.

Moreover, the model is enriched, allowing energy, charge or flux to be used on the simulated device as the triggering magnitude that releases the switching events. Following the idea shown in [27]–[31], this model computes the energy, charge or flux levels at which the device experiences a state change. Using individual submodules, we calculate the energy, charge or flux applied to the device in order to define the switching, the cycle and event count, building up the whole state vector s. Following this approach Figure 5 shows the characteristic pinched hysteresis loop for a charge controlled device similar to [3].

Compared to Verilog-A implementations [7], [8], where different variables can be used, in SPICE-like subcircuit design we need to use signals to store the related information. Therefore, the energy, charge, flux or cycle/event count computations require individual signals, commonly node voltages, to define their value.

Instead of using capacitors to integrate magnitudes [4], the energy computation can be accelerated [1] using the time integral function provided by the SPICE-like simulator `idt`. On the other hand a user defined function, `switching`, performs the switching conditions verification. Taking energy as the magnitude managing the switching, `switching` would be described by equation 6.

$$s^{(1)}_{next} = switching(E, P, s^{(1)}_{current}), \quad (6)$$

There we name P as the matrix whose elements p_{jk} define the energy thresholds to switch from state j to state k. This state-controlling scheme was used for the multilevel simulation show in Figure 2. Appendix A includes the SPICE code associated with `switching` function.

Pristine State Modeling: Using the proposed conduction and switching schemes allows us to model the pristine (conductive filament preforming) state. The ability of including this additional state enriches the model capabilities. By defining the conduction mechanism and forming energy -e_p-, the pristine state can be easily included in the netlist:

$$s^{(1)}_{next} = \begin{cases} s^{(1)}_{pristine} & \text{if } E < e_p \\ switching(E, P, s^{(1)}_{current}) & \text{otherwise.} \end{cases} \quad (7)$$

Cycle and Event Count Computation: As explained in Section III, the ability to compute how many switching events a device has suffered is essential to accurately model its degradation. Using the magnitude that defines the switching -energy, charge or flux- we propose a novel scheme that allows the device cycling count to be stored. For the sake of simplicity, equations 8 and 9 will suppose devices with two states and an initial *HRS*. Let E be the computed energy, parameters p_set and p_reset the required energy levels to perform the *SET* and *RESET* respectively, and $p_cycle = p_set + p_reset$. For

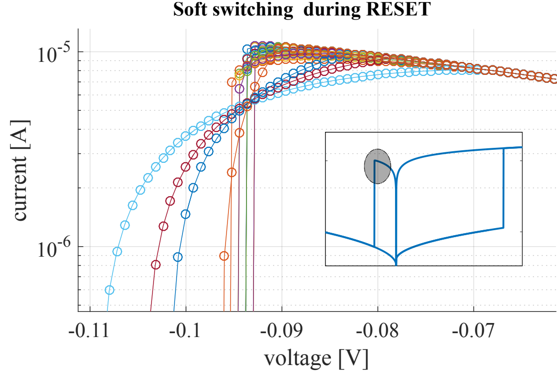


Fig. 6. Proposed soft-switching mechanism: the softening functions make use of the auxiliary variable b to soften the state switching. Different thresholds and p values produce the shown effects during reset process.

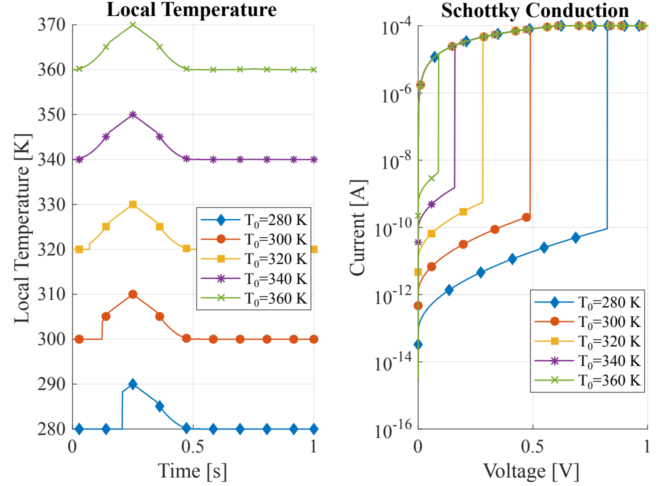


Fig. 7. Device's local temperature during the SET process and computed voltage-current relation, varying circuit temperature T_0.

unipolar devices we can compute the state vector s as

$$\begin{aligned} E &= \int_0^t v \times i \, dt \\ cycles &= \left\lfloor \frac{E}{p_cycle} \right\rfloor \\ extra_set &= \begin{cases} 1 & \text{if } (E - cycles \times p_cycle) > p_set \\ 0 & \text{otherwise} \end{cases} \\ events &= 2 \times cycles + extra_set \end{aligned} \tag{8}$$

The same methodology can be applied to bipolar devices. However, positive contributions E_+ are required to be treated independently from negative contributions E_-:

$$\begin{aligned} cycles &= \left\lfloor \frac{E_-}{p_reset} \right\rfloor \\ events &= \left\lfloor \frac{E_-}{p_reset} \right\rfloor + \left\lfloor \frac{E_+}{p_set} \right\rfloor \end{aligned} \tag{9}$$

Soft Switching Events: We can avoid hard-switching events by introducing an additional variable b that softens the transition between states. For a device experiencing a transition from state $s_j^{(1)}$ to state $s_{j+1}^{(1)}$, where i_j and i_{j+1} are their corresponding current levels, the current switching can be softened if the global current is redefined as

$$i = ... + w_j(b) \times i_j + w_j(1-b) \times i_{j+1} + ... \tag{10}$$

where $w_j(b)$ are the softening functions that control the different state's current contributions. The softening variable b can be described based on the corresponding energy thresholds

$$\begin{aligned} a1 &= \left\{ \frac{E_j}{e_{a1}} \right\} \\ a2 &= \left\{ \frac{E_j}{e_{a2}} \right\} \\ b &= \begin{cases} min(1, max(0, a1)) & \text{if } s^{(1)} = s_j \\ 1 - min(1, max(0, a2)) & \text{if } s^{(1)} = s_{j+1} \end{cases} \end{aligned} \tag{11}$$

where E_j is the total/partial energy (depending on the device type), and e_{a1} and e_{a2} the energy thresholds required to perform the transitions $s_j^{(1)} \rightarrow s_{j+1}^{(1)}$ and $s_{j+1}^{(1)} \rightarrow s_j^{(1)}$ respectively.

The softening functions $w_j(b)$ make use of the state variable b to control the partial contributions of i_j and i_{j+1}. The model designer is able to customize these functions to better adapt the switching mechanism to the physical measures. Figure 6 describes one of the possible softening schemes for bi-state devices, together with the produced effects. In these proposed functions the partial contributions depend on two thresholds, `b_th_set` and `b_th_reset`, and the parameter p, which manages the softening in the following expressions:

$$\begin{aligned} f_{set}(b) &= \begin{cases} 1 & \text{if } b \geq b_{th_set} \\ (\frac{b}{b_{th_set}})^p & \text{if } b < b_{th_set} \end{cases} \\ f_{reset}(b) &= \begin{cases} 1 & \text{if } b \leq b_{th_reset} \\ (1 - \frac{b - b_{th_reset}}{1 - b_{th_reset}})^p & \text{if } b > b_{th_reset} \end{cases} \end{aligned} \tag{12}$$

C. Extensibility and Verilog-A Implementation

The modular design of the proposed scheme allows its extension in order to consider additional phenomena. As an example, temperature dependence has proven a key factor in the device behavior [7], [17], [32]. Each of these extensions can be considered as independent behavioral sources for their later reference in dependent signals. The cited temperature influence can be directly incorporated within our model in both conduction mechanisms and energy thresholds computation by simply altering the behavioral source's nominal expressions. Figure 7 presents the results after the incorporation of local thermal behavior due to Joule-heating [7], [8].

Once the conduction mechanisms and the threshold parameters are defined, the present model can be easily ported to the Verilog-A language, with the consequent speed up of the circuit simulation. Each behavioral source is directly translated into an independent variable, following the same approach shown in [7]. Additionally, Verilog-A is more flexible regarding the use of user defined functions or variable data types (such as arrays), which eases the implementation of the methods adopted to reproduce variability effects shown in the next section.

However, even though some circuit simulators such as `Cadence Spectre` allow Verilog-A code execution, widely used SPICE simulators like `LTSPICE` do not allow Verilog-A co-simulation, accepting SPICE-like code only. Consequently, research community may benefit from the SPICE proposed compact model.

III. Variability & State Retention Modeling

Variability in memristors is one of the most concerning issues to be solved in memristive applications. Its effects are so visible that some works even use RRAMs to provide random pattern based circuit modules [33]. Three distinct kinds of variability are expected to occur in resistive switching devices [34]:

- *Inter-Device Variability.* Device to device variations in size, thickness, ion-concentrations, etc.
- *Intra-Device Variability.* Small cycle-to-cycle fluctuations caused by the stochastic nature of generation and recombination of oxygen vacancies and ion migration.
- *Read Current Fluctuations*, called *Random telegraph noise (RTN)*, is a variation in the measured current under constant bias during reading operations. It can be caused either by the electron capture and emission processes that inherently exist in oxides with high defect concentrations, or by atomic changes in the conducting filament.

Therefore, several works have studied the variability in different devices [34]–[37] and its inclusion into some Verilog-A models such as the one presented in [7].

Our proposal, fully compatible with SPICE-like simulators, allows modeling variability not only by using probability density functions but also by the direct injection of random patterns extracted from physical measurements. Figure 8 shows the scatters and histograms after measuring and normalizing the required energy to perform consecutive cycles (*SET* and *RESET* process). Therefore we can extract from those graphs the energy threshold mean and standard deviation values. By contrast, in cases where the random data does not follow a suitable function, measurements directly from the scatter are used.

The energy thresholds, the current flowing through the device or any other signal requiring variability injection can be modeled as sources whose value is composed of nominal and variable contributions. The variable contribution is described through a user defined function, $r_j()$, that can directly refer to the probability density function [35], [36]

$$i = \begin{cases} r_1(v,s) f_1(v,s) & \text{if } s^{(1)} = s_1 \\ ... & \\ r_N(v,s) f_N(v,s) & \text{if } s^{(1)} = s_N \end{cases} \quad (13)$$

The probability density function can be generated using the uniform random generator function built into the circuit simulator. If the circuit simulator does not support this feature, we can extract the random pattern by adding an additional zero amplitude voltage source affected by uniform noise.

On the other hand, by using a piecewise function we can include the physical measured data. In this case the measured variable contribution is extracted from the PWL file and injected using an additional source. An alternative to the PWL defined sources are the specific noisy source components that allow values defined via input files.

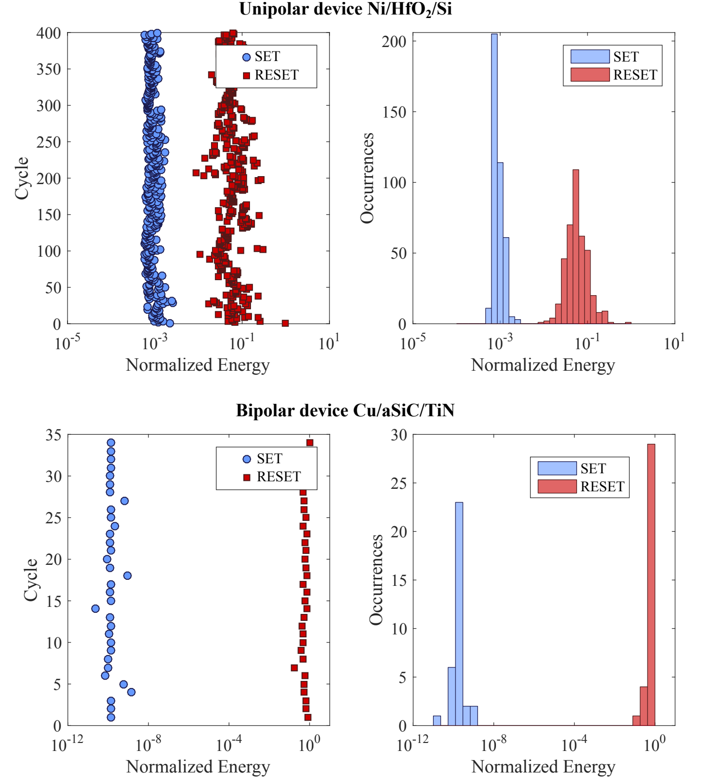
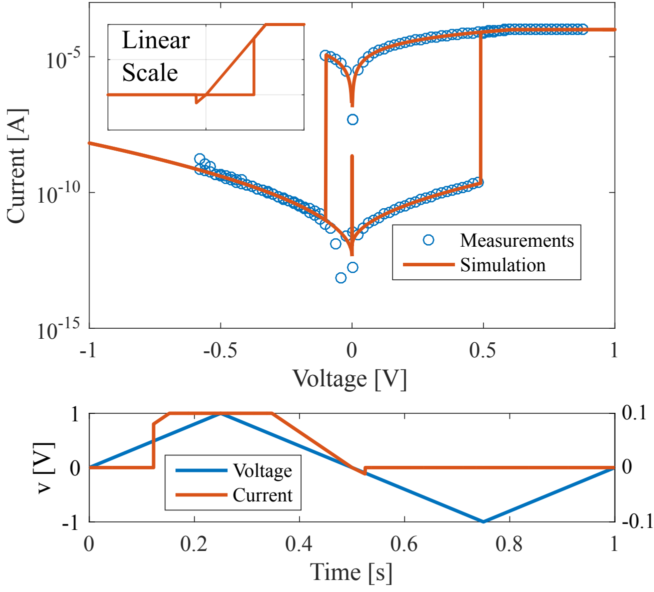


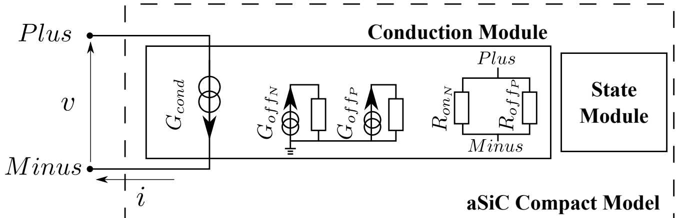
Fig. 8. *SET* and *RESET* scatter and histogram of measured energy levels required to perform switching in bipolar and unipolar devices. The values have been normalized using the maximum value of both processes.

The above scheme covers two variability types: *Inter-Device Variability* and *Read Current Fluctuations* variability. As an additional feature, the proposed modeling scheme admits *Intra-Device Variability*, defining how variability changes throughout time/cycling. This also provides the ability to define how the device gets degraded depending on its workload, and consequently, the determinability of its stored data. Therefore, by simulating consecutive switching events, the resistance state retention can be studied. Using the device state vector s we can access at each moment the number of cycles and/or events experienced by the device, and provide a more accurate variability/degradation modeling:

1) Variability dependency on time or cycle number is extracted from physical measurements [36].
2) Variability is modeled using time/cycle dependent user defined functions. Therefore, the statistical characteristics such as standard deviation (σ) and mean (μ) values become dynamic ($\sigma(t), \mu(t)$).

Finally, as reflected in equation 13, the explicit declaration of the different conduction mechanisms eases the tuning of variability and degradation functions at each resistive level. The complex, level and time dependent variability characteristics shown in the results of Section IV-C take advantage of the proposed variability modeling scheme.

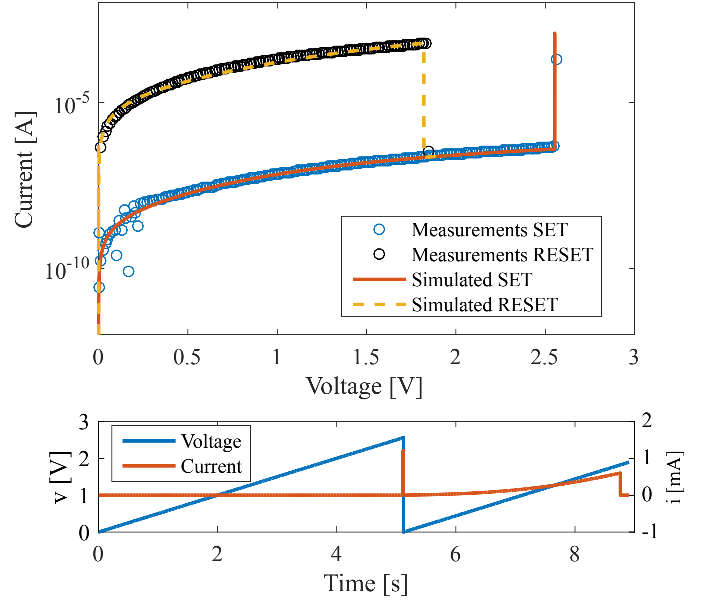


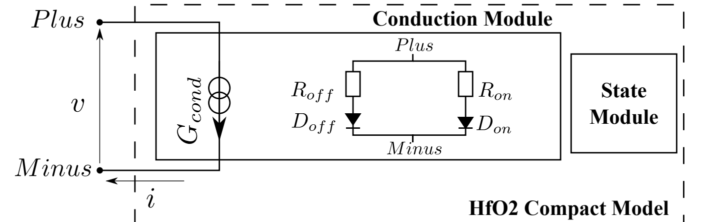


(a) Voltage-current relationship together with the voltage-current transients. On the upper graph the different slopes show how asymmetric behavior, depending on the input voltage polarity, was perfectly mimicked.

(b) Subcircuit using four different conduction submodules: *off* and *on* states for both positive and negative voltages.

Fig. 9. Bipolar device fitting: $v - i$ curves together with the used circuit.





(a) Voltage-current relationship together with the voltage-current transients. The measurement method imposes the input voltage waveform: right after the *SET* is accomplished the sawtooth wave is reset to perform the next switch.

(b) Subcircuit using two resistor-diode submodules for *off* and *on* states.

Fig. 10. Unipolar device fitting: $v - i$ curves together with the used circuit.

IV. Physical Devices Simulations

To show the model capabilities, two physical devices have been studied and fitted: a bipolar *a-SiCCu-TiN* and a unipolar *NiHfO$_2$Si* device. Figure 8 shows the measured energy levels required to perform consecutive *SET-RESET* processes in both devices. The simulations shown in this section have been performed using *Cadence Spectre* circuit simulator, replicating the measurement experiments applied to the physical devices. The full source code of those models, together with their `SPICE` and `Spectre` implementations can be found in [25]. The parameter set fitting was automatically accomplished using *MAF* simulator [1].

A. Bipolar Device

The first fitted device shows a reverse Schottky emission as its basic *HRS* conduction process, even though it displays a leakage phenomena. The model is able to fit a minimum asymmetric behavior regarding its polarity. The *LRS* is modeled using two different resistors depending on the voltage polarity. Figure 9 presents the simulated subcircuit and the achieved fitting compared against the measured data. The simulated voltage follows the stimulus that fed the device during its characterization.

B. Unipolar Device

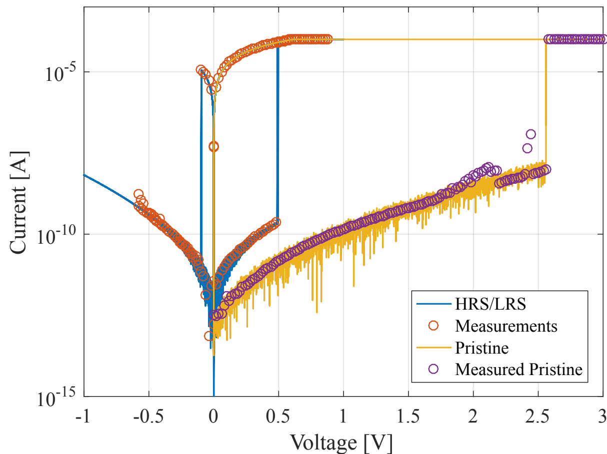
The state handling approach described by system (8) perfectly fits the behavior of unipolar devices as shown in Figure 10a. The conductivity modeling follows the guidelines from [9]: two pairs of in series resistance-diodes match both *LRS* and *HRS* (Figure 10b). In this case the simulation input voltage reproduces the sawtooth stimulus feeding the memristor during the measurements.

C. Variability

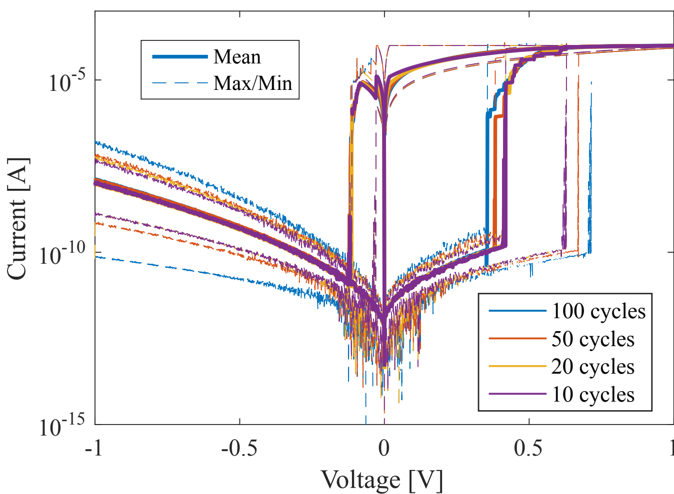
The present section provides a simple example on how variability can be included within a specific device modeling. Two representative kinds of variability are considered: random telegraph noise and intra-device variability.

Using the random values r_{noise} obtained from the normal distribution given by a characterized noisy voltage source, we shape the introduced RTN to affect in a higher grade the lower currents [34]:

$$i = \begin{cases} i_p(v)(1 + k_0(v_0 - v)^{p_0} r_{noise}) & \text{if } s^{(1)} = s_p \\ i_{on}(v)(1 + k_1(v_1 - v)^{p_1} r_{noise}) & \text{if } s^{(1)} = s_{on} \\ i_{off}(v)(1 + k_2(v_2 - v)^{p_2} r_{noise}) & \text{if } s^{(1)} = s_{off} \end{cases} \tag{14}$$



(a) Bipolar device suffering random telegraph noise over 50 cycles. The included pristine state is also affected by this variability phenomena.



(b) Bipolar device with variability on its conduction mechanisms: intra-device variability (cycle/event dependent) and random telegraph noise. Mean and max/min values are shown for 10 to 100 consecutive cycle experiments.

Fig. 11. Different examples of variability/degradation modeling.

Here the fitting parameters k_j (with $k_1 < k_2$), v_j and p_j allow the generation of the variability effects shown in Figure 11a, for each pristine, *LRS* and *HRS* states.

The second modeled variability effect regards the conduction parameters on both the *LRS* and the *HRS*. In this case the parameters, cycle/time dependent in order to describe the device degradation, are extracted from PWL functions containing the normal distributed values and then the RTN is added. Figure 11b presents the fingerprint of ten to one hundred consecutive cycles with these variability characteristics. The mean current-voltage relationship is represented together with the maximum and minimum values achieved during the experiment. It can be seen how the device current response varies with the cycling, widening the curves data and illustrating the device degradation.

V. Conclusions

We provided a customizable, physical memristor SPICE compact model, being able to accurately fit both unipolar and bipolar devices without requiring a Verilog-A compatible simulator. The conduction modeling allows multi-level description, each level being able to be characterized using diverse contributions. The component state modeling is based on the process that trigger resistive switching (device electrical thresholds, energy, charge or flux), while omitting complex geometry/internal process computations.

This design simplifies the arduous work of translating physical device characteristics to the circuit compact model, and therefore helps device manufacturers to simulate state of the art devices. Not only is the model able to handle variability but it also describes how variability/parameter degradation evolves with time, making durability simulations straightforward. Its modular scheme allows phenomena such as temperature effects to be considered, improving memristor SPICE simulations and making the analysis more reliable. Finally, the model has been validated against two different physical devices.

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Appendix
Multilevel Device LTSPICE Code

To illustrate the proposed model structure, we present the `LTSPICE` source code related to the memristor characterized in Figure 2. Additional resources such as the full source code of charge controlled memristor, unipolar and bipolar devices, temperature dependency and variability aware experiments can be downloaded from http://vlsi.die.upm.es/memristor_spice_model. Compatible simulators: `Linear Technologies LTSPICE` and `Cadence Spectre`.

```
1  ****************************************************
   ** http://vlsi.die.upm.es/memristor_spice_model
3  ** 2b-multilevel v1.0, 21/01/2016
   ** switching defined by energy thresholds
5  ** Three Schottky and one ohmic levels
   ****************************************************
7  .SUBCKT memristor Plus Minus PARAMS:
   +pi=3.1415926 Kb=1.38e-23 q=1.6e-19 eps0=8.85e-12
9  +area=6.4e-9 d=4e-8 scl1=5  scl2=7 scl3=9 AA1=1e6
       AA2=2e6 AA3 =5e7 Ub=0.9
   +epsr=8
11 +Ron=300 T0=300 ktemp=1 cI=1e-4 ronp=6.1k ronn=8.5k
       epsi=epsr*eps0
   ** energy threshold multilevel parameters
13 +p_th_1_2=0.5e-13 p_th_2_3=p_th_1_2+1e-8 p_th_3_4=
       p_th_2_3+0.5e-5
   +p_th_4_3=-1e-7 p_th_3_2=p_th_4_3-1e-8 p_th_2_1=
       p_th_3_2-1e-9
15 ** internal voltages
   +v_s1=0e-7 v_s2=1e-7 v_s3=2e-7 v_s4=3e-7
```

```
**************************************************
** Energy computation
**************************************************
* total energy
Etpospower tpp 0 value={idt( IF( V(Plus, Minus)>0 &
    v(pp)<p_th_3_4, I(Gcond)*V(Plus,Minus), 0) ,0 )}
Etnegpower tnp 0 value={idt( IF( V(Plus, Minus)<0 &
    v(np)>p_th_2_1, abs(I(Gcond))*V(Plus,Minus), 0)
    ,0 )}
* relative energy
Epospower pp 0 value={idt( IF( V(Plus, Minus)>0, I(
    Gcond)*V(Plus,Minus), 0) ,0, v(trig_p)>0)}
Enegpower np 0 value={idt( IF( V(Plus, Minus)<0, abs
    (I(Gcond))*V(Plus,Minus), 0),0, v(trig_n)>0)}
E_trigger_p trig_p 0 value={IF( v(s)==v_s1 & v(pp)>=
    p_th_3_4, 1e-7, 0)}
E_trigger_n trig_n 0 value={IF( v(s)==v_s4 & v(np)<=
    p_th_2_1, 1e-7, 0)}

**************************************************
** state computation
**************************************************
Estate s 0 value={ switching(V(Plus, Minus), V(pp),
    V(np), p_th_1_2, p_th_2_3,  p_th_3_4, p_th_4_3,
    p_th_3_2, p_th_2_1, v_s1, v_s2, v_s3, v_s4) }
Rstate s 0 r=100k

****************************************************
** Conduction processes
****************************************************
Eon  on 0 value={V(Plus, Minus)}
Ron  on 0 r=ron
Goff1 0 off1 value={ sgn(V(Plus, Minus))*area*AA1*
    ktemp*(T0**2)*exp(-q*Ub/(Kb * T0))*exp( sqrt(abs
    (V(Plus, Minus)))*(scl1 + q / (Kb * T0) * ( sqrt
    (q / (d * 4 * pi * epsi)))) ) }
Goff2 0 off2 value={ sgn(V(Plus, Minus))*area*AA2*
    ktemp*(T0**2)*exp(-q*Ub/(Kb * T0))*exp( sqrt(abs
    (V(Plus, Minus)))*(scl2 + q / (Kb * T0) * ( sqrt
    (q / (d * 4 * pi * epsi)))) ) }
Goff3 0 off3 value={ sgn(V(Plus, Minus))*area*AA3*
    ktemp*(T0**2)*exp(-q*Ub/(Kb * T0))*exp( sqrt(abs
    (V(Plus, Minus)))*(scl3 + q / (Kb * T0) * ( sqrt
    (q / (d * 4 * pi * epsi)))) ) }
Raux1 off1 0 r=1k
Raux2 off2 0 r=1k
Raux3 off3 0 r=1k
Gcond Plus Minus value={ max( -cI, min(cI, IF(V(s)==
    v_s1, i(Goff1), IF(V(s)==v_s2, i(Goff2), IF(V(s)
    ==v_s3, i(Goff3), i(Ron) ) ) ) )) }

****************************************************
**  event counters
****************************************************
E_p_events p_events 0 value={floor( V(tpp)/p_th_3_4
    )}
E_n_events n_events 0 value={floor( V(tnp)/p_th_2_1
    )}

*********************************************
** switching function
*********************************************
.func switching(v,pp,pn,th_1_2,th_2_3,th_3_4,th_4_3,
    th_3_2,th_2_1,v_s1,v_s2,v_s3, v_s4) {
+       IF(v>=0,
+               IF(pp>=th_3_4, v_s4,
+               IF(pp>=th_2_3, v_s3,
+               IF(pp>=th_1_2, v_s2,
+               v_s1) ) ),
+               IF(pn>=th_4_3, v_s4,
+               IF(pn>=th_3_2, v_s3,
+               IF(pn>=th_2_1, v_s2,
+               v_s1)) ) )      }
.ENDS memristor
```

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