# SPICE-Compatible Compact Model for Graphene Field-Effect Transistors

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***Abstract*—This paper presents a compact device model for graphene field-effect transistors. This model extends prior iterative models (due to Meric *et al.* and Thiele *et al.*) in two ways. First, the model is given as a closed-form expression that is more computationally efficient. Second, it is valid for devices based upon either monolayer graphene or bilayer graphene. Simulations demonstrate that this model agrees closely with experimental data. Furthermore, the efficiency of this model enables the design and analysis of logic circuits composed of multiple graphene devices. Example simulation results are provided that demonstrate the potential for graphene-based circuit speeds five times that of circuits based upon 32-nm silicon technology.**

## I. Introduction

It is likely that the continued miniaturization of silicon transistors soon will become ineffective as a means to enable improvements in speed and power consumption. This has motivated the search for novel materials with electronic properties that will allow for continued performance scaling. Graphene, an atomically thin carbon film, has been identified as a strong candidate due to its ultra-high mobility (up to 200,000 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [1]). Also, its planar structure allows for the use of lithographic circuit manufacturing techniques.

However, a major drawback of graphene is its lack of an intrinsic bandgap. This greatly limits the "off"-state resistance of graphene transistors, and thus, limits their use as switches in digital logic applications. For this reason, a number of designs have been proposed for graphene-based transistors that include mechanisms for inducing a bandgap [2]–[5].

Due to the complexity of these mechanisms, the device models proposed thus far [6], [7] require substantial iterative computation in order to achieve quantitative accuracy. These models are not efficient enough to permit the simulation of large-scale circuits based upon graphene transistors. To surmount that obstacle, this paper presents a compact, computationally efficient model for graphene field-effect transistors.

The equations for this model are provided below in Section II. Then, Section III presents simulation results comparing the predictions of the new model with experimental data obtained by Xia *et al.* [2]. The close agreement of these predictions with experimental results prompts the use of this model to project the performance of digital circuit designs based upon graphene transistors. Section III discusses these projections. Finally, Section IV provides a summary and conclusions.

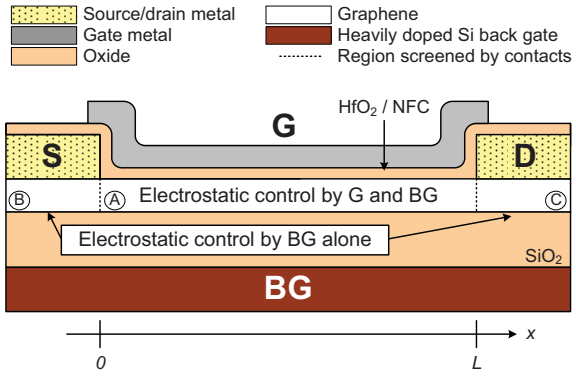


Fig. 1. Cross-sectional schematic view of a front- and back-gated bilayer graphene transistor designed and demonstrated by Xia *et al.* [2]. In this device, a graphene bilayer is contacted by source (S) and drain (D) electrodes and gated by a front gate/top gate (G) and a back gate (BG).

## II. Model Equations

### A. Background: Iterative Charge-Sheet Model

Fig. 1 provides a cross-sectional view of a graphene-based transistor [2], as modeled in this work. In such a transistor, a rectangular strip consisting of either monolayer or bilayer graphene is contacted by source and drain electrodes. A gate electrode is placed in close proximity to the graphene strip and isolated by a high-k dielectric stack. The entire device rests on a silicon substrate with a thick isolation oxide. The substrate is used as a back gate for the device, the purpose of which is to induce a bandgap.

A prior model for this device is an iterative charge-sheet model developed by Meric *et al.* [6] and by Thiele *et al.* [7]. In this model, the drain current $I_D$ for a device of width $W$ and length $L$ is given by

$$I_D = \frac{W}{L}\int_0^L e\cdot n\cdot\left(\frac{\mu E}{1+\frac{\mu E}{v_{sat}}}\right)dx. \qquad (1)$$

Here, $n$, the carrier density, and $E$, the lateral electric field, are functions of the position $x$ along the channel, while $\mu$ is the carrier mobility and $v_{sat}$ is the saturation velocity. The carrier density $n(x)$ is given by

$$n(x) = \sqrt{n_0^2 + (C_{TOP}(V_{GS} - V(x) - V_0)/e)^2}, \qquad (2)$$

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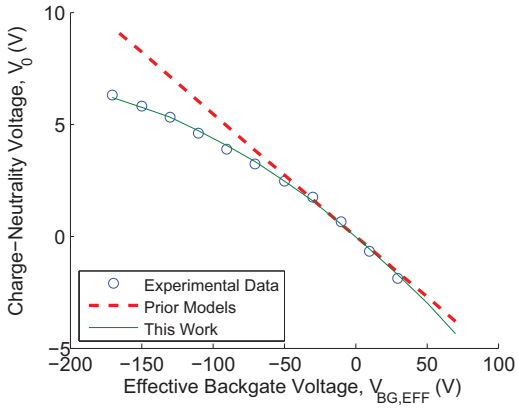


Fig. 2. Evaluation of bilayer device behavior at the charge neutrality point. Models for monolayer devices posit a linear relationship between the charge-neutrality voltage and the back-gate voltage. In contrast, experimental data on bilayer devices from Xia *et al.* [2] demonstrate nonlinear behavior. To extend prior models to bilayer devices, the model presented here adds a second-order term to the linear relationship.

where $n_0$ is the intrinsic carrier density due to impurities and defects, $C_{TOP}$ is the top-gate sheet capacitance, $V_{GS}$ is the gate-to-source voltage, $V(x)$ is the voltage at $x$, and $V_0$ is the charge-neutrality voltage (i.e., the top-gate voltage that minimizes the net charge in the channel at a given back-gate voltage).

The quantity $V_0$ is calculated by

$$V_0 = \frac{C_{BACK}}{C_{TOP}} V_{BG,EFF}, \tag{3}$$

where $C_{BACK}$ is the sheet capacitance of the back gate, $V_{BG,EFF} = V_{BG} - V_{BG,0}$ is the effective back-gate voltage, and $V_{BG,0}$ is the back-gate voltage that minimizes charge in the channel when the top-gate voltage is zero.

The saturation velocity [6] is given by

$$v_{sat} = \frac{\Omega}{(\pi n)^{0.5-\varepsilon}}, \tag{4}$$

where $\Omega$ is the phonon energy, $n$ is the carrier density, and $\varepsilon$ is an empirical corrective factor.

Together, Eqs. 1-4 form a model that allows for the determination of the current-voltage behavior of a monolayer graphene dual-gate transistor. However, there are two substantial drawbacks to this model. First, it is seen that $I_D$ is not closed-form since Eqs. 1 and 2 are mutually dependent. Instead, these equations must be solved self-consistently. Second, the model assumes monolayer graphene and must be extended in order to apply to bilayer graphene. These issues are resolved with the model presented here.

### *B. Closed-Form Model*

In this work, four modifications are made to the model described above in order to make it closed-form and accurate for both monolayer and bilayer graphene. First, to make the model closed-form, the approximation is made that the electric field is uniform along the channel. This approximation is reasonable so long as the current-voltage behavior is dictated by the electrostatics at the contacts. This is borne out below in Section III via a comparison to experimental data.

Under this approximation, the mobility and electric field may be moved outside the integral in Eq. 1. What remains may be transformed into an averaging of the carrier density over the channel voltage $V$:

$$\bar{n} = \frac{1}{V_{DS,CH}} \int_{V(x=0)}^{V(x=L)} \sqrt{n_0^2 + (C_{TOP}(V_{GS} - V - V_0)/e)^2}\, dV. \tag{5}$$

In Eq. 5, $V_{DS,CH} = V(x=L) - V(x=0)$ is the voltage drop across the channel (i.e., excluding the voltage drop at the contacts). This integral evaluates to a closed-form, albeit lengthy, expression.

The second modification adjusts the calculation of $V_0$ in the case of bilayer graphene devices. For these devices, a corrective term modulated by a fitting parameter $\gamma$ must be introduced in Eq. 3 due to nonlinearity in the response of the charge-neutrality voltage to the back-gate voltage. The modified equation is as follows:

$$V_0 = \frac{C_{BACK}}{C_{TOP}} V_{BG,EFF} - \gamma V_{BG,EFF}^2 \tag{6}$$

To illustrate the need for this adjustment, Fig. 2 plots the values obtained using the original Eq. 3 and the adjusted Eq. 6. These values of $V_0$ are compared in the figure to those from experiments on bilayer devices by Xia *et al.* [2]. The best fit of Eq. 6 to the experimental data is obtained with $\gamma = 1.1 \times 10^{-4}\ \mathrm{V}^{-1}$.

The third modification accounts for mobility variations observed in bilayer graphene [8]. Specifically, in bilayer graphene, mobility increases strongly with carrier density. In contrast, monolayer graphene exhibits only a slight decrease in mobility as a function of carrier density. Fig. 3 shows the mobility of the device of Xia *et al.* [2] as obtained by fitting to a charge-sheet model. On the basis of this fit, the mobility $\mu$ is replaced by the following expression:

$$\mu(\bar{n}, V_{BG,EFF}) = \Delta_\mu(V_{BG,EFF}) \cdot \bar{n}, \tag{7}$$

where the mobility slope $\Delta_\mu(V_{BG,EFF})$ is obtained empirically, i.e., from Fig. 3. For large values of the effective back-gate voltage, this may be simplified further by using the average value $\Delta_\mu$ obtained from the average behavior represented by the dashed line in the figure.

The three modifications given thus far are sufficient to obtain a closed-form expression for the drain current in both monolayer and bilayer graphene devices. Specifically, by substitution of Eqs. 5, 6, and 7 into Eq. 1, one obtains:

$$I_D = \frac{W}{L} e \bar{n}^2 \Delta_\mu \left( \frac{V_{DS,CH}}{1 + \frac{\Delta_\mu \bar{n} V_{DS,CH}}{L v_{sat}}} \right). \tag{8}$$

The model is completed with a fourth modification that accounts for behavior at the contacts in bilayer graphene devices. For these devices, the induced bandgap results in a Schottky barrier being formed at the contacts. The barrier height is proportional to the effective back-gate voltage, $V_{BG,EFF}$. Furthermore, it is modulated by the top gate, with the maximum occurring when the top gate is at the charge

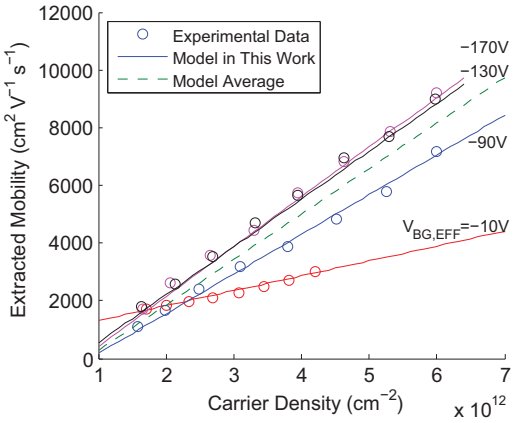


Fig. 3. By fitting data from Xia *et al.* [2] to a charge-sheet model [6], a linear relationship is observed between carrier mobility and carrier density.

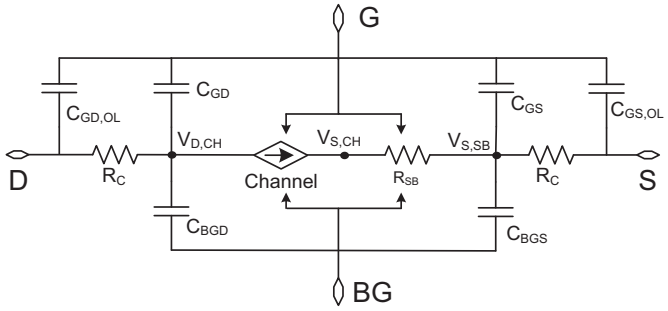


Fig. 4. Equivalent circuit model for the device shown in Fig. 1. Transport in the channel is given by Eq. 8. Schottky-barrier resistance is given by Eq. 9. Parasitic resistances and capacitances also may be supplied via estimates from the device geometry or from experimental data.

neutrality voltage $V_0$. Thus, the Schottky barrier effective resistance is observed to be modeled by

$$R_{SB} = A\, e^{\Delta_\phi \cdot V_{BG,EFF}}\, e^{-(V_{GS}-V_0)^2/4V_W^2}. \qquad (9)$$

Here, $A$, $\Delta_\phi$, and $V_W$ are empirical fitting parameters.

The complete model, consisting of Eqs. 8 and 9, may be represented schematically via the equivalent circuit shown in Fig. 4. Parasitic components (e.g., contact resistances and capacitances) are included in the schematic for use in circuit-level simulation software, such as Cadence tools [9].

## III. Simulation Results

Fig. 5 compares the current-voltage behavior observed in the experimental device of Xia *et al.* [2] with the predictions of the model presented above in Section II. To generate these predictions, the model was implemented using the parameters given in Tbl. I. This implementation was coded in the Verilog-A language and simulated using the Cadence Spectre simulator [9]. As such, it is compatible with other common circuit simulators, including SPICE.

As is seen in Fig. 5, the predictions of the compact model presented here agree closely with experimental data. Thus, the model provides the opportunity for simulation and analysis of circuit designs that incorporate multiple graphene transistors.

TABLE I
Model Parameters for Example Bilayer Graphene Device

| | | |
|---|---|---|
| **Physical Parameters** | | |
| $W, L$ | Channel width and length ($\mu$m) | 1.6, 3.0 |
| $n_0$ | Intrinsic carrier density (cm$^{-2}$) | $0.9 \times 10^{-12}$ |
| $C_{TOP}$ | Top-gate sheet capacitance (nF cm$^{-2}$) | 209 |
| $C_{BACK}$ | Back-gate sheet capacitance (nF cm$^{-2}$) | 11.5 |
| $\Omega$ | Scattering optical phonon energy (meV) | 50 |
| $V_{BG,0}$ | Charge-neutral back-gate voltage (V) | 50 |
| **Empirical Parameters** | | |
| $\varepsilon$ | Phonon scattering correction | $1.7 \times 10^{-2}$ |
| $\gamma$ | Charge-neutrality voltage correction (V$^{-1}$) | $1.1 \times 10^{-4}$ |
| $\Delta_\mu$ | Mobility slope (cm$^4$ V$^{-1}$ s$^{-1}$) | $1.58 \times 10^{-9}$ |
| $A$ | Schottky barrier fitting parameters | 1.8 KΩ |
| $\Delta_\phi$ | | -0.024 V$^{-1}$ |
| $V_W$ | | 0.3 V |

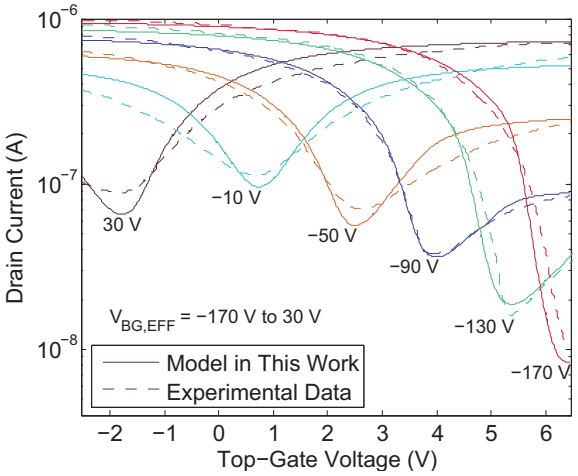


Fig. 5. Comparison of the predictions of the model presented here with the experimentally-obtained current-voltage behavior of the bilayer graphene device of Xia *et al.* [2].

In order to implement such circuits, it is desirable to have multiple device types that are complementary, i.e., that act akin to n-type and p-type silicon transistors.

Fig. 5 shows that the desired complementary devices might be obtained by using distinct back-gate voltages, e.g., 30 V for "n-type" transistors and -130 V for "p-type" transistors. However, Fig. 5 also demonstrates that the charge neutrality voltage, and therefore the threshold voltage, is dependent on the back-gate voltage. In particular, the threshold for the "n-type" device is negative, while it is positive for the "p-type" device. In both cases, this is the opposite of what is desired.

Thus, an additional mechanism is required that controls the charge neutrality voltage without disturbing the bandgap induced electrostatically by the back gate. For example, Castro *et al.* [5] predicted and Brenner and Murali [10] demonstrated experimentally that it is possible to shift the charge neutrality voltage using chemical doping. This mechanism is incorporated into the model by adding a voltage shift parameter to $V_0$. With this parameter, current-voltage curves may be

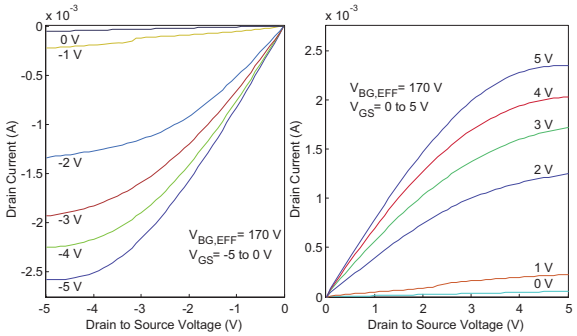


Fig. 6. Modeled drain current for a prospective "p-type" device (left) and "n-type" device (right) using back-gate voltage to establish a bandgap and channel doping to shift the charge-neutrality voltage.

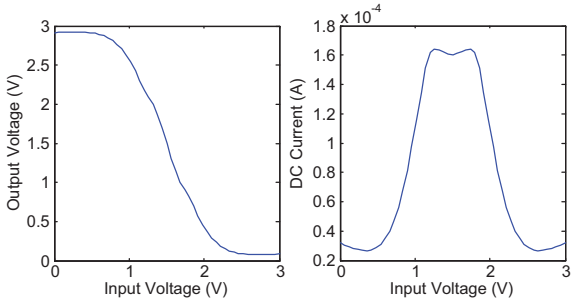


Fig. 7. Voltage and current transfer characteristics of an inverter designed using the complementary transistors whose models are given in Fig. 6.

obtained for prospective complementary "doped" graphene-based devices. These curves are shown in Fig. 6.

Using these transistor models, an inverter readily is designed. Simulated voltage and current transfer curves for this inverter are shown in Fig. 7. This figure demonstrates that sufficient gain is achieved, but also that substantial static current is drawn by the inverter (in excess of 30 $\mu$A). This is approximately three orders of magnitude higher than in state-of-the-art high-performance CMOS. The high static current is a result of the high "off"-state current of the graphene transistors. This demonstrates that even more sophisticated methods will be required to engineer the bandgap of bulk graphene transistors for low-power or low-energy applications. Such methods also might be of use in avoiding any issues that might arise with the use of large back-gate voltages in extended, densely integrated circuits.

Nonetheless, one of the most promising aspects of graphene is its potential for ultra-high speed. This is borne out by simulations of a five-stage ring oscillator. This circuit produces the simulated output shown in Fig. 8. As is seen in this figure, this oscillator generates a 125 GHz signal, which is five times as fast as is obtained using a 32-nm silicon process [11].

## IV. Summary and Conclusions

In summary, this paper presents a model for graphene-based field-effect transistors. This model is computationally efficient and closed-form. Furthermore, it enables simulation of devices based upon either monolayer or bilayer graphene. Comparisons with experimental data demonstrate the model

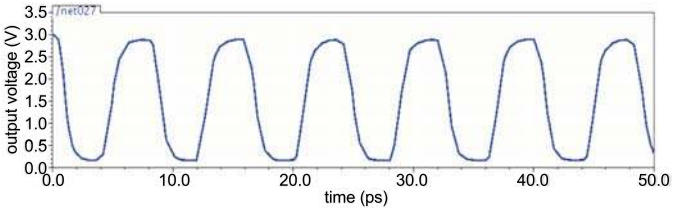


Fig. 8. Transient switching behavior of a five-stage ring oscillator based upon the inverter whose characteristics are given in Fig. 7.

to be in close agreement. Thus, the model described here enables the rapid simulation and exploration of graphene-based circuits.

Results presented in this paper validate the prevalent expectations for the use of graphene devices in digital applications. Specifically, circuits based upon these devices are likely to be much faster than equivalent silicon-based circuits, albeit much less energy efficient. Simulations of an inverter and a ring oscillator predict speeds as much as five times as fast, but with a power consumption as much as three orders of magnitude higher. Nevertheless, should applications have the need to take advantage of graphene for its speed, the model presented here would enable their robust design.

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