SPICE-Compatible Thermal Simulation with Lumped Circuit Modeling for Thermal Reliability Analysis based on Modeling Order Reduction

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Abstract

With the growing power dissipation in modern high performance VLSI designs, nonuniform temperature distribution and limited heat-conduction capability have caused thermal induced performance and reliability degradation. However, the problem modeled by finite difference method for interconnect reliability analysis has huge size if we require the resolution with wire width. In addition, the generated lumped circuit has significant number of input sources, and the bottleneck of traditional model reduction methods is the big number of input ports. In this paper, we propose a method of SPICE-compatible thermal simulation for interconnect reliability analysis. The lumped thermal circuit modeling with adaptive approach is used to reduce the problem size. The improved extended Krylov subspace (IEKS) method, independent of the number of input ports, is used for thermal simulation. The experimental results show that our method provides highly accurate results with performance improvement $15\times$ *over T-Spice for the problem with node number* 72428.

1 Introduction

The ever-increasing demands for more functionality and higher speed have pushed the very large scale integration (VLSI) industry towards more aggressive scaling [1]. This trend has lead to the rapid increase of power consumption and heat generation. As a result, nonuniform temperature distribution on chip has become more and more serious [2] [3] [4]. Without thermal management, thermal problems not only lead to timing failure but also degrade chip reliability.

Electromigration (EM) is the main reliability concern and will become a more limiting factor of IC designs. The power generated by self-heating effect in interconnects only contributes a small part of the chip power consumption. However, the impacts of thermal effects on the reliability of interconnects are serious. Therefore, EM must be addressed together with a thermal reliability modeling and is recognized in the International Technology Roadmap for Semiconductors (ITRS) 2002 update as one of the difficult challenges [1]. In order to diagnose the thermal reliability and improve the design quality, an efficient chip-level three-dimensional (3-D) thermal simulator is crucial to success for the VLSI designs.

There are some challenges for the thermal modeling and simulation. First, the uniform heat distribution in a chip does not guarantee the uniform temperature profile due to the complex 3-D nature of heat spreading and the complicated boundary conditions. Simulation runtime and memory usage are another issues due to the large size of integrated circuit systems. Several approaches have been proposed. A full-chip thermal simulation was presented in [5] solving function-block size problem. The finite difference method (FDM) with equivalent RC model has been presented [6] [7]. However, due to the large size of matrix, the direct matrix-solving algorithms have runtime and memory usage problems for large scale systems. A thermal simulation method based on model reduction was presented to improve the runtime [8]. However, the bottleneck in such method is that the number of input sources can cause big Krylov subspace. This is especially difficult for equivalent thermal circuit which has a large number of equivalent independent current sources. An efficient full-chip thermal simulator based on alternating direction (ADI) method was presented [9] [10]. However, for interconnect related applications such as thermal reliability analysis, the generated problem is huge due to the discretization size of interconnects.

In this paper, we present a SPICE-compatible method of thermal simulation with lumped thermal circuit modeling for interconnect reliability analysis based on the technique of IEKS. First, lumped thermal circuit with adaptive approach is used to model the problem. The complicated packaging, heat sinks, and cooling system are modeled as equivalent thermal resistors. Substrate is discretized according to the temperature gradient and modeled with equivalent thermal elements. Interconnects are also modeled as lumped elements. With this modeling method, the problem size can be reduced and the wire temperature can be obtained. Second, the problem is solved by the IEKS method. Unlike the tradition model reduction method whose runtime is heavily dependent on the number of input ports, the runtime of the proposed method is independent of that. In addition, there is no moment shifting for IEKS method.

The remainder of the paper is organized as follows. The modeling method and problem formulation is presented in Section 2. The multiport model reduction method, IEKS, is presented in

Section 3. The implementation and experimental results are discussed in Section 4, followed by the conclusion in Section 5.

2 Modeling Method and Problem Formulation

The modeling method and problem formulation will be discussed in this section. Noon-homogeneous case and boundary conditions are also presented.

2.1 Chip Modeling

For a chip with packaging, heat sinks, and cooling systems, the system can be modeled with two parts. First, the temperature distribution in a chip including substrate and interconnects is governed by the heat conduction equation [11]

$$\rho C_p \frac{\partial T(\vec{r},t)}{\partial t} = \bigtriangledown \cdot [\kappa(\vec{r},T) \bigtriangledown T(\vec{r},t)] + g(\vec{r},t), \quad (1)$$

where T is the time dependent temperature, ρ is the density of the material, C_p is the specific heat, κ is the thermal conductivity, and g is the heat energy generation rate. The physical meaning of (1) can be described from the law of energy conservation. For a control volume, the rate of energy stored causing the temperature increase is $\frac{dE}{dt} = \int \rho C_p \frac{\partial T}{\partial t} dV$, the rate of heat conduction through surface $d\vec{A}$ is $(\kappa \bigtriangledown T \cdot d\vec{A})$ and all surface of the control volume is $Q = \int \kappa \bigtriangledown T \cdot d\vec{A} = \int \bigtriangledown \cdot [\kappa \bigtriangledown T]\, dV$, and the power generated is $Q_p = \int g dV$.

Second, packaging, heat sinks, and cooling systems are modeled as 1-D equivalent thermal resistance network. Suppose that the package surfaces are held isothermal. If the package surfaces are not isothermal, 3-D model is needed for better accuracy to include the contribution due to heat spreading within the package [12]. The effective heat transfer coefficient in the direction of heat flow, $\vec{i}$, is modeled as $h_i^e = 1/A^i R_\theta^i$, where A^i is the effective area normal to $\vec{i}$ and R_θ^i are the equivalent thermal resistance. The equivalent convection boundary conditions are

$$\kappa(\vec{r},T) \frac{\partial T(\vec{r},t)}{\partial n_i} = h_i^e (T_a - T(\vec{r},t)), \quad (2)$$

where T_a is the ambient temperature and $\partial / \partial n_i$ is the differentiation along the outward direction normal to the boundary surface.

2.2 Substrate Modeling

The term $\bigtriangledown \cdot [\kappa(\vec{r},T) \bigtriangledown T(\vec{r},t)]$ in (1) can be replaced by $\kappa(T) \bigtriangledown^2 T(\vec{r},t)$ for homogeneous materials, and then a second-order parabolic partial differential equation can be obtained

$$\rho C_p \frac{\partial T(\vec{r},t)}{\partial t} = \kappa [\frac{\partial^2 T(\vec{r},t)}{\partial x^2} + \frac{\partial^2 T(\vec{r},t)}{\partial y^2} + \frac{\partial^2 T(\vec{r},t)}{\partial z^2}] + g(\vec{r},t). \quad (3)$$

Suppose that the substrate is discretized with size Δx, Δy, and Δz in x, y, and z directions, respectively. Then the temperature $T(x,y,z,t)$ at node (i,j,k) can be can be replaced by $T(i\Delta x, j\Delta y, k\Delta z, t)$, which is denoted as $T_{i,j,k}$ for the rest of the paper. To have second order accuracy in space $O[(\Delta x)^2, (\Delta y)^2, (\Delta z)^2]$, we use the central-difference discretization on (3). After rearranging, the difference equation at node (i,j,k) can be expressed as

$$\rho C_p \Delta V \frac{dT_{i,j,k}}{dt} =$$

$$-\kappa \frac{A_x}{\Delta x}(T_{i,j,k} - T_{i-1,j,k}) - \kappa \frac{A_x}{\Delta x}(T_{i,j,k} - T_{i+1,j,k})$$
$$-\kappa \frac{A_y}{\Delta y}(T_{i,j,k} - T_{i,j-1,k}) - \kappa \frac{A_y}{\Delta y}(T_{i,j,k} - T_{i,j+1,k})$$
$$-\kappa \frac{A_z}{\Delta z}(T_{i,j,k} - T_{i,j,k-1}) - \kappa \frac{A_z}{\Delta z}(T_{i,j,k} - T_{i,j,k+1}) + \Delta V g_{i,j,k}. \quad (4)$$

where $\Delta V = \Delta x \Delta y \Delta z$ is the control volume of node (i,j,k), $A_x = \Delta y \Delta z$, $A_y = \Delta x \Delta z$, and $A_z = \Delta x \Delta y$. The physical meaning of (4) is clear from the law of energy conservation

$$\frac{dE}{dt} + Q_1 + Q_2 + Q_3 + Q_4 + Q_5 + Q_6 = Q_p, \quad (5)$$

where $\frac{dE}{dt} = \rho C_p \Delta V \frac{dT_{i,j,k}}{dt}$, $Q_1 = \kappa \frac{A_x}{\Delta x}(T_{i,j,k} - T_{i-1,j,k})$, $Q_2 = \kappa \frac{A_x}{\Delta x}(T_{i,j,k} - T_{i+1,j,k})$, $Q_3 = \kappa \frac{A_y}{\Delta y}(T_{i,j,k} - T_{i,j-1,k})$, $Q_4 = \kappa \frac{A_y}{\Delta y}(T_{i,j,k} - T_{i,j+1,k})$, $Q_5 = \kappa \frac{A_z}{\Delta z}(T_{i,j,k} - T_{i,j,k-1})$, $Q_6 = \kappa \frac{A_z}{\Delta z}(T_{i,j,k} - T_{i,j,k+1})$, and $Q_p = \Delta V g_{i,j,k}$. Then (4) can be translated into the equivalent lumped thermal circuit as shown in Figure 1:

$$C^\theta \frac{dT_{i,j,k}}{dt} + \frac{T_{i-1,j,k} - T_{i,j,k}}{R^\theta_{i-1,j,k}} + \frac{T_{i+1,j,k} - T_{i,j,k}}{R^\theta_{i+1,j,k}} + \frac{T_{i,j-1,k} - T_{i,j,k}}{R^\theta_{i,j-1,k}}$$
$$+ \frac{T_{i,j+1,k} - T_{i,j,k}}{R^\theta_{i,j+1,k}} + \frac{T_{i,j,k-1} - T_{i,j,k}}{R^\theta_{i,j,k-1}} + \frac{T_{i,j,k+1} - T_{i,j,k}}{R^\theta_{i,j,k+1}} = Q_p, \quad (6)$$

where $C^\theta = \rho C_p \Delta V$ is the thermal capacitance, Q_p is the heat flow coming from power generated in ΔV, and $R^\theta_{i\pm1,j,k} = \Delta x/(\kappa A_x)$, $R^\theta_{i,j\pm1,k} = \Delta y/(\kappa A_y)$, and $R^\theta_{i,j,k\pm1} = \Delta z/(\kappa A_z)$ are the thermal resistances. The analogy between electrical and thermal circuits is shown in Table 1. In fact, (6) is equivalent to the KCL in electrical circuit at node (i,j,k) because heat flow is equivalent to current flow in electrical circuit. Since there are a lot of power sources, the equivalent thermal circuit has a large number of current sources.

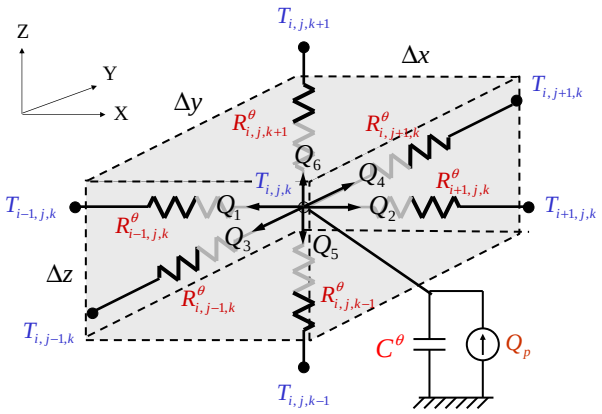

Figure 1. The modeled thermal circuit.

2.3 Non-homogeneous Case and Boundary Conditions Modelings

Consider a point (i,j,k) located among three different materials and at the boundary $k=N$ as shown in Figure 2. The rate

Electrical Circuit			Thermal Circuit		
V	$[V]$	Voltage	T	$[^oC]$	Temperature
I	$[A]$	Current Flow	Q	$[W]$	Heat Flow
σ	$[1/\Omega m]$	Electrical Conductivity	κ	$[W/^oCm]$	Thermal Conductivity
R	$[\Omega]$	Resistance	R^θ	$[^oC/W]$	Thermal Resistance
C	$[F]$	Capacitance	C^θ	$[J/^oC]$	Thermal Capacitance

Table 1. The analogy of the equivalent thermal circuit

of energy stored in a control volume causing the temperature increase is $\frac{dE}{dt} = [\frac{1}{8}\Delta V\rho_1 C_{p1} + \frac{1}{8}\Delta V\rho_2 C_{p2} + \frac{1}{4}\Delta V\rho_3 C_{p3}]\frac{dT_{i,j,N}}{dt}$. The power generated in control volume is $Q_p = \frac{1}{8}\Delta V g_1 + \frac{1}{8}\Delta V g_2$. The rate of heat conduction from $T_{i,j,N}$ to $T_{i-1,j,N}$ and $T_{i+1,j,N}$ are $Q_1 = \frac{\kappa_1+\kappa_3}{4}\frac{\Delta A_x}{\Delta x}(T_{i,j,N} - T_{i-1,j,N})$ and $Q_2 = \frac{\kappa_2+\kappa_3}{4}\frac{\Delta A_x}{\Delta x}(T_{i,j,N} - T_{i+1,j,N})$, respectively. The other terms can be calculated similarly: $Q_3 = \frac{\kappa_3}{2}\frac{\Delta A_y}{\Delta y}(T_{i,j,N} - T_{i,j-1,N})$, $Q_4 = \frac{\kappa_1+\kappa_2}{4}\frac{\Delta A_y}{\Delta y}(T_{i,j,N} - T_{i,j+1,N})$, and $Q_5 = \frac{\kappa_1+\kappa_2+2\kappa_3}{4}\frac{\Delta A_z}{\Delta z}(T_{i,j,N} - T_{i,j,N-1})$. The equivalent thermal convection from $T_{i,j,k}$ to T_a is $Q_6 = h^e_{z+}\Delta A_z(T_{i,j,N} - T_a)$, where h^e_{z+} is the effective heat transfer coefficient. From energy conservation (5) and equivalent lumped thermal circuit like (6), we can obtain the equivalent thermal circuit as shown in Figure 2.

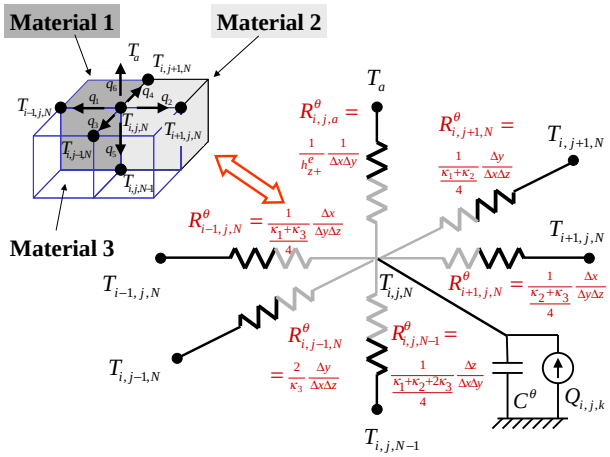

Figure 2. The example of non-homogeneous case and boundary conditions.

2.4 Interconnect Modeling

Figure 3 shows a metal wire on an insulator, in which the width, length, thickness, and thermal conductivity are w_m, l, t_m, and κ_m, respectively. The thickness and the thermal conductivity of the underlying insulator are t_{ins} and κ_{ins}. The wire resistivity is temperature dependent and can be described as follows:

$$\rho_m(T_m) = \rho_o[1 + \beta(T_m - T_o)], \quad (7)$$

where ρ_o is the wire resistivity at reference temperature T_o, and β is the temperature coefficient of resistivity. Here we suppose that, e.g., C4/CBGA package, the primary heat transfer path is through substrate and heat sinks to the ambient, and the secondary heat transfer path is through the solder balls and PCB to the ambient. The heat conduction from nearby interconnects are ignored. The detailed discussions about the accuracy compared to other models can be found in [13].

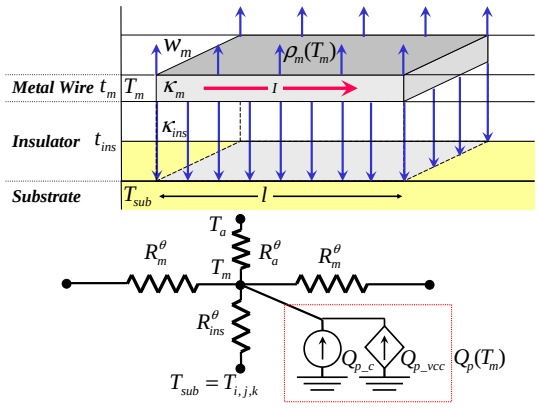

Figure 3. Interconnect lumped model.

The heat flow generated by self-heating in wire segment l can be expressed as

$$Q_p(T_m) = I^2R = I^2\rho_m(T_m)\frac{l}{t_m w_m} = Q_{p_c} + Q_{p_vcc}, \quad (8)$$

where I is the current flowing through the wire, $Q_{p\_c} = I^2\rho_o(1 - \beta T_o)l/t_m w_m$ is the constant current source, and $Q_{p\_vcc} = (I^2\rho_o\beta l/t_m w_m)T_m$ is the voltage-controlled current source due to the temperature dependent resistivity. The thermal resistor along the interconnect has resistance

$$R^\theta_m = \frac{1}{\kappa_m}\frac{l/2}{t_m w_m}. \quad (9)$$

The primary heat transfer path can be modeled by equivalent thermal resistor with resistance

$$R^\theta_{ins} = \frac{1}{\kappa_{ins}}\frac{t_{ins}}{l w_m}. \quad (10)$$

The secondary heat transfer path will be modeled similarly with resistance

$$R^\theta_a = \frac{1}{h^e_{z+}}\frac{1}{l w_m}. \quad (11)$$

Figure 3 shows the equivalent lumped thermal circuit. The other cases of interconnect modeling can be derived similarly.

2.5 Adaptive Approach

In order to keep the reasonable size of the formulated problem, we will use the adaptive approach to discretize the substrate. In the region of high temperature gradient, finer discretization size is used to reach the accuracy. On the contrary, coarser grid will be used in the region of low temperature gradient to keep the problem size small. To decide the regional discretization size of the chip, we need to know the rough temperature distribution. The temperature profile of the substrate with coarse grid discretization will be simulated first. According to the simulated results, the adaptive method is applied to satisfy the requirements of both problem size and accuracy.

After modeling the substrate and interconnects, the equivalent thermal circuit can be expressed by the time-domain Modified Nodal Analysis (MNA) equation

$$Gx + C\dot{x} = Bu, \tag{12}$$

where G and C represent the conductance and capacitance matrices, x is the vector of node voltages, u is the vector of independent current sources, B is the input adjacency matrix mapping the sources to the internal states. In the thermal circuit, there are no equivalent inductors, but there are a lot of current sources due to the significant number of heat sources. The conductance matrix G and capacitance matrix C are symmetric and positive definite.

3 Multiport Model Reduction

Model order reduction generates an analytic model which is a compact representation of original circuits by matching their moments or poles. After taking the Laplace transformation of (12), we have

$$GX + sCX = BU. \tag{13}$$

Apply the Taylor series expansion at zero frequency on both side of (13), we have

$$\begin{aligned}(G + sC)(m_0 + m_1 s + m_2 s^2 + \cdots) \\ = B(u_0 + u_1 s + u_2 s^2 + \cdots),\end{aligned} \tag{14}$$

where m_i and u_i, the coefficients of the i_{th} term in the Taylor series, are known as the i_{th} moment of x and u, respectively. Moment matching is a method to represent the finite unknown moments of the left hand side of (14) in terms of the known moments of the right hand side. In standard method like PRIMA [14], the sources are impulse sources in the moment matching process in order to preserve the input-output transfer characteristics. The impulse sources are constant in the frequency domain and have contribution only in the initial vector for the Krylov iteration. Then (14) can be rewritten as

$$(G + sC)(m_0 + m_1 s + m_2 s^2 + ...) = Bu_0. \tag{15}$$

This results in an iterative relationship between the moments: $Gm_0 = Bu_0$, $Gm_i + Cm_{i-1} = 0$. However, there is numerical stability problems in such moment matching, especially in higher order iterations. To avoid the numerical errors, an orthogonal bases V based on Krylov subspace, which is defined as $Kr(A, R, q) = colsp(R, AR, A^2R, ..., A^{q-1}R)$ with $A = -G^{-1}C$ and $R = G^{-1}B$, is constructed to span the same subspace spanned by finite moments of $x(s)$. Thus the order-reduced model can be obtained by projecting the original system onto the Krylov subspace by congruent transformation

$$\tilde{G}\tilde{x} + s\tilde{C}\tilde{x} = \tilde{B}u \tag{16}$$

where $\tilde{G} = V^T GV$, $\tilde{C} = V^T CV$, and $\tilde{B} = V^T B$.

However, the bottleneck in such method is the number of sources in the input vector u due to the big size of B causing big Krylov subspace. This is especially difficult for solving the equivalent thermal circuit which has a large number of independent current sources.

3.1 IEKS

The proposed method is inspired by the EKS method [15] which directly calculates the orthogonalized moments of the response when multiple sources are turned on at the same time. Therefore, unlike PRIMA whose runtime is heavily dependent on the port number, the runtime of EKS is independent of that. EKS models the piece-wise-linear (PWL) independent sources as a sum of delayed ramps in frequency domain

$$u(s) = \frac{1}{s^2}\sum_{i=1}^{N} r_i exp(-\beta_i s). \tag{17}$$

This expression contains $1/s$ and $1/s^2$ terms. In general, the traditional Krylov subspace methods start the moment matching from the 0^{th} moment. EKS extends the Krylov subspace by shifting the moments in the frequency spectrum. However, the moment shifting in EKS is tedious and error-prone. Therefore, an improved moment calculation method is proposed for thermal simulation, IEKS, which ensures the -1^{st} and -2^{nd} order moments are zero for arbitrary finite time PWL waveforms and the moment shifting process can be eliminated. Since only a specific time period is interested for a specific time period, the finite-time assumption is quite general. We believe this procedure is numerically more sound than the original approach.

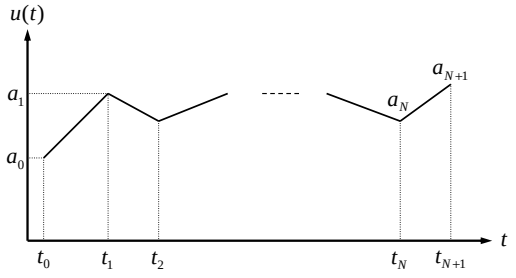

Figure 4. PWL waveform of the input source

For a given finite-time PWL source, the moment representation of IEKS with -1^{st} and -2^{nd} order are zero. Suppose that

the given finite-time PWL source $u(t)$ is

$$u(t) = \sum_{i=0}^{N} \left\{ [a_i + \gamma_i (t - t_i)] \, \mathrm{E}_{(t-t_i)} - [a_{i+1} + \gamma_i (t - t_{i+1})] \, \mathrm{E}_{(t-t_{i+1})} \right\}, \quad (18)$$

where $\gamma_i = (a_{i+1} - a_i)/(t_{i+1} - t_i)$ and $\mathrm{E}_{(t-t_i)}$ is the unit-step function with t_i delay. By taking the Laplace transform and Taylor expansion of (18), we have

$$u(s) = \frac{1}{s^2} \sum_{i=0}^{N} \left[a_i s \sum_{l=0}^{\infty} (-1)^l \frac{t_i^l}{l!} s^l + \gamma_i \sum_{l=0}^{\infty} (-1)^l \frac{t_i^l}{l!} s^l - a_{i+1} s \sum_{l=0}^{\infty} (-1)^l \frac{t_{i+1}^l}{l!} s^l - \gamma_i \sum_{l=0}^{\infty} (-1)^l \frac{t_{i+1}^l}{l!} s^l \right] \quad (19)$$

Let $\tilde{u}_i$ denote the coefficient of the s^i term, then (19) can be simplified as

$$\mathcal{L}(u(t)) = \left\{ \tilde{u}_{-2} s^{-2} + \tilde{u}_{-1} s^{-1} + \tilde{u}_0 + \tilde{u}_1 s + \tilde{u}_2 s^2 + \cdots + \tilde{u}_m s^m + \cdots \right\}. \quad (20)$$

After the detailed calculation, the first two coefficients, $\tilde{u}_{-2}$ and $\tilde{u}_{-1}$, are zero. The process of IEKS to calculate the first M moments is summarized in Table 2. The process of generating an orthogonal basis V for the corresponding moments is similar to [15].

Algorithm *Find the first M moments of PWL source*

Given
  PWL sources $\{a_0, \ldots, a_{N+1}; t_0, \ldots, t_{N+1}\}$
  The number of moments to calculate M
for $i = 0 \ldots N$
  $\gamma_i = \dfrac{(a_{i+1} - a_i)}{(t_{i+1} - t_i)}$
end
for $m = 1 \ldots M$
  for $i = 0 \ldots N+1$
    $\beta_i^{(m)} = \dfrac{(-t_i)^m}{m!}$
  end
  $\tilde{u}_{m-1} = (a_0 - \gamma_0 \dfrac{t_0}{m}) \beta_0^{(m-1)} - \sum_{i=0}^{N-1} (\gamma_i - \gamma_{i+1}) \beta_{i+1}^{(m)} - (a_{N+1} - \gamma_N \dfrac{t_{N+1}}{m}) \beta_{N+1}^{(m-1)}$
end

Table 2.

After generating a system transform matrix V, the original system is transformed into a compact description

$$\tilde{G}\tilde{X} + \tilde{C}\frac{d}{dt}\tilde{X} = \tilde{B}u. \quad (21)$$

The compact form can be solved quickly in the time domain by standard integration algorithms. The solution of the original system can be derived by $X = V\tilde{X}$.

4 Experimental Results

The proposed simulator with IEKS method was implemented with C++ language, and executed on a notebook with a $1.6\,GHz$ Pentium 4 processor and $640\,MB$ memory.

The extraction runtime of equivalent thermal circuits is not included in the runtime comparison. Figure 5 and Table 3 show the runtime comparison of the thermal simulation with the IEKS method and Tanner T-Spice for 1000 iterations. In the case of circuit-8 with 72428 nodes, the simulation with IEKS method took $221.21sec$. It is about 15 times faster than T-Spice.

Circuit	Node number	IEKS (s)	T-Spice (s)	Speedup (X)
Circuit-1	897	0.260	7.730	29.731
Circuit-2	3217	1.823	25.720	14.109
Circuit-3	7067	6.750	68.350	10.126
Circuit-4	12180	15.733	165.490	10.519
Circuit-5	19228	31.355	346.220	11.042
Circuit-6	27268	53.597	595.060	11.102
Circuit-7	36708	85.543	1059.080	12.381
Circuit-8	72428	221.210	3384.450	15.300

Table 3. Runtime of Thermal Circuits

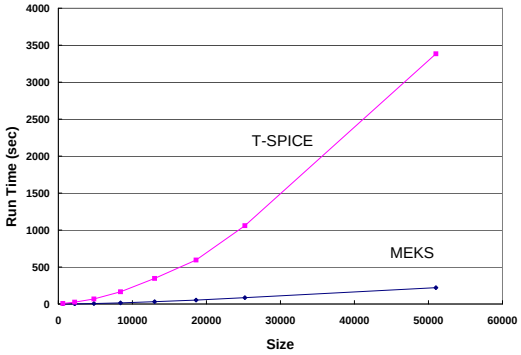

Figure 5. Runtime comparison of the simulation with IEKS method and T-Spice.

Next consider a chip with size $11.3\,mm \times 14.4\,mm$ and total power consumption $48W$. The chip is discretized with $\Delta x = 120\,\mu m$, $\Delta y = 120\,\mu m$, and $\Delta z = 20\,\mu m$. The effective heat transfer coefficients, h_i^e, are supposed to be $7 \times 10^3\ W/m^2K$ in the primary heat transfer path, and no heat transfer around the side faces. The simulation runs 1000 iterations with time increment $\Delta t = 10^{-3}\ sec$, and the results are shown in Figure 6. The average temperature is 52.41^oC, but the highest temperature is about $75\ ^oC$ which is influenced by the effective heat transfer coefficients and the location of power sources. There are three main parameters that affect the temperature: the board-level component population (thermal loading), the heat sink style and design, and the air velocity on the components and/or the heat sink [16]. From the results, we can observed that there are hot spots in the chip even though the average temperature may be low due to the improvement of the cooling technologies. These hot spots are the reliability concerns.

The transient simulation with IEKS method and T-Spice is tested and is shown in Figure 7. The difference of the results

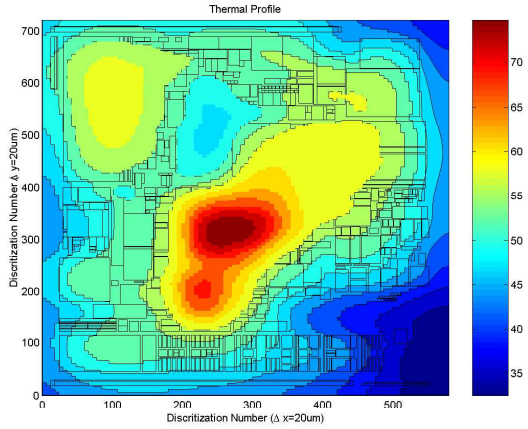

Figure 6. Temperature Profile.

between these two approaches is within 0.001%.

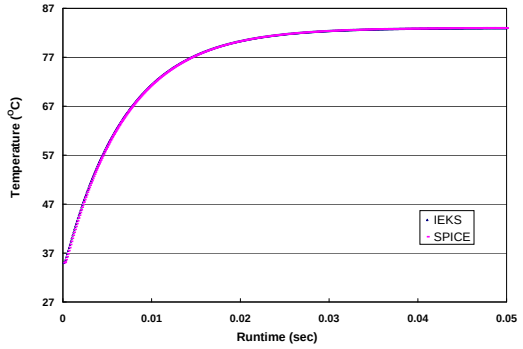

Figure 7. Transient results for the simulation with IEKS method and T-Spice.

5 Conclusion

In this paper, we propose a SPICE-compatible method of thermal simulation with lumped thermal circuit modeling for interconnect reliability analysis based on the IEKS method. Unlike the traditional model reduction method whose runtime is heavily dependent on the number of input ports, the runtime of the proposed method is independent of that. Therefore, the simulation runtime is improved significantly. In addition, the lumped thermal circuit modeling with adaptive approach reduces the formulated problem size. The proposed method can also be used for other interconnect related thermal applications.

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