SPICE Macro Model for MAGFET and its Applications

Shen-Iuan Liu, Jian-Fan Wei, and Guo-Ming Sung

***Abstract*— SPICE macro models for magnetic MOSFET (MAGFET) devices in the saturation region are presented. By using the proposed models, the performance of several readout circuits using MAGFET devices could be predictable. In this paper, the magnetic field-to-voltage converter, the magnetically controlled operational-transconductance amplifier, and the magnetically controlled filter and magnetic-operational amplifier using MAGFET devices have been designed, simulated, and tested. The proposed readout circuits using two different CMOS processes have been fabricated. Both simulation and measurement results verify the correctness and flexibility of the proposed SPICE macro models.**

***Index Terms*—Magnetic, MOSFET, circuit, sensor.**

I. Introduction

THE magnetic MOSFET (MAGFET) device is one kind of magnetic sensor which can sense the magnetic field and convert the magnetic field into a corresponding electrical signal such as voltage, current, frequency, etc. [1]–[3]. Its physical structure usually has two or three adjacent drain terminals [4]. With the split-drain structure, MAGFET can sense the magnetic field which is perpendicular to the channel of the device. In some applications [4]–[8], the Hall sensor is more popular than MAGFET, since the latter is more temperature-dependent, has large offset [9], and is noisier. Although there is similar physical operation between the two devices, the resulting output signals are much different. The Hall sensor is the transducer that converts magnetic field into Hall voltage, owing to the Hall effect. However, MAGFET can produce the corresponding current signal with respect to the external magnetic field. Additionally, the ideas to design the readout circuits for these two devices are also different. For the Hall sensor, it is a standalone device for the readout circuit, but MAGFET can be combined into the readout circuit.

In the absence of a magnetic field, the operation of MAGFET is the same as that of MOSFET. As a result, MOSFET can be easily replaced by MAGFET in the readout circuit. The evaluation of the circuits built by MAGFET devices is very important but difficult. In this paper, SPICE macro models of MAGFET will be offered to evaluate the performance of the circuits. This paper is constructed as follows. The operational principle of MAGFET and how the SPICE macro model is formed are described in Section II.

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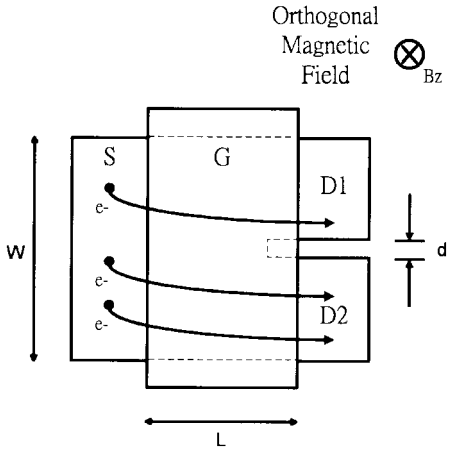


Fig. 1. Layout of the concave MAGFET device.

Some practical readout circuits consisting of MAGFET are presented in Section III. The simulation and experimental results of these circuits are also presented in Section IV. Some conclusions are summarized in Section V. At last, the netlist file of SPICE models for MAGFET is listed in the Appendix. Our SPICE version is HSPICE [10].

II. Principle

The Hall effect is the basic principle of MAGFET. The law of physics in a semiconductor is the formation of the Lorentz force F_B on an electrical charge q_e moving in a stable magnetic field B_Z with speed v

$$F_B = q_e \cdot (v \times B_Z) = q_e \cdot E_H \tag{1}$$

where E_H represents the equivalent Hall electrical field intensity [11]. Fig. 1 shows the physical structure of MAGFET with two adjacent drains, $D1$ and $D2$ [4]. For the MAGFET device, it is equivalent to two MOSFET devices that have just one-half the width of the MAGFET. So, the two drain currents are ideally equal if no magnetic field exists. Under the influence of a perpendicular magnetic field, the current imbalance of the two drains occurs. Due to the Hall effect, the MOSFET device with two adjacent, but isolated, drains can sense the perpendicular magnetic field. Another MAGFET structure is shown in Fig. 2. Compared to the gap-isolation of the origin MAGFET, the ploy gate is used to form isolation between two drain regions. The former is called "concave MAGFET," and the latter is called "convex MAGFET."

SPICE macro models for these two kinds of MAGFET are developed. For concave MAGFET, its equivalent circuit is

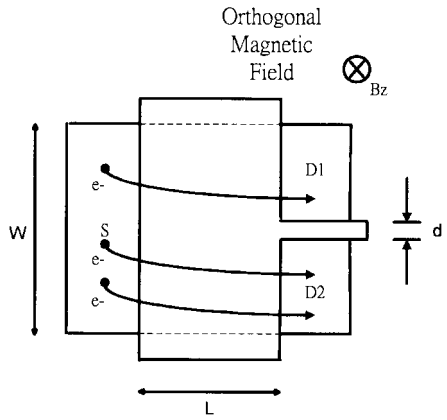


Fig. 2. Layout of the convex MAGFET device.

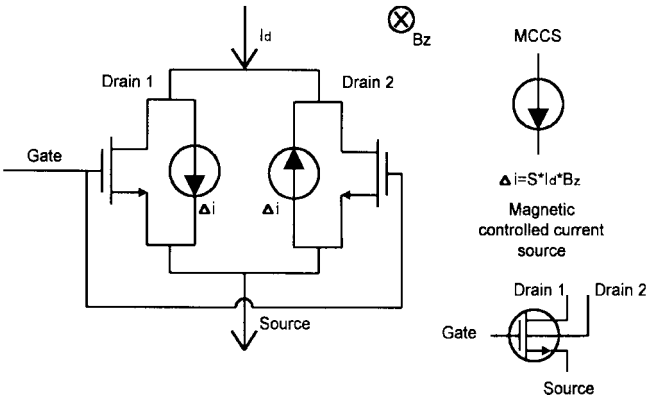


Fig. 3. SPICE model for the concave MAGFET device.

shown in Fig. 3 and the corresponding net-list file is given in the appendix. The magnetic control current source (MCCS) in Fig. 3 is used to model the current deviation caused by the external magnetic field. The quantity of MCCS is calculated by relative sensitivity of MAGFET, i.e.,

$$\Delta i = S \cdot I_d \cdot B_Z \tag{2}$$

where I_d is the bias current of MAGFET, S is the relative sensitivity of MAGFET, and B_Z is the perpendicular magnetic field. In the net-list file, the voltage source $V_{\rm mag}$ is used to represent the external magnetic field B_Z. The value of the relative sensitivity S is proportional to the inverse value of the resistor $R_{\rm sen}$. For the convex MAGFET, a similar model in Fig. 4 is developed. However, since the ploy gate is used to isolate two drains, a small parasitic MOSFET should be included. Fig. 4 shows the equivalent circuit for the convex MAGFET, and the corresponding net-list file is also given in the Appendix.

III. Circuit Description

The magnetic field-to-voltage converter (B-to-V converter) is shown in Fig. 5. V_t-referenced self-biased circuit [12] is used to bias the proposed circuit. Three sets of cascode current mirrors are used to stream out the current difference $2\Delta i$ of MAGFET. At last, M_1 and M_2 can be equivalent to a ground

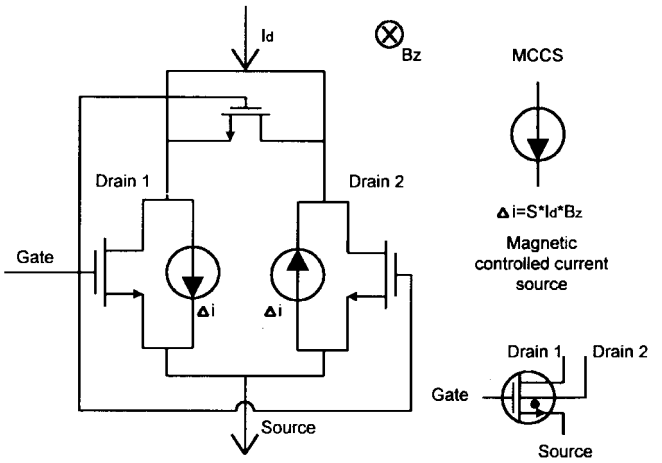


Fig. 4. SPICE model for the convex MAGFET device.

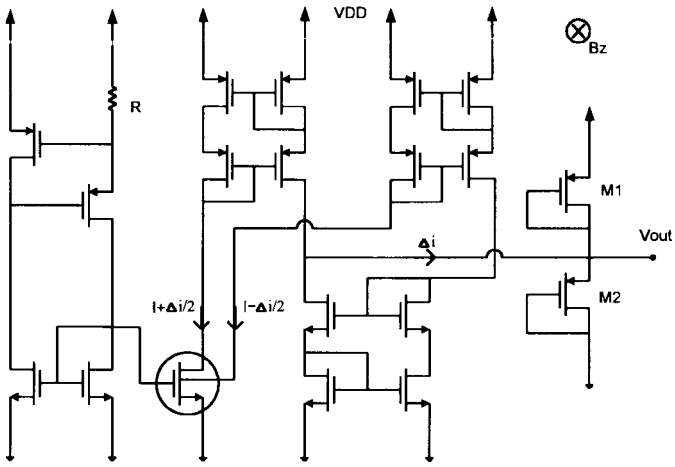


Fig. 5. The magnetic-to-voltage (B-to-V) converter.

resistor [13]. Its equivalent resistance can be expressed as

$$R_{\rm eq} = \frac{1}{2K(V_{\rm dd} - 2V_T)}. \tag{3}$$

The output voltage of this B-to-V converter will be proportional to the external magnetic field which does not enter into the nonlinear region.

Fig. 6 shows the operational transconductance amplifier (OTA), where its transconductance can be controlled by the external magnetic field. The additional pMOS diode-connected current mirrors are used to balance the loads of differential pairs. For the left-half part of the OTA, its transconductance value can be approximated to be

$$g_{ml} = \sqrt{2K(I + \Delta - \Delta i/2)}. \tag{4}$$

Similarly, the transconductance value of the right-half circuit can be

$$g_{mr} = \sqrt{2K(I - \Delta i/2)}. \tag{5}$$

So, the total transconductance value can be approximated as

$$g_{mt} = \sqrt{\frac{K}{2I}}\,\Delta i \propto B_Z, \qquad \text{if } \Delta i \ll I. \tag{6}$$

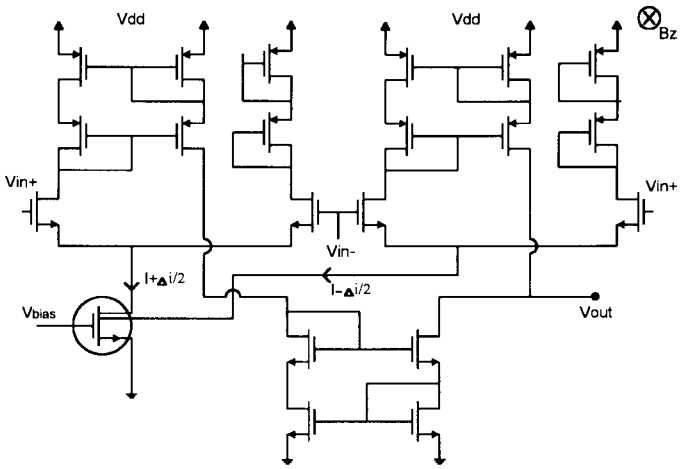


Fig. 6. Circuit configuration of OTA.

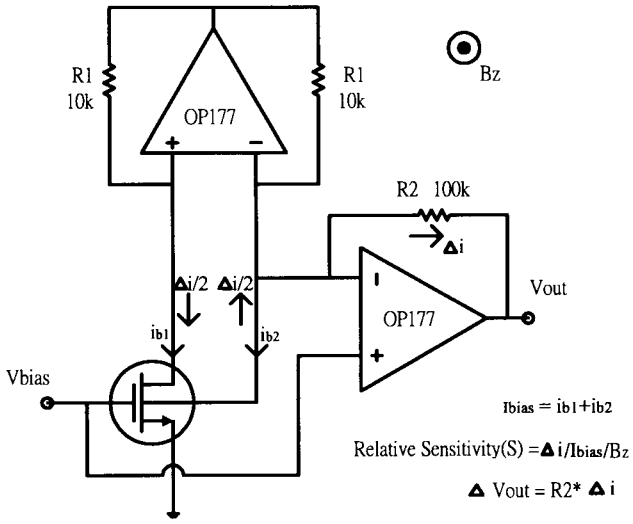


Fig. 7. Readout circuit for the MAGFET device.

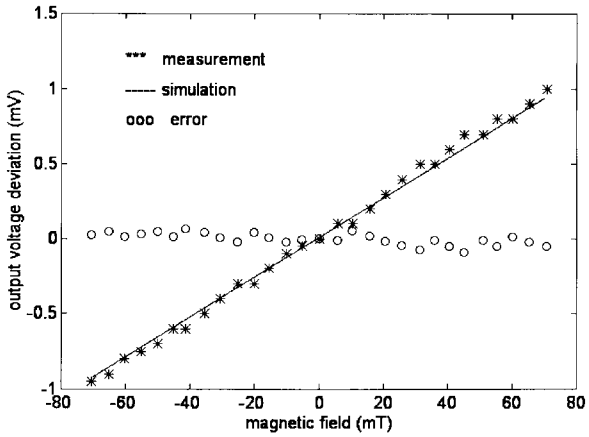


Fig. 8. Simulation and measurement results of the B-to-V converter using the concave MAGFET device.

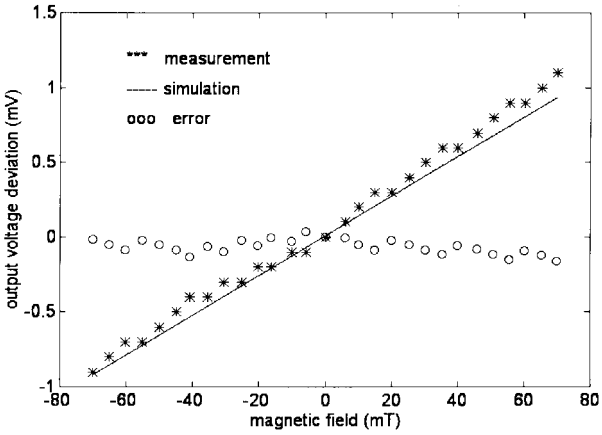


Fig. 9. Simulation and measurement results of the B-to-V converter using the convex MAGFET device.

This OTA has also been used to implement a magnetically controlled first-order filter. Its measurement results will be reported later.

Fig. 7 shows the readout circuit to measure the concave and convex MAGFET device [14]. The operational amplifier must be low-offset to avoid the undesired deviations. The deviation of the output voltage will be proportional to the current deviation of MAGFET caused by the external magnetic field. Their relation can be given as

$$\Delta V_{\text{out}} = R_2 \cdot \Delta i. \tag{7}$$

This readout circuit is used to extract the relative sensitivity for the MAGFET devices.

IV. Simulation and Measurement

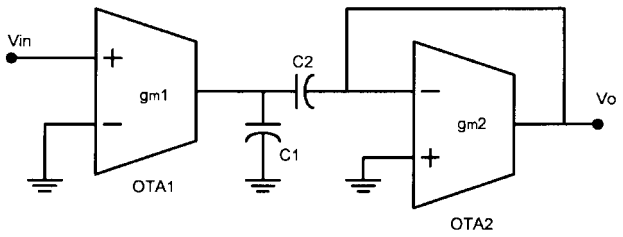
The B-to-V converter in Fig. 5 has been fabricated in a commercial 0.6 μm single-poly double-metal (SPDM) CMOS process [15]. The die area is 0.033 mm^2 and the power dissipation is 3.4 mW at the single supply 5 V. The OTA circuit in Fig. 7 and the magnetic operational amplifier have been fabricated in a commercial 0.8-μm SPDM CMOS process [16]. The die area of the OTA is 0.083 mm^2 and its power dissipation is 1.5 mW. The concave and convex MAGFET devices have also been fabricated in both the above processes [15], [16]. The simulation and measurement results of the readout circuits are discussed as follows:

A. B-to-V Converter

The B-to-V converter built with the concave MAGFET device in Fig. 1 ($W = 100\mu$m, $L = 50\mu$m, and $d = 4\mu$m) is considered. Fig. 8 shows the simulation and measurement of the output voltage deviation of the B-to-V converter versus the external magnetic field. In Fig. 8, the output voltage difference is linearly proportional to the magnetic field. The measured linearity error is within 4.7% for ±70 mT external magnetic field. Additionally, the measured results fitted very well with the simulation results. Similar measurement results of the B-to-V converter with the convex MAGFET device are shown in Fig. 9.

B. Magnetically Controlled First-Order Filter Using OTA's

In order to test the magnetically controlled function of the OTA's, a first-order filter using the proposed OTA's is presented. The circuit configuration of the filter is shown in



$$\frac{V_o}{V_{in}} = \frac{g_{m1}}{sC_1 + g_{m2}\left(1 + C_1 / C_2\right)}$$

Fig. 10. First-order filter with OTA's.

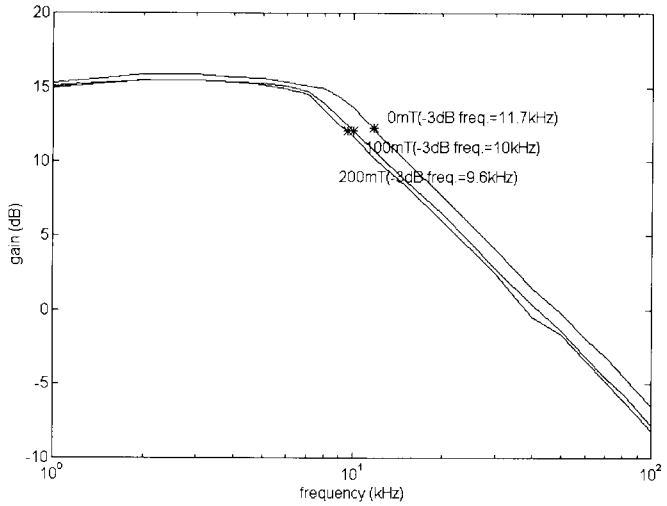


Fig. 11. Measured results of first-order filter.

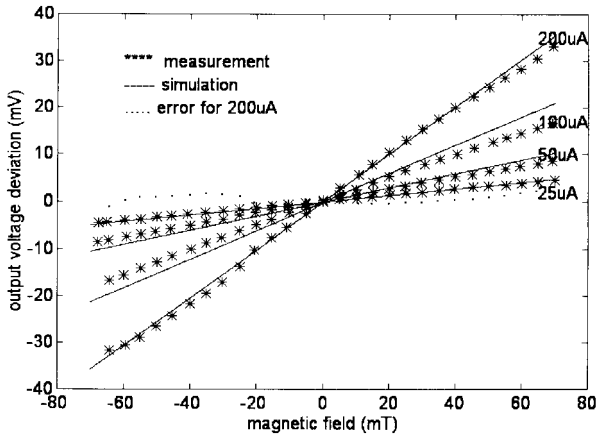


Fig. 12. Simulation and measurement results of the readout circuit using the concave MAGFET device.

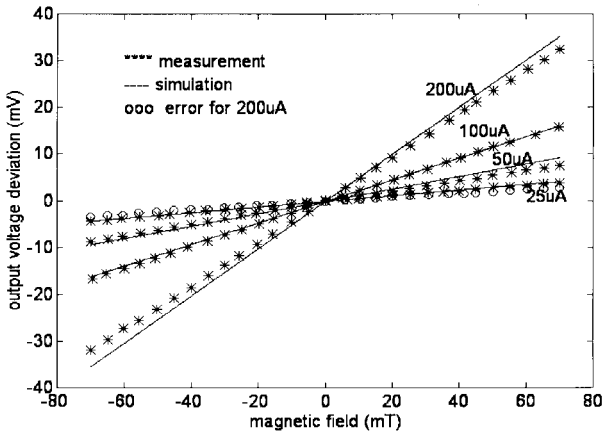


Fig. 13. Simulation and measurement results of the readout circuit using the convex MAGFET device.

Fig. 10 [17]. If the external magnetic field is applied to the OTA2, the -3-dB frequency of the first-order filter would be changed according to the transfer function in Fig. 10. Two off-chip capacitors C1 (200 pF) and C2 (300 pF) are used. The measured results are shown in Fig. 11. However, the dc gain has a little deviation. The reason might be that some magnetic flux enter into the OTA1 which causes the transconductance g_{m1} to vary.

C. Readout Circuit for the MAGFET Device

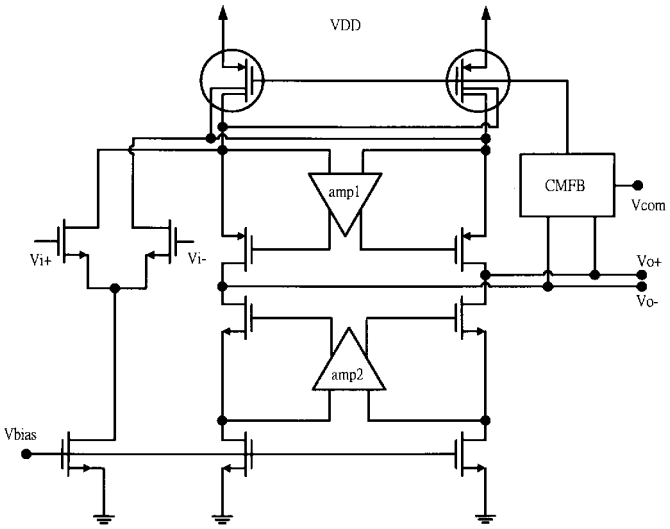
To test the characteristics of the convex and concave MAGFET devices, the discrete operational amplifier (OP177G) [18] with low-offset voltage is used. The values of the components are listed in Fig. 7. The simulation and measurement results of the concave and convex MAGFET devices for different bias current conditions are given in Figs. 12 and 13. It is obvious that these results are matched no matter which device is used. The measured relative sensitivities S for the magnetic nMOS and pMOS transistors are about $0.0125\mathrm{T}^{-1}$ and $0.0062\mathrm{T}^{-1}$, respectively.

D. Magnetic Operational Amplifier

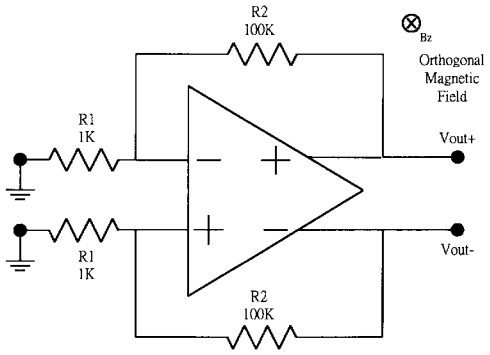
A fully-differential operational amplifier [19] with magnetic pMOS transistors as loads is shown in Fig. 14(a). This operational amplifier uses the gain boosting and continuous-time common-mode feedback circuit [20]. By crosscoupling the magnetic pMOS transistors, one can convert the current deviation caused by the external magnetic field into the output voltage. The test circuit is shown in Fig. 14(b). The measurement results with the concave MAGFET for different feedback resistors R_2 are shown in Fig. 15. The results for convex MAGFET are similar, but not shown.

V. Conclusion

Although MAGFET is not a standard device in the SPICE library, the macro models for the MAGFET devices are presented to evaluate the performance of circuits composed of the MOSFET and MAGFET devices. Two MAGFET devices and their readout circuits have been fabricated in two different CMOS processes. The experimental results have been compared with the simulation results of the proposed models. The correctness and flexibility of the proposed SPICE models have been verified. The proposed methods are expected to make the prediction of the circuits using the MAGFET and MOSFET devices possible.



(a)



(b)

Fig. 14. (a) The magnet operational amplifier. (b) The test circuit for (a).

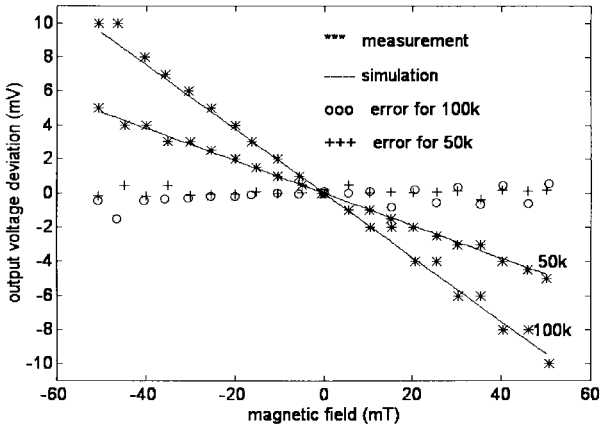


Fig. 15. The measurement results of Fig. 14(b) for different R_2 and $R_1 = 1$ kΩ.

APPENDIX

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* - - - - - - - - - - concave MAGFET - - - - - - - - - -
* - - - - - - - - - - sensor MAGFET - - - - - - - - - - -
Msen1 11 12 31 vss1 nm W=48u L=50u
Msen2 13 12 33 vss1 nm W=48u L=50u
Vsen+ 31 vss1 dc 0V
Vsen− 33 vss1 dc 0V
* - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
* - - - - - - - magnetic current simulation - - - - - - -
Hsen+ 1 vss1 Vsen+ 1
Hsen− 2 vss1 Vsen− 1
Rsen+ 1 vss1 1 Meg
Rsen− 2 vss1 1 Meg
Vmag 3 vss1 x        *****external magnetic field
Rsen 3 4 2000        *****1/sensitivity
vtt 4 vss1 dc 0 v
Hmag 5 vss1 Vtt 1
Rmag 5 vss1 1 Meg
Gmag+ 31 11 poly(2) 1 vss1 5 vss1 0 0 0 0 1 0
Gmag− 13 33 poly(2) 2 vss1 5 vss1 0 0 0 0 1 0
* - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

* - - - - - - - - - convex MAGFET - - - - - - - - - - -
* - - - - - - - - - sensor MAGFET - - - - - - - - - - - -
Msen1 11 12 31 vss1 nm W=48u L=50u
Msen2 13 12 33 vss1 nm W=48u L=50u
Mpara 11 12 13 vss1 nm W=6.5u L=4u
Vsen+ 31 vss1 dc 0 V
Vsen− 33 vss1 dc 0 V
* - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

* - - - - - - - magnetic current simulation - - - - - - -
Hsen+ 1 vss1 Vsen+ 1
Hsen− 2 vss1 Vsen− 1
Rsen+ 1 vss1 1 Meg
Rsen− 2 vss1 1 Meg
Vmag 3 vss1 x        *****external magnetic field
Rsen 3 4 2000        *****1/sensitivity
vtt 4 vss1 dc 0 v
Hmag 5 vss1 Vtt 1
Rmag 5 vss1 1 Meg
Gmag+ 31 11 poly(2) 1 vss1 5 vss1 0 0 0 0 1 0
Gmag− 13 33 poly(2) 2 vss1 5 vss1 0 0 0 0 1 0
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
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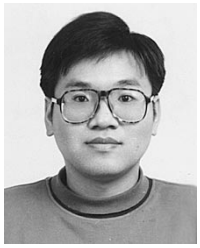

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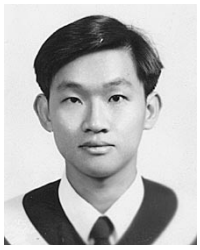

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