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SPICE Model Libraries for Via Transitions

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Abstract

A procedure of building SPICE models for signal via transitions between printed circuit board layers is presented in this paper. The method of extracting parameters of SPICE models from full-wave simulation tool is demonstrated. Then the validity of SPICE models is studied by comparing the solution from SPICE model with that from the full-wave simulation.

Keywords

PCB, multilayer PCB, CEMPIE, PEEC, SPICE, via transition.

Introduction

In high-speed digital designs, signal transitions from layer to layer through vias on printed circuit board (PCB) are becoming an important signal integrity issue. When the data rate is greater than a giga-bit per second, via transitions can slow down the signal and degrade the signal. Efficient and accurate models for via transitions can be important for high bit-rate digital circuit system designs. These models should be compatible with fast running simulation tools, such as SPICE.

Prior work focused on the impacts of the via on the signal quality [1-3]. In this paper, a procedure to build a SPICE model library for via transitions on multilayered board is proposed. Using this library, SPICE models for various vias on a specified PCB stackup are constructed by cascading "building blocks", which are SPICE models for elements of the via structure. A full-wave numerical approach, CEMPIE/PEEC (Circuit Extraction based on Mixed Potential Integral Equation-Partial Element Equivalent Circuit)[4], was used to extract the lumped element parameters of these "building blocks".

Modeling a via with CEMPIE and SPICE

To validate the reliability of CEMPIE/PEEC approach for modeling via transitions, a test PCB configuration shown in Fig. 1 was built and measured. It is a 15 by 10 cm four-layer board. A microstrip line goes from the top layer to the bottom layer through a via across the second and the third solid planes. A vertical SMA connector is mounted at every end of the microstrip line as measurement ports. The measured S-parameters have been compared with the CEMPIE/PEEC modeling. Fig. 2 shows the comparison. The shapes of modeled and measured results are the same, but there are resonance shifts between them.

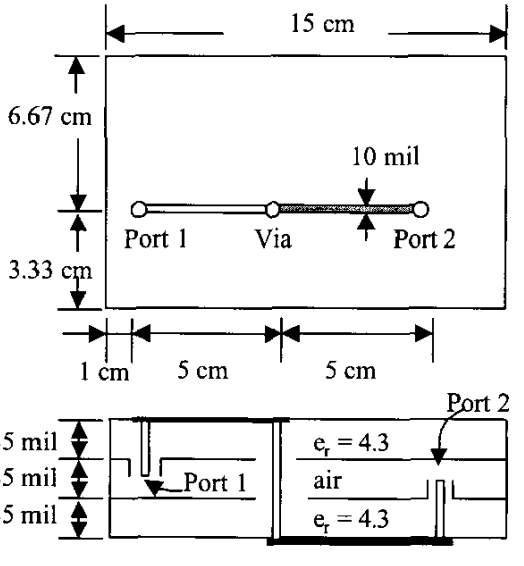
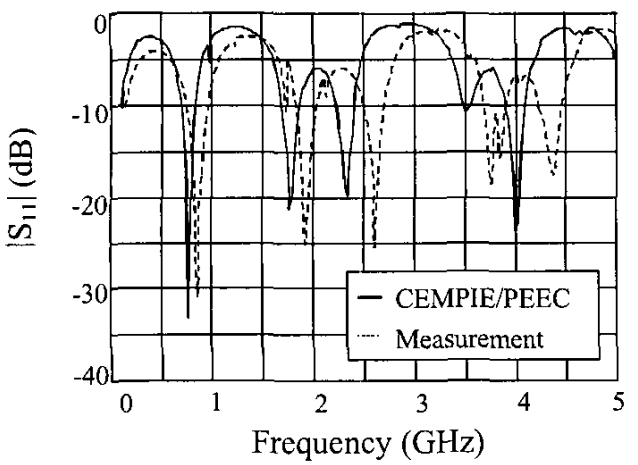
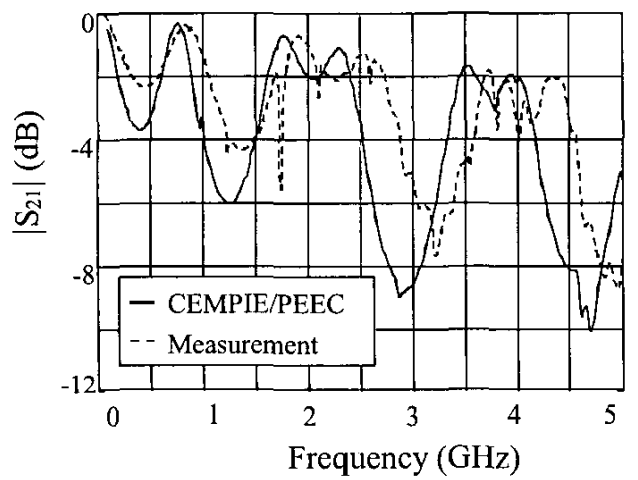


Fig. 1. Geometry of a test PCB configuration

A methodology for extracting SPICE models and developing a library



(a)



(b)

Fig. 2. Comparison of results (a) Magnitude of S_{11} (b) Magnitude of S_{21}

To simplify the modeling of via transitions, a multi-layer board can be viewed as many two-layer board elements laminated together. Every two-layer board element can then be modeled independently, which is called a "building block". The assumption of this procedure is to neglect coupling between blocks. Cascading building blocks assembles the whole model for the entire via transition. To demonstrate the procedure mentioned above, an example was investigated. The geometry of this case is similar to Fig. 1 as shown in Fig. 3. FR4 (e_r=4.3) material is used between all solid planes. The microstrip lines are shorter and there is no SMA jack at ends of microstrip lines. The first step is to separate the entire geometry into three building blocks. Among them the blocks above and below solid planes are same. Therefore, only two blocks were modeled independently. A SPICE model was constructed for each block. Then the SPICE model for the whole geometry is the models of the blocks in cascade, as shown in Fig. 4. To obtain the element values of each constructed SPICE model,

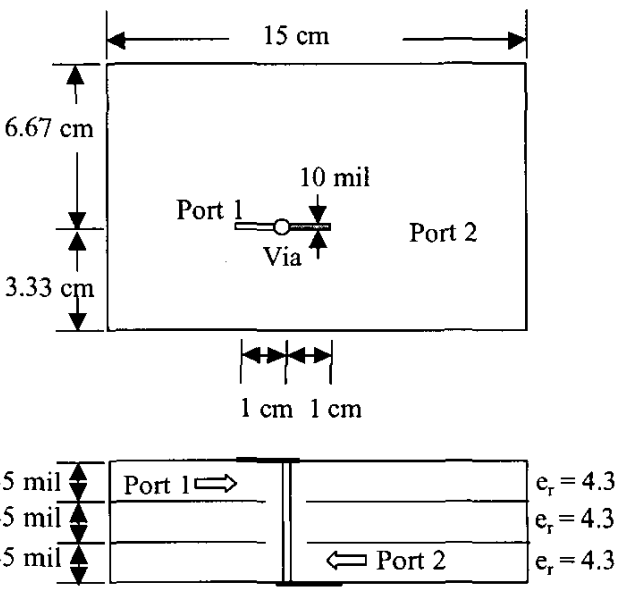


Fig. 3. Geometry of a via transition for model extraction

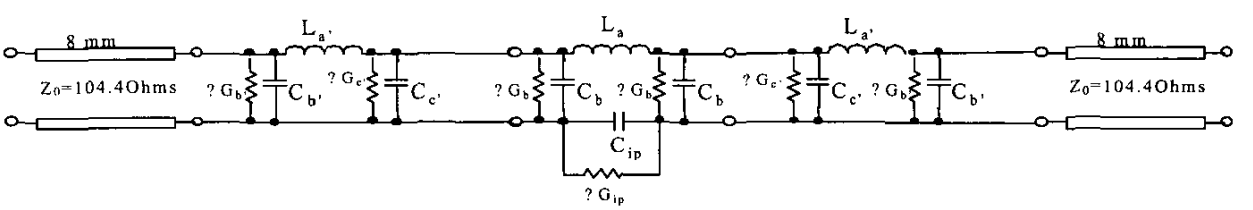


Fig. 4. Complete SPICE model for the entire via transition shown in Fig. 3

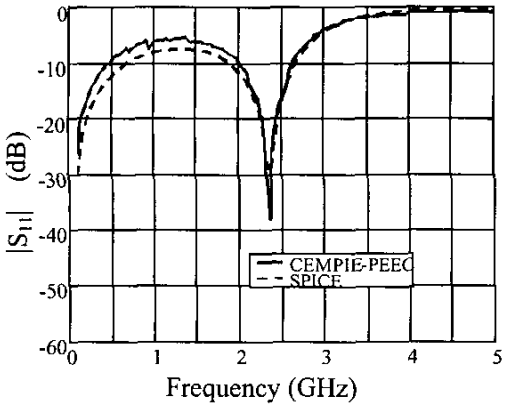
a nodal-based admittance matrix is acquired from CEMPIE/PEEC simulation. Consequently a Z-matrix for two external ports is solved from it. Also, a Z-matrix for external ports is obtained from the SPICE model. Comparing these two Z-matrices, the lumped element parameters in the SPICE model can be calculated [5]. As an example, those parameters for the block above/below solid planes are found to be

L_a ? 1.17nH,C_b ? 0.295pF
G_b? 0.00494pS/rad,C_{ip} ? 505pF,G_{ip}? 10.2pS/rad.

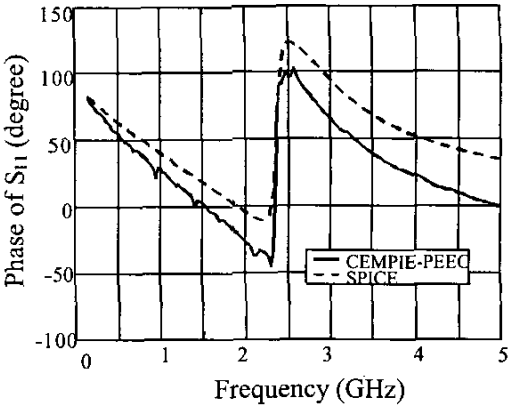
The block between two solid planes is modeled by the same method. S-parameters calculated using the CEMPIE/PEEC simulation and the entire SPICE model agree closely as shown in Fig. 5. The difference between the modeled values of $|S_{21}|$ is less than 1 dB at frequencies up to 4GHz.

Library matrix

An example of the library matrix for a 10-layer board was constructed to demonstrate the using of the procedure above in a real design environment. There are 6 building blocks shown in Fig. 6. Table 1 shows the geometries for 4 kinds of vias. Once the via needed to model is decided, which building blocks are needed and how to cascade them to construct a complete SPICE model can be know from Table 2. For example, a via connects two signal lines located in layer 3 and layer 8. The model for this via can be build by cascading the Block EBCBE. In the Table 2, underline represents the flip of the model, and the superscript 1 for Block 2 represents that Port 2 connects to



(a)



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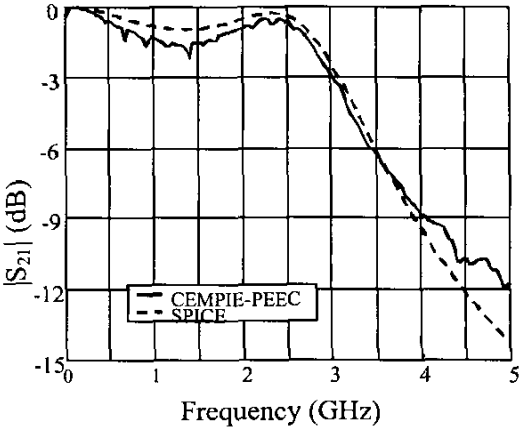
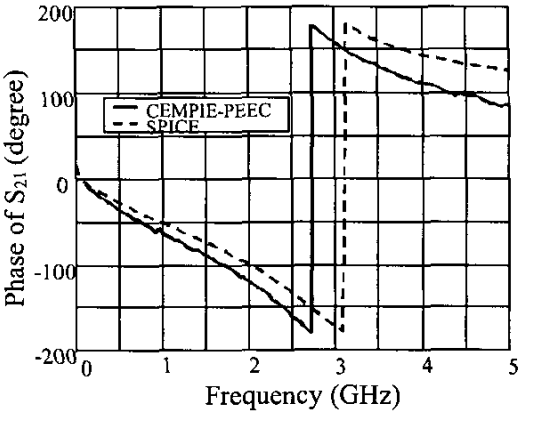


(c)



(d)

Fig. 5. Comparison of modeled results for the geometry shown in Fig. 3
(a) Magnitude of S_{11} (b) Phase of S_{11}
(c) Magnitude of S_{21} (d) Phase of S_{21}

signal path and Port 3 connects to via stub as shown in Fig. 7. By contraries the superscript 2 represents that Port 3 connects to signal path and Port 2 connects to via stub.

TABLE I

VIA GEOMETRIES IN A 10-LAYER BOARD

Through Hole Via Diameter (mils)	Via Pad Diameter (mils)	Via Anti-Pad Diameter (mils)
10	22	27
20	32	37
30	42	47
40	52	57

TABLE II

LIBRARY MATRIX FOR A 10-LAYER BOARD

	1	3	4	7	8	10
1		AB^1CDE	AB^2CDE	$ADCB^1E$	$ADCB^2E$	$ADCDA$
3			EFCDE	EB^1CB^1E	EB^1CB^2E	EBCDA
4				EB^2CB^1E	EB^2CB^2E	EBCDA
7					EDCFE	$EDCB^1A$
8						$EDCB^2A$
10						

Partitioning issues

A p-shape inductance and capacitance model is used to model the building block. Only one inductor is used in the model. The value of this inductor was not fixed and depends on the current distribution. When different building blocks are cascaded together, the current distribution is different than with an isolated building block. An artificial inductor is put between every two blocks when building blocks are cascaded together to compensate for the effect of current redistribution. An example for single-ended signaling was shown in Fig. 8,where a through hole via transverses a 4-layer board of dimensions 3 cm by 2 cm. The stack up of the board is shown in Fig. 8(a). Two ports are set by specifying two super nodes at the ends of a microstrip stub to model the entire geometry. The mesh patterns used in CEMPIE/PEEC are shown in Fig. 8 (b) and (c). After every block is modeled independently, a compensation inductance is put between every two connected blocks as shown in Fig. 9.

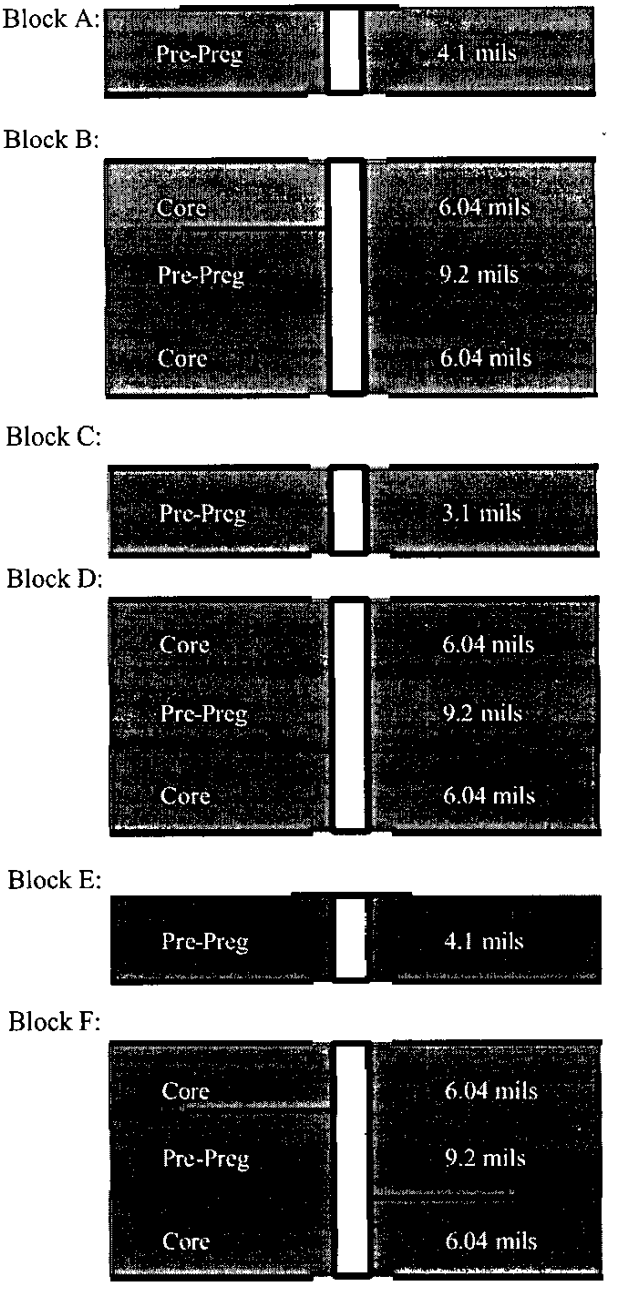


Fig. 6. Building blocks for a 10-layer board

Fig. 10 shows the simulation results of CEMPIE/PEEC for an entire geometry, a cascaded block A-D-A without and with compensation inductances. The value of the compensation inductance is estimated by curve fitting. The cascaded results are calculated from the S-parameters of blocks directly.

The impact of the transverse current and overall current distribution in the partitioning and peeling process, and the

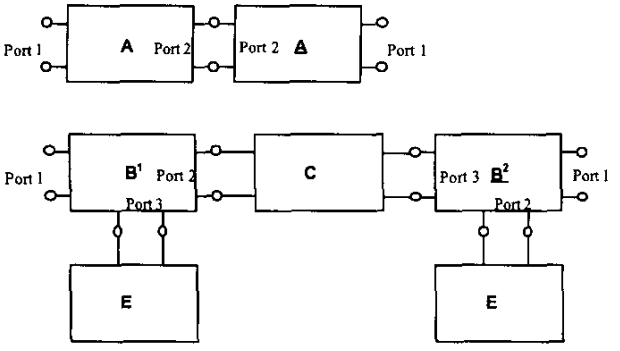
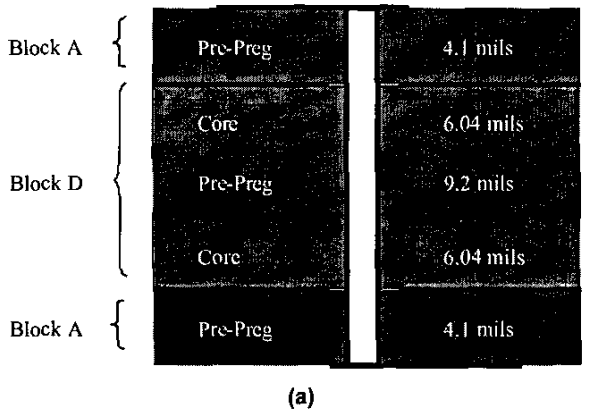
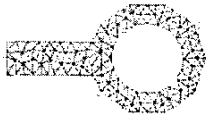


Fig. 7. The meanings of underline and superscript in the library matrix



(a)



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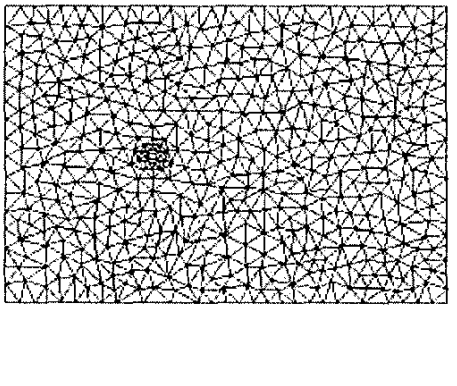

(c)

Fig. 8 A via geometry and mesh patterns (a) Side view (b) Mesh pattern of top and bottom layer (c) Mesh pattern of two middle layers

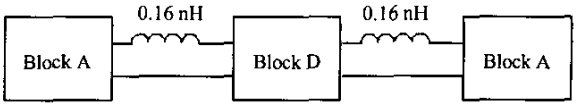

Fig. 9. Blocks and compensation inductances

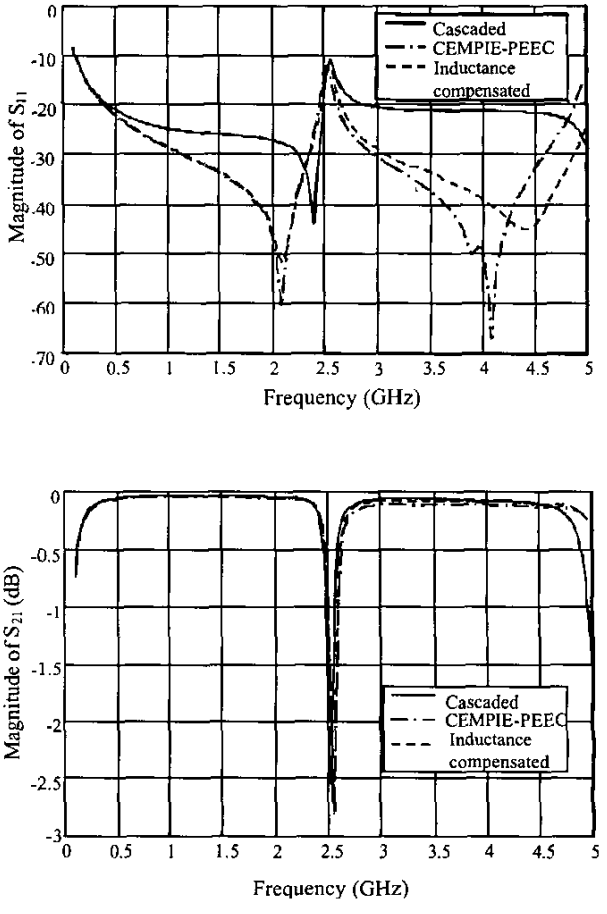

Fig. 10. Comparison of simulation results

relationship between the current distribution along a via body and the equivalent inductance of the via were investigated. The CEMPIE/PEEC tool currently does not model certain cases accurately. The difficulty is that the basis functions in the current numerical formulation do not allow for transverse currents on vertical structures, rather only in the planes. A partitioning process that does not incorporate the current distribution through the discontinuity correctly will not result in a correct model. Further, because there is not a pure TEM mode at the port connections, there are not well-defined voltages for the ports of individual blocks. This causes difficulties for the

partitioning process in modeling the current distribution along the via body correctly.

In practice, time domain simulations are more common in the design of high speed digital data links than frequency domain simulations. Therefore, the effect of the peeling process on a time domain simulation was investigated. Fig. 11 shows the eye diagrams of Block A D A cascaded and as an entire geometry in Fig. 8(a). The eye diagrams were produced with the 2 GBit/s input bit rate, 50 ps rise time (20%-80%), 3EB05H (comma, comma bar) as the format of bit pattern. The comparison of two eye diagrams is shown in Figure 11. The differences are small. The eye widths are 405 ps and 400 ps individually. The eye openings are 0.353 V and 0.356 V. The jitters at left edge are 15.3 ps and 18.4 ps. The jitters at right edge are 16.3 ps and 16.4 ps. Furthermore, shapes of two eye diagrams are similar. The transfer function $F = S_{21}/(1+S_{11})$ and the significant differences in S_{11} are at the nulls, which have small values as compared with one, the eye pattern is relatively insensitive to these differences of S_{11}. The small difference of the eye patterns is due to the slight difference in S_{21} and the peaks of S_{11}. These results show that the SPICE models in the library matrix are good for engineering studies, even without the compensation inductances.

Conclusions

For a given stackup of PCB, a SPICE model library for via transition can be built using the proposed method and every via on the board can be modeled by a few cascaded blocks in this library. With this model, simulation results are acceptable with errors approximately 1% up to 5 GHz in the time-domain.

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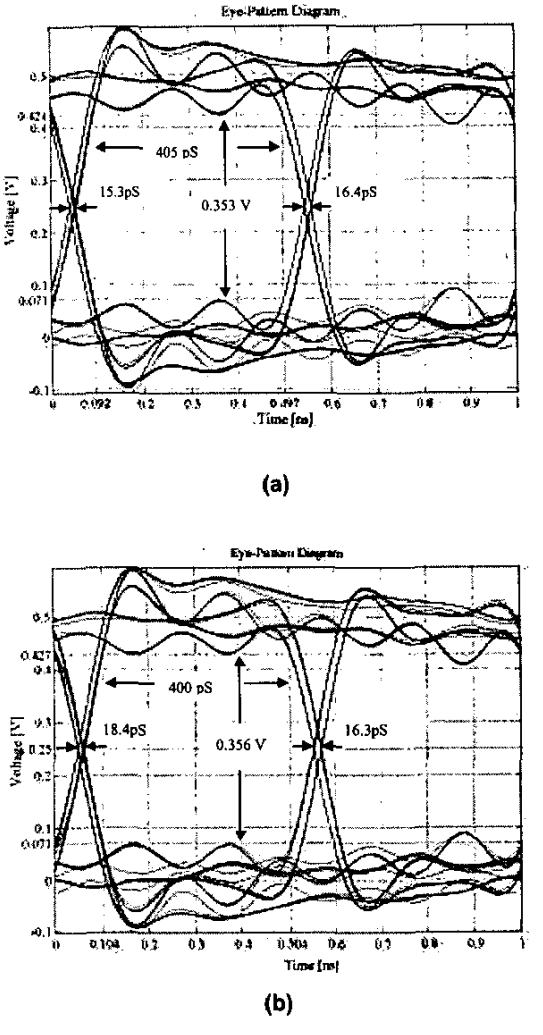

Fig. 11. Eye diagram from the transfer function of simulations (a) from entire geometry (b) from cascading results

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