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SPICE Modeling of Insulator Metal Transition: Model of the Critical Temperature

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ABSTRACT This paper proposes a compact SPICE phenomenological model for insulator metal transition (IMT) devices. The proposed model captures the interplay of electric field and Joule heating to effect a transition from a high resistance insulating state to a low resistance metallic state. The model is corroborated against experimental results and electrothermal simulations available in the literature. The proposed model is implemented in Verilog-A and is fully compatible with commercial SPICE simulators such as Spectre from Cadence, used in this paper. An IMT-based artificial neuron is then designed and simulated using the proposed IMT compact model and design expressions for the operation of the proposed neuron are derived. The simulation results agree with the expected neuron behavior as well as the simulation results of other similar neurons proposed in the literature. This paper will enable circuit designers to design and simulate IMT-based systems and help them explore the full potential of such novel devices.

INDEX TERMS Insulator metal transition, IMT, compact model, SPICE model, neuron, Mott transition.

I. INTRODUCTION

Insulator Metal Transition (IMT) devices have recently spurred significant interest in the research community [1], [2]. Their switching characteristics have shown to be ideal in applications such as crossbar memory arrays and neuromorphic circuits. For example, in crossbar arrays, IMTs show promising selector characteristics such as high ON/OFF ratio which circumvents sneak path currents and, more importantly, provide Back-End-Of-Line (BEOL) compatibility which helps achieve the ideal $4F^2$ density of crossbar arrays [3], [4]. On the neuromorhpic front, researchers have shown that IMTs can be leveraged in building Integrate-And-Fire (IAF) neurons without the need for complex CMOS circuitry owing to their inherent switching dynamics, thus, providing a significant density advantage [5], [6].

Several works have presented experimental studies on IMT devices attempting to unravel the underlying switching mechanisms contributing to phase transition. Several studies have shown that temperature is the prime cause of phase transition such as the work in [7] and [8] while others have attributed the transition to the electric field [9] with temperature playing a secondary role. A more in depth study about the switching mechanism is presented in [10] and [11] which show that Joule heating may not be sufficient for phase transition and an electric field assisted transition is more plausible. Yang *et al.* [10] hypothesize that a certain threshold voltage is required to effect a phase transition which decreases with increasing temperature. Lin *et al.* [12] have classified IMT devices into two categories: Electronic IMT (E-IMT) and Thermally-driven IMT (T-IMT) and the characteristics of each type have been studied.

The lack of a physics-based compact model, however, has hindered circuit designers from exploring the full potential of IMTs in circuit applications. In particular, understanding the interplay between temperature and electric field has been the main stumbling block to the development of such a compact model [12]. In [5], an electro-thermal model was developed for IMT devices which leverages the positive electro-thermal

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feedback to effect a phase transition of the device. The model was compared to vanadium oxide (VO_2) experimental data and could reproduce the data with sufficient accuracy. In [13], a similar model was developed based on the Mott insulator theory and provides a device simulation framework for modeling IMT devices.

On the neuromorphic front, researchers found that the intrinsic dynamics of IMT devices can be leveraged in the design of artificial neurons. In [6] and [14], an IMT-based neuron was proposed. This work, however, did not include the temperature dynamics in the IMT model nor did it study their effect on the IMT-based neuron. In [15] and [16], an IMT-based neuron coupled with a temperature-based model for the IMT device was proposed. However, the model proposed in that work is complex and may not be readily integrated in SPICE simulators nor can it be easily used to derive simple design expressions to facilitate the design process for IMT neurons. Also, the neurons proposed in these works are studied in isolation and do not show how they can be integrated in a larger system.

In this work, a SPICE compatible IMT compact model is developed and implemented in Verilog-A. The proposed model describes the IMT device as a memristive system wherein the state variable is the local temperature of the device. The model is simulated using Spectre from Cadence and shows a close match to experimental results and electrothermal simulations based on the models in [5] and [13]. Using the proposed model, an IMT based artificial neuron is designed and simulated using Spectre from Cadence. Design expressions and oscillation conditions for the proposed design are derived based on the proposed model. Background about previous modeling efforts for IMT devices is described in Section II. Section III describes the proposed compact model. Section IV validates the model against experimental data and electrothermal simulations available in the literature. The IMT-based artificial neuron is described in Section V and the proposed design is presented in Section VI. Section VII provides discussions and future prospects about IMT fabrication and device requirements and Section VIII presents the conclusions.

II. BACKGROUND

Two IMT device models were proposed in [5] and [13]. In [5], a device model that captures the positive feedback between the temperature and electric field was presented. In this model, however, the relationship between the device resistance and the device temperature was implemented using a look up table. This method, while it might be favorable in a device simulation framework, is not compatible with SPICE simulators which require closed form compact models for efficient circuit simulation.

A more refined device model was developed in [13] based on band theory. The IMT device is modeled as a low bandgap semiconductor. Increasing the device temperature results in decreasing the bandgap. This decrease in the bandgap results in an increase of the carrier concentration which ultimately results in decreasing the device resistance. A model is also presented which captures the change in the thermal conductivity with temperature. The bandgap model and the thermal conductivity model are then solved in a self consistent manner to effect a phase transition as a function of temperature. The model in [13] was implemented in Sentaurus TCAD simulator wherein the built-in electrothermal models and finite element drift-diffusion model where leveraged. This model, similar to the previous one, is best used in a TCAD simulation flow and not SPICE level simulators.

The proposed compact model, presented in the next section, builds upon both electrothemal models wherein simplifications such as using lumped element thermal model and proposing a phenomenological relationship between the device temperature and resistance were employed to arrive at a closed form model suitable for integration in commercial SPICE simulators.

III. THE PROPOSED IMT SPICE MODEL

The switching dynamics of IMT devices have been attributed to the interaction of electric field and Joule heating as alluded to before. As the current flows through the device, the device temperature rises until it hits a critical temperature at which point the device transitions from a high resistance insulating phase to a low resistance metallic phase. As the device cools down, the resistance relaxes back to its initial high resistance state.

Here we leverage the memristor theory [17]–[19] to describe the IMT device. The memristive dynamics of the IMT device can be described as follows [20]:

$$I = G(x).V, \tag{1}$$

$$\frac{dx}{dt} = g(x, V), \tag{2}$$

where (1) and (2) describe the output and state equations, respectively, with x being the state variable. The proposed model has two main governing equations: (I) the resistance change equation which corresponds to the output equation (here we used the resistance rather than conductance for modeling convenience) and (II) the temperature evolution equation which corresponds to the state equation, with the temperature being the state variable such that $x = T(t)$.

The behavior of the resistance change versus temperature can be captured by two thermistor states for the high resistance and low resistance states and a sigmoid function for the transition from a high resistance state to a low resistance state. Since the thermistance behavior depicts a linear relationship between the resistance and the temperature in the Log-Linear plot, one can simply model the two thermistor states as exponential functions of the temperature such that $R_{LRS} = R_{LRS_F} e^{-B_{LRS}(T(t)-T_F)}$ and $R_{HRS} = R_{HRS_0} e^{-B_{HRS}(T(t)-T_0)}$. R_{LRS_F} is the low resistance state defined at temperature T_F (a reference temperature) and R_{HRS_0} is the high resistance state defined at the ambient temperature T_0. B_{LRS} and B_{HRS} are the temperature coefficients which are extracted from the slope of the thermistance

vs. temperature plot and the negative sign describes Negative Temperature Coefficient (NTC) thermistors. This implementation, however, requires clipping of the R_{LRS} and R_{HRS} at some minimum and maximum values to avoid any unphysical behavior during circuit simulation. Clipping, however, requires the use of conditionals which hampers the "smoothness" of the model yielding potential convergence difficulties during circuit simulation. Hence, we reformulate the model equations such that R_{LRS} and R_{HRS} smoothly plateau to R_{LRS_F} and R_{HRS_0} at high and low temperatures, respectively.

This relationship between the temperature and the resistance can be expressed as follows:

$$R_{LRS} = R_{LRS_F}(1 + K_{LRS}{}^{A})^{\frac{1}{A}}, \tag{3a}$$

$$R_{HRS} = R_{HRS_0}\left(\frac{K_{HRS}}{(1 + K_{HRS}{}^{A})^{\frac{1}{A}}}\right), \tag{3b}$$

$$R_{IMT} = R_{LRS} + \frac{(R_{HRS} - R_{LRS})}{1 + e^{\frac{T(t)-T_c}{T_x}}}, \tag{3c}$$

where $K_{LRS} = e^{-B_{LRS}(T(t)-T_F)}$ and $K_{HRS} = e^{-B_{HRS}(T(t)-T_0)}$. T_x is a fitting parameter that captures the sharpness of the resistive transition. T_c is the critical temperature which is around 340K in the case of VO_2 devices [6]. R_{LRS} and R_{HRS} are the Low Resistance State and High Resistance State, respectively. A is a control parameter which governs how the two thermistor states approach the asymptotes [21]. In this work, $A = 10^4$ is used. However, this parameter can be varied by the user as needed. While the model might seem complicated at first glance, the principal equations are simple exponential functions as aforementioned. This formulation is only employed to abide by compact modeling practices as suggested in [21] and [22]. Appendix A provides a more thorough explanation for (3) and describes the parameter extraction procedure.

The temperature evolution dynamics are described by the compact thermal model in [23] as shown in (4):

$$C_{th}\frac{dT(t)}{dt} = V_{IMT}I_{IMT} - \frac{(T(t) - T_0)}{R_{th}}, \tag{4}$$

where $V_{IMT}I_{IMT}$ is the Joule heating, C_{th} and R_{th} are the effective thermal capacitance and the effective thermal resistance, respectively, and T_0 is the ambient temperature. This model assumes that the device stays at an effective temperature $T(t)$ and exchanges heat with the ambient environment at an ambient temperature T_0.

Listing 1 depicts Verilog-A code snippet of the core model equations. Suggested good practices for writing compact models are considered based on the work in [24] and [25]. Note that (3a) and (3b) are each split into two equations in the VerilogA implementation. This formulation is to avoid numerical overflow as the values for K_{LRS} and K_{HRS} become large; see [21] for more detailed explanation. However, one can readily show that the expressions in each conditional are mathematically identical and, hence, the use of conditionals will not introduce any discontinuities.

```
Iwr = I(p,n);
 V(p,n) <+ Iwr*Rm;


K_HRS=exp(-B_HRS*(tem-T_0));
K_LRS=exp(-B_LRS*(tem-T_F));

if (tem>T_F) begin
  LRS=LRSF*pow((1+pow(K_LRS,A)),1/A);
end
else begin
  LRS=LRSF*K_LRS*pow((1+pow(K_LRS,-A)),1/A);
end

if (tem>T_0) begin
  HRS=HRS0*K_HRS/(pow((1+pow(K_HRS,A)),1/A));
end
else begin
  HRS=HRS0/(pow((1+pow(K_HRS,-A)),1/A));
end

Rm= LRS + (HRS-LRS)/(1+exp((tem-Tc)/Tx));
Pwr(temp)<+ ddt(Temp(temp));
Pwr(temp)<+ -pow(Iwr,2)*Rm/Cth;
Pwr(temp)<+(Temp(temp)-T0)/(Rth*Cth);
```

Listing 1. Verilog-A code snippet.

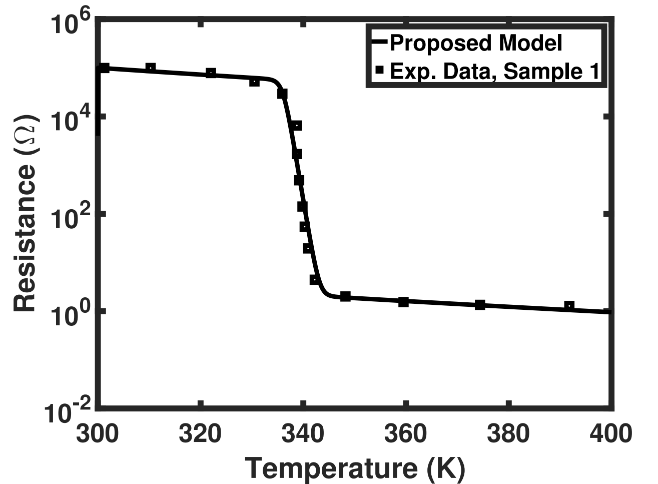

Fig. 1. Model fitting against experimental data.

IV. MODEL VALIDATION AGAINST EXPERIMENTAL RESULTS AND ELECTRO-THERMAL SIMULATIONS

The proposed model is validated against the results in [5]. The proposed model closely matches the experimental results as well as electro-thermal simulation as shown in Figs. 1, 2, 3, 4, 5 and 6. Fig. 1, 2 and 3 depict the resistive transition about the critical temperature which is about 340K in VO_2 devices fitted against experimental data from [5]. Fig. 4 depicts the hysteresis in the V-I plane (a fingerprint of memristive systems) exhibited by the IMT device as shown in [5] and [6] and fitted against the experimental data from [5]. Figures 5 and 6 depict the time dependence of temperature and resistance evolution, respectively, fitted against electrothermal simulations from [5]. Three voltage

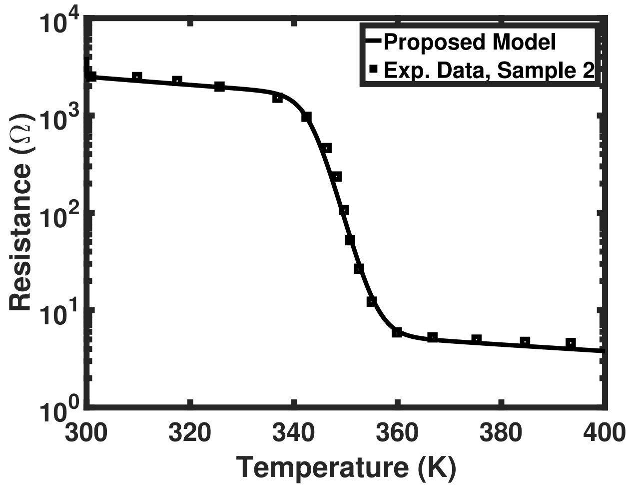

Fig. 2. Model fitting against experimental data.

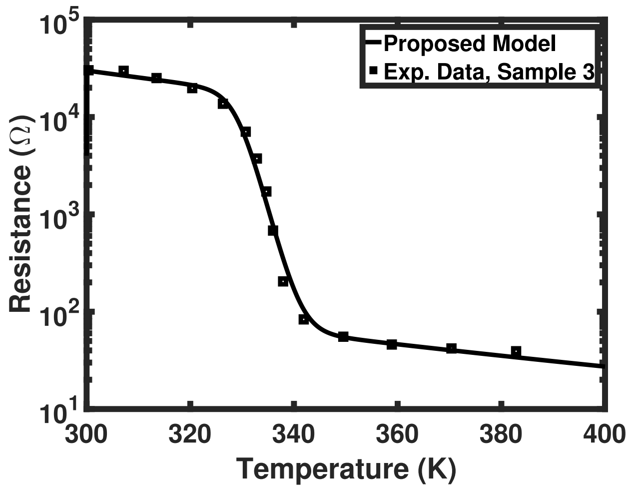

Fig. 3. Model fitting against experimental data.

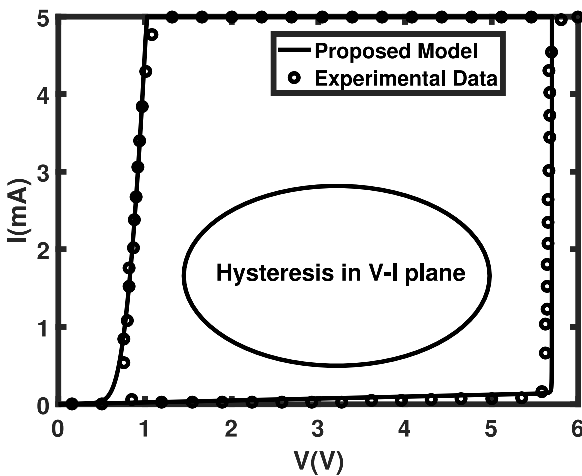

Fig. 4. Demonstration of device Hysteresis in the V-I plane which demonstrates the memristive dynamics of the IMT device.

levels, based on the values used from [5], were applied across the device: 1.4V, 1.6V and 1.8V. One can readily observe in Fig. 5 that the local temperature of the device saturates

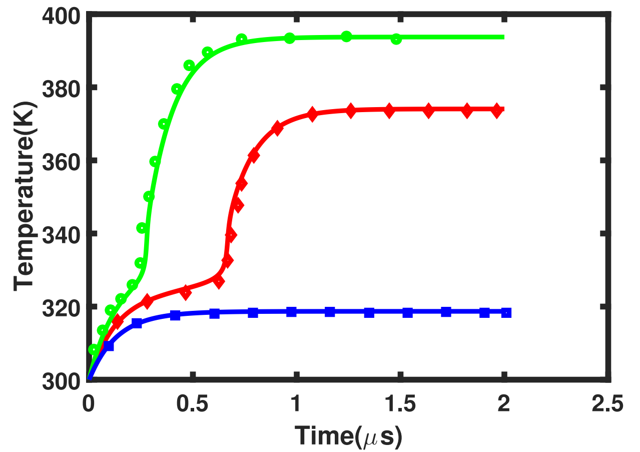

Fig. 5. Model (solid line) fitting against electro-thermal simulations (markers). Plotting the Device local temperature against time for three applied voltage values.

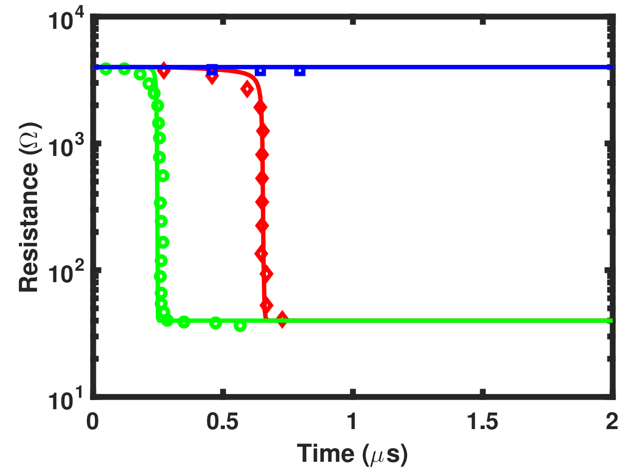

Fig. 6. Model (solid line) fitting against elector-thermal simulations (markers). Plotting the Device resistance against time for three applied voltage values.

at a higher temperature value for higher voltages due to increased Joule heating. In Fig. 6, higher voltages result in faster transition time due to faster rate of joule heating.

V. SIMULATION OF AN ARTIFICIAL NEURON USING IMT

This section showcases the utility of the proposed model in a SPICE level simulation framework. The proposed neuron circuit in [5] is simulated in Cadence environment using Spectre circuit simulator with the IMT model implemented in VerilogA.

A typical neuromorphic system consists of synapses and neurons. First, inputs to the synapse network are multiplied by their corresponding weights. In memristive neuromorphic systems, the weights are often represented by the conductance of a nonvolatile memristive device (typically, a transition metal oxide in most of state-of-the-art architectures), the inputs are the voltages across the device and the output, result of the multiplication, is the current flowing

through the device such that Ohm's law is leveraged for multiplication without the need for additional complex circuitry. The current through the synapses are then summed and fed to the neuron input. The neuron compares the inputs to a threshold and fires if the input signal exceeds the threshold. The neuron then remains idle for a period of time known as the refractory period wherein no fires can take place. A schematic of a neuromorphic system is presented in Fig. 7.

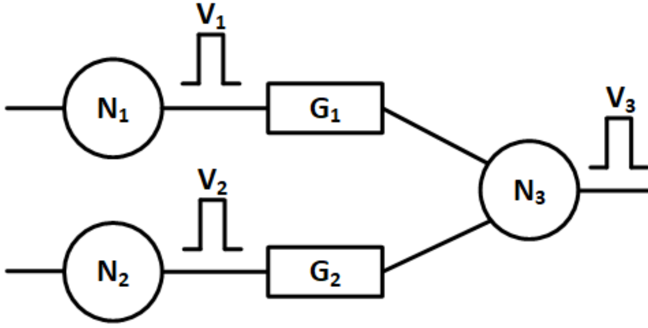

Fig. 7. Schematic of a neuromorphic system.

Here, since the aim is to validate the utility of the proposed IMT SPICE model, we replicate the circuit presented in [5]. The accumulated sum through the synaptic weight is represented by a current source feeding into a capacitor such that:

$$\Sigma I_{SYNAPSE} = \Sigma V_i G_i, \tag{5}$$

where V_i is the voltage spike generated by the *ith* input neuron and G_i is the conductance (weight) of the *ith* synaptic element. The core of the neuron is the IMT device which switches from R_{HRS} to R_{LRS} once the temperature exceeds T_c. Unlike conventional CMOS neurons, here the neuron's threshold is the device temperature, not a specified voltage value. Fig. 8 depicts the circuit under study.

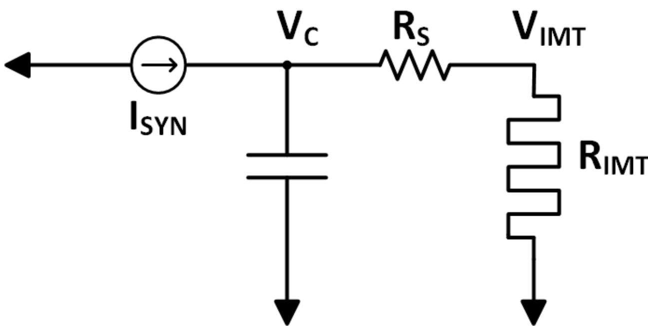

Fig. 8. Schematic of an IMT neuron Circuit.

Fig. 9 depicts the SPICE simulation of the circuit in Fig. 8. Current pulses were supplied through the capacitor to model voltage spikes multiplied by their corresponding weights. As time evolves, the voltage across the IMT V_{IMT} increases as well as the device temperature $T(t)$ due to Joule heating. Once the temperature hits T_c, the resistance of the IMT

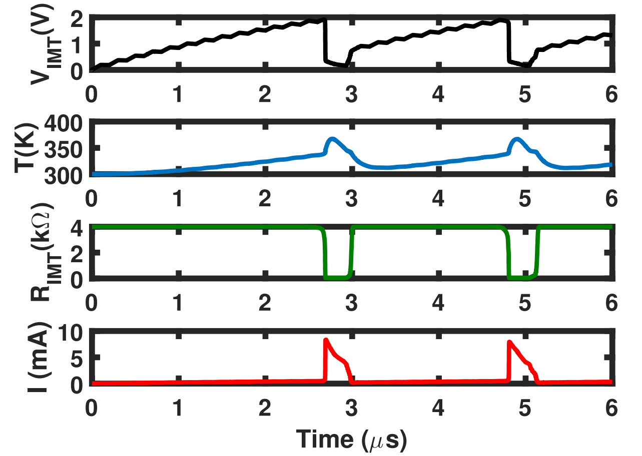

Fig. 9. Simulation of an IMT neuron using the proposed mode [5].

R_{IMT} switches to R_{LRS} and a current spike is generated. The system then remains idle for a period of time equal to the refractory period as shown in Fig. 9 where the capacitor does not accumulate voltage as long as the IMT is at R_{LRS}. After the device cools down, the resistance relaxes back to R_{HRS} and the capacitor starts to accumulate voltage while the device starts to heat up again. The obtained SPICE simulation results capture the neuron behavior shown in [5]. Table 1 depicts the device parameters used in the simulation of the circuit in Fig. 9. $R_{LRS/HRS}$ were extracted from the device geometry and resistivity based on $R = \rho.L/A$.

TABLE 1. IMT VerilogA model parameters for neuron circuit simulation.

Parameter	Symbol	Value
Thermal Resistance	$R_{th}(K/W)$	$41.6X10^3$
Thermal Capacitance	$C_{th}(J/K)$	$3.17X10^{-12}$
High Resistivity State	$\rho_h(\Omega.m)$	$1X10^{-3}$
Low Resistivity State	$\rho_l(\Omega.m)$	$1X10^{-5}$
Area	$A(m^2)$	$5X10^{-13}$
Width	$W(m)$	$2.5X10^{-6}$
Length	$L(m)$	$2X10^{-6}$
Ambient Temperature	$T_0(K)$	300
Series Resistance	$R_S(\Omega)$	200

VI. PROPOSED IMT-BASED IAF NEURON

The proposed neuron builds off the proposed circuit in [5]. First, the current source is replaced by a synaptic network. Second, an output stage is added in order to provide signal restoration as well as convert the current spike into voltage spike as the output of the neuron serves as an input to the following stages. Fig. 10 depicts the proposed design. Input pulses are fed into the synaptic network wherein each synaptic element is comprised of a nonvolatile memristive device to store the synaptic weight and a diode (a rectifying device) to prevent any back current. The proposed design functions in much the same way as the circuit in Fig. 8 until the current spike is generated. The current spike is then fed

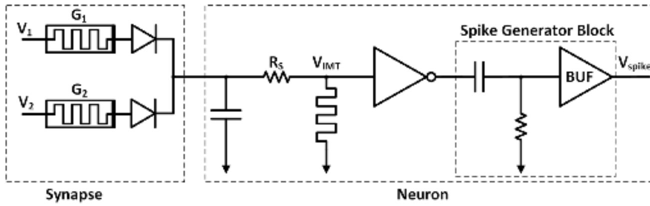

Fig. 10. Schematic of the proposed neuron circuit.

to an inverter to generate a voltage pulse. A spike generation circuit is then added to produce an output voltage spike with a pulse width controlled by the RC time constant of the RC network preceding the output buffer. Fig. 11 depicts the simulation of the proposed design.

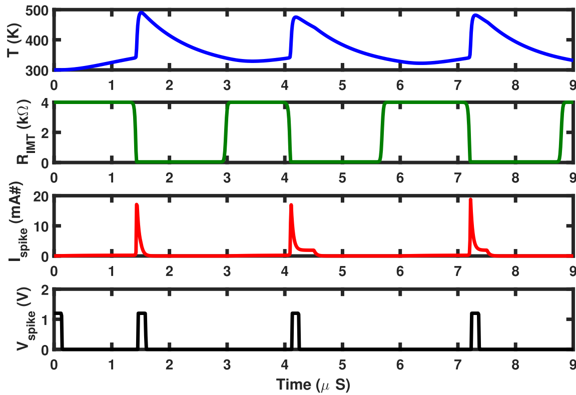

Fig. 11. Simulation of the proposed neuron.

It is important to understand the impact of the design parameters on the operation of the proposed neuron. The essence of neuron oscillation rests in the IMT device alternating between R_{HRS} and R_{LRS}. At R_{HRS}, the steady state temperature exceeds the critical temperature and, accordingly, the neuron fires. At R_{LRS}, the steady state temperature drops below the critical temperature, the neuron resets and the process is repeated for the next inputs.

At steady state ($\frac{dT}{dt} = 0$), the solution to the differential equation in (4) can be expressed as follows:

$$T_{ss} = T_0 + R_{th} I_{IMT}^2 R_{IMT}, \quad (6)$$

where T_{ss} is the steady state temperature of the IMT device. Hence, according to the aforementioned explanation, the oscillation condition can be expressed as follows:

$$R_{th}.I_{IMT}^2.R_{LRS} < T_c - T_0 < R_{th} I_{IMT}^2 R_{HRS}, \quad (7)$$

Inequality (7) establishes the oscillation condition for the IMT-based neuron as a function of device parameters such as R_{th}, R_{LRS}, R_{HRS} and T_c and circuit variables such as I_{IMT} which is a function of the amplitude of the voltage spike and the series resistance with the IMT device including the synapse resistance, diode ON resistance and the IMT series resistance. This oscillation is the essence of operation of the IAF neuron as shown in [6]. The relaxation oscillator is a typical circuit that exhibits oscillation which can be found in Appendix B.

The neuron typically operates in three phases: (I) accumulation wherein the inputs from the synapse networks are summed, (II) firing when the accumulated value reaches the neuron's threshold and (III) refractory period wherein the neuron is idle.

In CMOS neurons, an OPAMP is required for accumulation (Integrator) and another is required for comparison against the threshold (comparator). Also, a feedback circuitry is often needed to implement the refractory period. These OPAMPS, besides entailing all the complexities of analog design, are also area consuming and power hungry. For example, extra capacitors are often needed for stability purposes which usually consume significant area.

On the other hand, the IMT device can provide the accumulation function through the heating of the device, fire through device transition and a refractory period during device cooling should the device be placed in such configuration. One can readily see the advantages provided by the IMT device. A typical CMOS neuron, such as the work in [26], requires more than 20 transistors while the proposed IMT-based neuron only requires 7 transistors.

VII. DISCUSSIONS AND FUTURE PROSPECTS

Here the values used for R_{HRS} and R_{LRS} are both relatively low which also agree with the experimental results in [5]. It should be noted, however, that this represents a limitation on the fabrication of such devices. Higher R_{HRS} values might require a significantly long period of time until the device hits the T_c which might be practically unfeasible. This problem can be overcome, however, via increasing the value of the applied voltage. Yet, another limitation is that the applied voltage should remain within the practical bounds of standard CMOS processes.

These values may not be suitable, however, for memory application. In memory arrays, IMT devices are typically used as selector devices to circumvent sneak path currents. Hence, low R_{HRS} values might not effectively suppress those unwanted leakage currents. This prospect shows that R_{HRS}/R_{LRS} values might vary depending on the application.

Finally, as alluded to before, understanding the exact switching dynamics of IMT devices is still subject to further research and, accordingly, the models might require constant refinements. The compact model developed in this work is based on the most established understanding of the switching mechanism of IMT devices available in the literature. Also, the developed compact model was fitted against device models (TCAD-like models) wherein the same physical switching mechanism was considered but with simpler formulation to arrive at closed form expression which can be easily implemented in SPICE simulators. However, further studies of IMT switching dynamics might reveal new switching mechanisms and physics which will require adjustments to the models.

VIII. CONCLUSION

This work presented a SPICE compatible compact model for Insulator Metal Transition devices validated against

experimental data and electrothermal simulations from the literature. The proposed model describes the IMT device as a memristive system and captures the role of temperature and electric field in the resistive transition of the device. Using the proposed model, a simple neuron was designed and simulated in Spectre. Design expressions for the neuron's oscillation where derived. The results agree with the expected neuron behavior and published experimental data. Impact of device parameters on the system performance were also discussed and device requirements for efficient circuit operation were projected.

APPENDIX A
IMT MODEL PARAMETER EXTRACTION

In this section, we develop the parameter extraction procedure of the proposed model. We primarily focus on the resistance model and show how B_{HRS} and B_{LRS} are extracted. First, the simplified form of equation (3) is used in the extraction procedure, described in Section III, which can be expressed in the following form:

$$ln(R_{LRS}) = ln(R_{LRS_F}) - B_{LRS}(T(t) - T_F), \quad (8)$$

$$ln(R_{HRS}) = ln(R_{HRS_0}) - B_{HRS}(T(t) - T_0), \quad (9)$$

four data points are then used to extract the thermal coefficients (B_{HRS} and B_{LRS}) as shown in Fig. 12. The thermal coefficients can be expressed as follows:

$$B_{LRS} = \frac{ln(R_{LRS_F}) - ln(R_{LRS})}{T_2 - T_F}, \quad (10)$$

$$B_{HRS} = \frac{ln(R_{HRS_0}) - ln(R_{HRS})}{T_1 - T_0}, \quad (11)$$

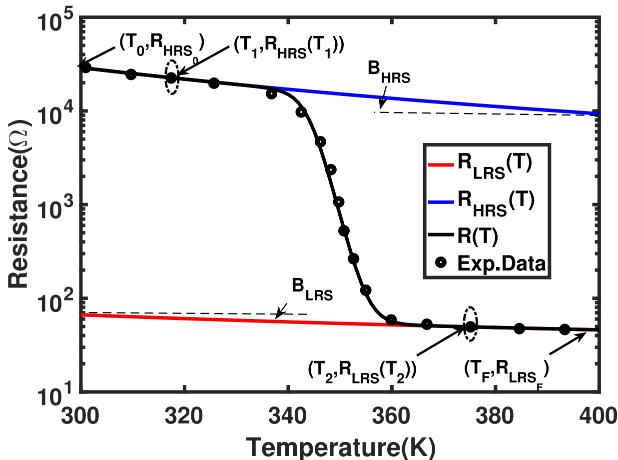

Fig. 12. Thermal coefficients extraction.

As alluded to before, the value chosen for A in this work is $A = 10^4$. The higher the value of A, the faster R_{HRS} and R_{LRS} saturate to R_{HRS_0} and R_{LRS_0} beyond T_0 and T_F, respectively.

APPENDIX B
RELAXATION OSCILLATOR DESIGN

Here we analyze an IMT-based relaxation oscillator and derive the Oscillation conditions. The relaxation oscillator is a simpler circuit than the proposed neuron with the same operation principle. Thus, analyzing this simple circuit may aid with the understanding of the proposed neuron circuit. Fig. 13 depicts the IMT-based relaxation oscillator proposed in [16].

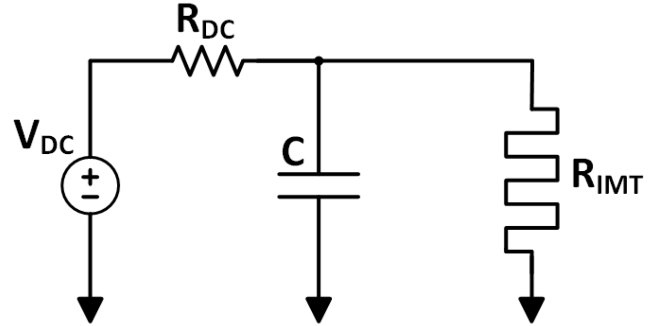

Fig. 13. Schematic of the relaxation oscillator.

A DC voltage is applied at the circuit's input. At steady state ($\frac{dT}{dt} = 0$), the solution to the differential equation in (4) can be expressed as follows:

$$T_{ss} = T_0 + R_{th} I_{IMT}^2 R_{IMT}, \quad (12)$$

where the current through the IMT device (at steady state) can be expressed as follows:

$$I_{IMT} = \frac{V_{DC}}{R_{DC} + R_{IMT}}, \quad (13)$$

To ensure oscillation:

$$T_{ss}(R_{LRS}) < T_c < T_{ss}(R_{HRS}), \quad (14)$$

Substituting (12) and (13) in (14):

$$\frac{R_{th} R_{LRS} V_{DC}^2}{(R_{LRS} + R_{DC})^2} < T_c - T_0 < \frac{R_{th} R_{HRS} V_{DC}^2}{(R_{HRS} + R_{DC})^2}, \quad (15)$$

Hence, one can readily see that given an IMT device with some arbitrary thermal resistance, high resistance state and low resistance state, circuit variables such as the applied DC voltage and the series resistance can impact the oscillation condition and, thus, should be carefully chosen.

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