

SPICE Simulations of Single Event Transients in Bipolar Analog Integrated Circuits using Public Information and Free Open Source Tools

F. J. Franco, C. Palomar, J. G. Izquierdo, and J. A. Agapito

Abstract—This paper proposes a technique to build SPICE micromodels of integrated circuits in bipolar technology appropriate to simulate single event transients. First of all, we will show how to obtain SPICE models of the internal transistors from texts in the scientific and academic literature. Next, several strategies to figure out the internal structure of the integrated circuits and bias point will be shown. Finally, simulation results will be compared to data issue from experiments, either performed by the authors or by other researchers. As the simulations do not require expensive software or hardware, this paper can be a start point for research groups with small budget or for academic purposes at universities.

Index Terms—Open-source tools, operational amplifiers, single event transients, SPICE, voltage comparators

I. INTRODUCTION

COMPUTER-AIDED simulation is an essential tool in the development of electronic circuits. Simulations allowed for the validation of a circuit and the exploration of new ideas without the need of building it, with obvious savings in work time and money. In the field of analog circuits, a lot of programs are able to accomplish this task (Qucs, GnuCap, AplaC, Verilog-AMS, A-VHDL, ...) but the most popular simulator is undoubtedly SPICE.

SPICE 3f5 was the last version released in 1993 by the University of Berkeley, the center where this software came to light. It was distributed by the University of Berkeley under its own permissive license, called Berkeley Software Distribution (BSD) license, that allowed the use of the source code for any purpose. In the following years, private companies adapted the original source code to build very powerful, but usually expensive, commercial versions (PSPice, HSPice, ...) for different operating systems and architectures. At the same time, the code was retaken by another project, called NGSpice [1], released with a modified BSD license. Another attractive project is Xyce [2], a SPICE clone rewritten from scratch at the Sandia Lab, released under the GNU General Public License (GPL). Finally, there are other closed-source but free-of-charge SPICE simulators such as Spice Opus [3], LTSpice

[4], etc. As they are compatible with the original SPICE 3f5, all the techniques shown in this paper can be adapted to these programs. However, we will focus mainly on NGSpice and, sometimes, instructions to implement the code in Xyce will be provided.

The area of electronics devoted to investigate the propagation of single event transients (SETs) also benefits from this procedure of work. However, a critical requirement is the need of simulating micromodels of integrated circuits (ICs) instead of macromodels. There are two strategies for developing blocks to emulate the behavior of an IC [5]. The first option is to build a *micromodel*, where every individual device inside the IC as well as the internal connections are depicted in detail. The second option is the *macromodel*, where ideal elements replace inaccessible internal blocks without changing the external circuitual behavior of the IC. This option has the advantage of speeding up simulations. However, as the SETs originate inside the IC, it is mandatory to use micromodels in spite of the drawbacks: Slower simulations, lack of information about the internal structure due to the manufacturer's policy, etc.

The difficulty in obtaining SPICE micromodels has made some authors to investigate alternative approaches. For instance, the LM124 operational amplifier (op amp) was successfully modeled using Laplace blocks with characteristics that depended on external measurable parameters [6]. This strategy led to achievements such as the prediction of the synergistic effects of the accumulated radiation damage and the SETs or ATREEs (Analog Transient Radiation Effects on Electronics) [7]–[10]. Besides, a behavioral model of the LM124 was developed to study its degradation due to total ionizing dose (TID) [11]. However, as SPICE is the “de facto” standard simulator in a great deal of fields in electronics, we feel that it is appropriate not to leave this line and to propose a technique to develop generalist micromodels of ICs. The required information will be drawn from public sources such as datasheets, textbooks, typical knowledge of electronic engineers, and scientific journals. Thus, anyone can recreate the models shown in this work and develop new ones independently of the economic framework.

Before starting the main part of paper, we consider that it is important to make clear the situations in which these SPICE models are useful. First of all, the models must not be used to predict the size of SETs in proportion to the deposited charge. The models are just approximations of the actual ICs, not accurate representations. The models can be used instead

This work was supported in part by the MCINN projects AYA2009-13300-C03-03 and Consolider SAUUL CSD2007-00013, by MCINN Grant CTQ2008-02578/BQU, and by UCM-BSCH.

Francisco J. Franco, Carlos Palomar, and Juan A. Agapito are with the Departamento de Física Aplicada III, Facultad de Físicas, Universidad Complutense de Madrid (UCM), 28040 Madrid (Spain) (e-mail: fjfranco, carlos.palomar, agapito@fis.ucm.es).

Jesús G. Izquierdo is with Centro de Láseres Ultrarrápidos, CLUR, Facultad de Químicas, Universidad Complutense de Madrid (UCM), 28040 Madrid (Spain) (e-mail: jegonzal@quim.ucm.es).

in the evaluation of the way that SETs propagate in the system where the IC works. Thus, one can roughly predict how the SET changes when the topology, external parameters, etc. do. Finally, the models are interesting tools to make preliminary deductions concerning the effects of accumulated radiation damage in the ICs, and also in the more complex networks where ICs such as op amps are included.

This work is structured as follows: First, we will explain the procedure to obtain realistic SPICE models of the basic devices present in bipolar ICs along with the method to generate transients. Next, we will explain how to create netlists depicting the ICs. Finally, we will compare simulations with experimental results obtained by the authors and, later, with some experiments performed by independent authors.

II. MODELS OF BASIC DEVICES

A. Transistor Models

1) *Bipolar Junction Transistors (BJTs)* : In previous works, some researchers decapsulated the IC, insulated every individual transistor by means of an ion microbeam, and, afterward, inserted microprobes in the transistor terminals to measure its SPICE parameters. Thus, an accurate SPICE micromodel of the IC could be obtained [12]. Unfortunately, this choice is at the disposal of only some research groups. Another option is to measure the transistor sizes from zoomed pictures of the decapsulated IC to fit the intrinsic capacities until the output of the simulations was identical to the actual one obtained, e. g., in laser experiments [13].

In this work, we propose to build the SPICE micromodels without physical access to the internal structure of ICs. Unlike CMOS technologies, which count on the data freely provided by MOSIS [14], we are not aware of an equivalent website offering SPICE models of integrated BJTs. A choice consists in using models of discrete transistors, such as the 2N2222A (npn) or the 2N2907 (pnp). However, this idea must be discarded due to two reasons: First, these transistors are very large, with huge parasitic capacitances, and, in consequence, the simulated IC may become unstable and oscillate (E. g., $C_{JC} = 7 \text{ pF}$, $C_{JE} = 22 \text{ pF}$ in the 2N2222A, two orders of magnitude above the data in Table II). Second, these are discrete transistors, with only three terminals. In ICs, it is important to take into account the fourth terminal (bulk), available in most versions derived from SPICE 3f5.

The solution adopted in this work consists in developing transistor models from the academic literature. The role of the SPICE parameters is public and can be found in different documents (e. g., on the University of Berkeley itself [15], or in the NGSPICE handbook [1]). Values of some parameter are well-known, such as the gap of the silicon forbidden band ($E_G = 1.12 \text{ eV}$, EG) and the nominal temperature of work ($T_{NOM} = 27^\circ \text{C}$, TNOM). Other parameters are purely geometric, such as SUBS, used by some SPICE flavors such as NGSpice or Spice Opus to make a distinction between lateral and vertical transistors, and the scaling factor, AREA, which modifies parameters depending on the transistor surface, such as ISX, CJX, RX, etc., while leaving other parameter such as BF, EG, VAF, ... unaffected. We postulated that the diffusion

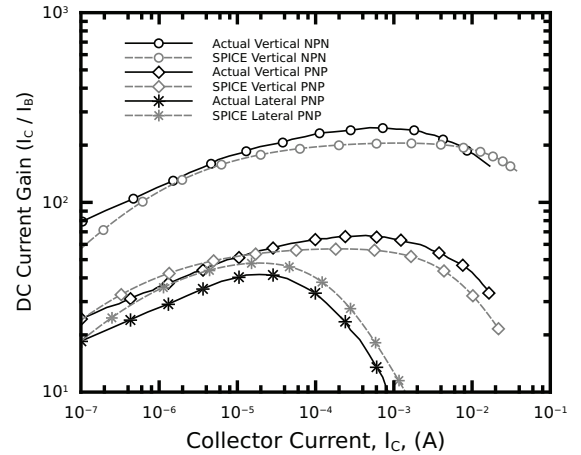


Figure 1. Comparison of h_{FE} vs I_C in actual and simulated BJTs. The characteristics of the actual transistors were obtained from Fig. 2.38 of [16] whereas the simulations were performed with the models depicted in Tables I-II, with $|V_{CE}| = 10 \text{ V}$.

Table I
SPICE PARAMETERS, COMMON TO ALL OF THE BJT MODELS.

Param.	Value	Param.	Value	Param.	Value
LEVEL	2	MJC	0.5	EG	1.11
NF	1	CJS	1p	TNOM	27
NE	2	VJS	0.52	NKF	0.5
NR	1	MJS	0.5		

as well as the generation-recombination currents were ideal. Therefore, $NF=NR=1$, and $NE=2$. The rest of parameters were obtained from data available in [16], a popular textbook to teach electronics. In particular, there are tables inside that depict the properties of the $5 \Omega\text{-cm}$, $17 \mu\text{-epi}$ & 44 V bipolar transistors, either lateral or vertical. A great deal of the physical properties can be directly extrapolated to SPICE parameters ($\beta_F \rightarrow \beta_{BF}$, $V_{AF} \rightarrow V_{VAF}$, ...).

However, these tables do not provide information about the gain degradation at very low or very high collector currents. At very low currents, this phenomenon is controlled by a parameter called ISE , which corresponds to the inverse saturation current of the generation-recombination component (related to NE). The other phenomenon, caused by the high injection effects, is controlled by IKF . In order to find out these important parameters, we tried to obtain $(I_C, \frac{I_C}{I_B})$ -curves to be compared with the equivalent graphs present in Fig. 2.38 of [16]. Both parameters were trimmed until the theoretical and actual curves were alike, as shown in Fig. 1.

Issued parameters, ready to be used in simulations, are shown in Tables I-II. They are expressed in the international system of units but written in SPICE-compatible format.

Unlike NPN transistors, usually vertical, it is difficult to know the geometry of a PNP transistor. If the IC is an old model, we can suppose that every PNP transistor is lateral except those with the collector connected to the negative power supply. This rule was used years ago to minimize the number of steps required to build an IC.

Unfortunately, there is no information about the dependence of the BJTs on the temperature, controlled by XTI , and XTB in

Table II
SPECIFIC SPICE BJT PARAMETERS

Parameter	NPN Vertical	PNP Vertical	PNP Lateral
SUBS	1	1	-1
IS	5f	10f	2f
BF	200	50	50
VA	130	50	50
ISE	0.3p	0.9p	0.6p
BR	2	4	4
VAR	130	50	50
RB	200	150	300
RE	2	2	10
RC	200	50	100
CJE	0.33p	0.17p	0.1p
VJE	0.7	0.55	0.55
MJE	0.33	0.5	0.5
CJC	0.1p	0.67p	0.33p
VJC	0.55	0.52	0.55
TF	0.35n	20n	30n
TR	400n	2u	3u
IKF	100m	10m	0.2m
ISS	5f	10f	2f

Table III
SPICE PARAMETERS OF IMPLANTED AND DIFFUSED JFETs.

Parameter	Imp.	Dif.	Parameter	Imp.	Dif.
LEVEL	1	1	CGS	2p	2p
VTO	±1	±2	CGD	0.5p	0.5p
BETA	300u	125u	PB	0.5	0.7
LAMBDA	0.01	0.01	FC	0.5	0.7
RD	50/2	50/2	IS	0.1n	0.1n
RS	50/2	50/2	TNOM	27	27

SPICE 3f5 and derived SPICE flavors. These two parameters are combined with EG and TNOM to predict the values of ISX, CJX, BF, etc. No information was found in the literature so only default values (XTI=3, XTB=0) can be used to model the BJT characteristics at values different than room temperature.

2) *Field effect transistors*: Junction field effect transistors (JFETs) are still found in bipolar analog ICs working as the core of current sources or in differential pairs inside some high-impedance input stages. However, its popularity has fallen during last years and it is difficult to find realistic models in literature. In our case, we had to use old editions of [16] to gather useful values. Table III shows parameters obtained from the third edition of the book by Gray *et al.* There are two kinds of transistors: implanted and diffused, similar from the simulation's point of view. It will be accepted that n-channel transistors share the parameters with the p-channel ones, with the exception of the pinchoff-voltage, which becomes negative.

3) *Other devices*: Passive devices such as resistors and capacitors were supposed to be ideal. Diodes were built from NPN transistors with shorted base and collector terminals. The dependence of the resistors on the temperature depends on the way of building (diffusion, polysilicon, etc.), usually unknown.

B. Current injection and generation of transients

Charge deposition by ions were simulated with current sources between the N and P zones of reverse-biased PN junctions. As BJTs usually work in forward-active zone, most of the current sources are in the base-collector junctions (Fig.

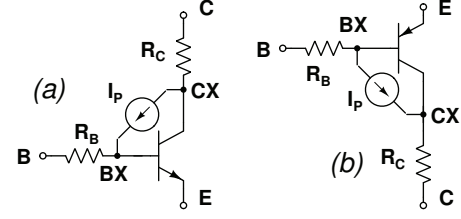


Figure 2. Method to place the current source to emulate a transient in NPN (a) and PNP (b) transistors. In SPICE, the double-exponential source is just `IQXX nodeA nodeB dc 0 EXP(0 {QT/(TAUF-TAUR)}) {TDTRANS} {TAUR} {TDTRANS} {TAUF}`.

2). Besides, in lateral PNP transistors, current transients can appear also between base and bulk and, in vertical NPNs, between collector and bulk. These are the only kinds of SETs that can be simulated with the technique proposed in the paper. To model the current source in SPICE, the following rules must be accomplished:

1) *DC value*: DC value must be 0 A.

2) *Role of parasitic resistances*: In previous works [17], it was found that the simulation of SETs was more realistic when the current source used the true base and collector nodes, beyond the parasitic resistors, instead of the usual terminals. Thus, the needed charge to generate a transient was closer to reality. Therefore, every transistor where a transient originates must be redesigned as a subcircuit (Fig. 2). In this subcircuit, the core is a BJT with null parasitic collector and base resistances, a current source and the parasitic resistances that connect the transistor with the rest of the circuit. The values of the resistors, R_B and R_C , can be found in Table II and must be divided by AREA if it is different than 1. That means that every BJT SPICE model (vnnpn, vnpnp and lpnp) has a corresponding twin model without parasitic resistances (vnnpn_nr, vnpnp_nr and lpnp_nr). In practice, in these new models, the value of R_B and R_C is 1m ($10^{-3} \Omega$) in order to make the convergence easier as suggested in [17].

3) *Use of double-exponential function*: Some works have put in evidence that the output of an IC depends on the shape of initial current pulse even though the response time of the devices and the IC itself are much higher than the duration of the current pulse [18]. Therefore, the current pulse must be simulated with a realistic source, such as the double exponential function:

$$I(t) = \frac{Q_T}{\tau_F - \tau_R} \cdot \left(e^{-\frac{t-T_D}{\tau_F}} - e^{-\frac{t-T_D}{\tau_R}} \right) \quad (1)$$

Q_T being the total deposited charge, τ_R and τ_F the rise and fall characteristic times, and T_D the time at which the transient occurs. In practice, only the total charge and the falling time are necessary [19]. From the data and conclusions in [19], we will postulate that the fall time, τ_F , is 250 ps and that τ_R is a fifth of τ_F . Thus, the pulse is not longer than 1 ns. However, the use of the double-exponential model brings an important setback to the simulations. Typically, transients are studied in SPICE with a sentence similar to `TRAN TSTEP TSTOP TSTART TMAX uic`. Its meaning is: Simulate a transient (TRAN) from 0 s on, using the initial conditions (uic), with a

time step between stored data equal to T_{STEP} , exiting when the time is T_{STOP} , and saving data only from T_{START} onwards. T_{MAX} is the highest allowed time step used by the simulator when solving the system with standard numerical algorithms. If T_{MAX} is provided by the user, some simulators replace T_{STEP} by T_{MAX} . The problem comes from the fact that sometimes the duration of a typical transient observed in the IC output is on the order of 10-100 μs meanwhile the current pulse duration is on the order of 1 ns. That means that the simulation step must be on the order of 10 ps to sample accurately the current pulse (Thus, the current source is sampled 100 times). In consequence, the total number of dots is on the order of 10^6 - 10^7 . Let us remember that a “dot” is actually an array with the voltage value of every node of the circuit as well as the current values in the voltage sources in floating point format. Sometimes, we came across with the fact that the personal computer runs out of memory leading to a simulation crash¹. On the contrary, if T_{STEP} is too large, the simulator can complete the simulation without detecting the existence of a current source with a value different than 0 only for a few tens of nanoseconds. We solved this problem using a “dummy” voltage source. The current pulse is modeled as a double-exponential source but, somewhere in the netlist, one must include a dummy Piece-Wise Linear (PWL) voltage source connected to a dummy load resistor. The value of the PWL voltage source is 0 V until the true transient starts (Fig. 3). Defining very close time values in the dummy voltage source, we force the simulator to recalculate the whole circuit in very close time steps. Once we consider the current pulse is over, the dummy voltage source does not change anymore and the simulator evaluates the system every T_{STEP} s. Thus, the system does not exit with errors and the computation time is dramatically reduced.

III. BUILDING THE MICROMODEL TOPOLOGIES

In spite of the fact that there are ICs fully depicted in the academic literature, such as the uA741 [20], NE5234 [16], LH0062, and uA760 [21], it is difficult to find accurate information about most of the ICs used in electronic systems working in radiation environments.

The first step is to find the datasheet of the IC to simulate. Sometimes, it is useful to visit the websites of several manufacturers. Thus, the LM311 voltage comparator is sold by Texas Instruments [22] and by Fairchild Semiconductors [23] but the former document is more detailed than the latter since it provides the values of some important internal resistors.

Surprisingly, this strategy is successful in some cases without any kind of additional step. An example is the LM119 voltage comparator [24], for which the internal structure provided by the manufacturer works using the transistor models depicted in Section II-A1. The only modification consisted in increasing the surface of the output transistor, called Q16 in the manufacturer’s datasheet, up to a relative area of 100. Thus, we obtained output LOW logic levels near 0 V even when the

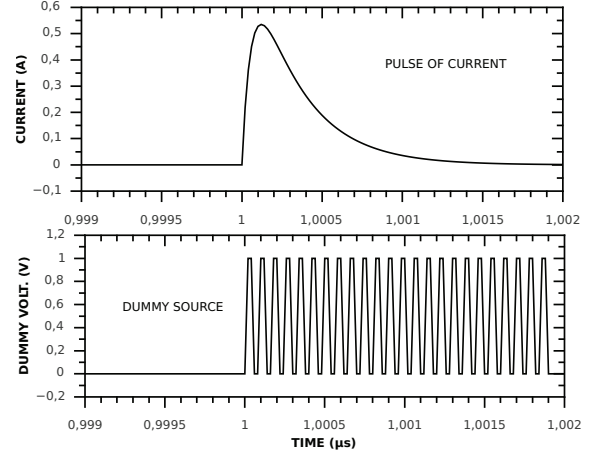


Figure 3. Dummy voltage source to compute the double-exponential current source. The presence of the PWL voltage source forces the simulator to recalculate the system state every time the dummy voltage source is defined. Thus, a double-exponential source (above) is computed every 20 ps due to the presence of the PWL signal (beneath). When this source returns to a constant value, the circuit evolution is computed every T_{STEP} s.

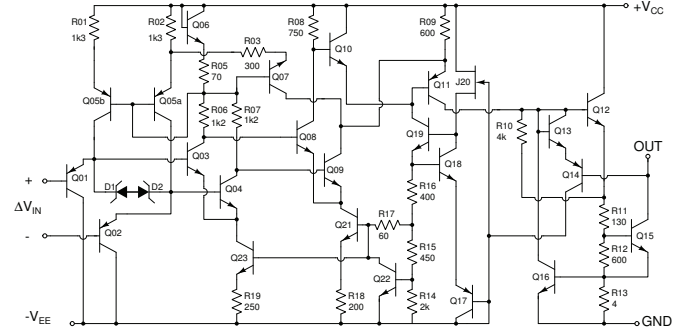


Figure 4. Internal structure of the LM111/LM311 according to its manufacturer [22].

pull-up resistor was on the order of 1 k Ω . However arbitrary this decision may be, it must be taken into account that the manufacturers do build huge output transistors in this kind of voltage comparators as it can be seen in microphotographs [25]. Finally, the transistors liable to trigger an SET were found in the related literature [26].

Another interesting IC, the LM139, was built from an application note distributed by the manufacturer [27], not from the datasheet.

In other cases, such as the LM111 comparator [22], the implementation from the datasheet (Fig. 4) did not work. Op amps and voltage comparators are ICs that usually have three stages: A differential pair at the input stage, the gain stage and the output. Very often, these stages are biased by current sources the value of which must be known in order to perform SPICE simulations. The solution to the LM111 problem was found in the literature. This comparator was invented in the 70’s by R. Widlar, one of the forefathers of the analog electronics, who left us a couple of works where this comparator was thoroughly explained [28], [29]. This information was used to trim the SPICE micromodel. In the LM111 structure, the primary current source was based in

¹Typically, our simulations were performed on a PC with a 4-core Intel Xeon processor, 8-Gb RAM, working at 3.39 GHz, and running Ubuntu GNU/Linux 14.04 64 bits.

a JFET (J20 in Fig. 4). This transistor was modeled as a diffused n-channel JFET ($V_{TO} = -2$) with a relative area of 1.2. Thus, the output of the current source was $6 \mu A$ with $\pm 15 V$ power supplies. Later, we made several trial-and-error tests until realizing that when the Q06 area was 2, the comparator worked as wished. Just like the LM119, the area of the output transistor, Q15, was set to 190 to obtain hard logic LOW output levels even when the $1\text{-k}\Omega$ pull-up resistors and to emulate transients observed in laser tests [30].

Sometimes, it is necessary to turn to the elementary knowledge of analog electronics. For instance, the current source biasing the input stage of an op amp or voltage comparator can be calculated from the input bias current, I_B . It is not difficult to demonstrate that, if the differential pair is bipolar without improvements, $I_B = \frac{1}{2} \cdot \frac{I_Q}{\beta_F}$. Given that I_B appears in the IC datasheet and β_F can be found in Table II, I_Q can be directly calculated. A better trick is that of the slew rate (SR), parameter that appears in the op amps datasheets. It is well-known that $SR = \frac{I_Q}{C_C}$, C_C being the stabilization capacitor between the input and output of the gain stage. Therefore, knowing I_Q , C_C is immediately obtained and vice versa.

Nevertheless, sometimes the solution is more difficult to find. An example is the LM6181 [31], a current-feedback op amp. According to the manufacturer, the internal structure is very simple but it is mandatory to know the value of two twin current sources, called I_O , present in the input stage. The strategy to find out its value was the following. It is possible to demonstrate that, in this structure, the impedance of the non-inverting input is $Z_{IN} \approx \frac{1}{2} \beta_{FN} \cdot \beta_{FP} \cdot \frac{V_T}{I_O}$, with $V_T = 0.026 V$. As the manufacturer claims that this impedance is $10 M\Omega$, it is immediately deduced that $I_O \sim 13 \mu A$. Using this value, it was possible to build a SPICE micromodel where SETs were spikes, positive or negative, with a duration of some tens of nanosecond, quite similar to those reported in [32].

However, the most productive SPICE micromodel from the scientific point of view is that of the LM124A, a popular op amp [36]. The datasheet distributed by the manufacturer provides useful information, such as the values of the internal current sources. From the value of the slew rate ($0.5 V/\mu s$) and the current source biasing the input stage ($6 \mu A$), it is deduced that the value of the stabilization capacitor, C_C , is $12 pF$. But little additional information can be obtained. Fortunately, there are previous works where the internal LM124A structure was depicted. In particular, we will focus on the work done by Savage *et al.* in 2002 [33]. Following the schematics therein (Fig. 5(a)), an LM124A SPICE micromodel was developed. Nevertheless, three corrections were necessary.

First, the primary current source depicted by Savage *et al.* seemed not to work in the SPICE simulations. Therefore, we used an older work by other authors [35], which showed a source with less devices and very easy to implement in SPICE (Fig. 5(b)). Using the transistor models depicted in Section II-A1 and II-A2, making $R_3 = 1.5 k\Omega$ and $R_4 = 2.4 k\Omega$ and the area of Q01 equal to 2, we obtained a $9\text{-}\mu A$ current sink. The second correction was that we observed a possible mistake in the schematic in [33], concerning the node where the Q16A collector was connected. The schematic was compared to that in [35] and the topology corrected. The third correction is

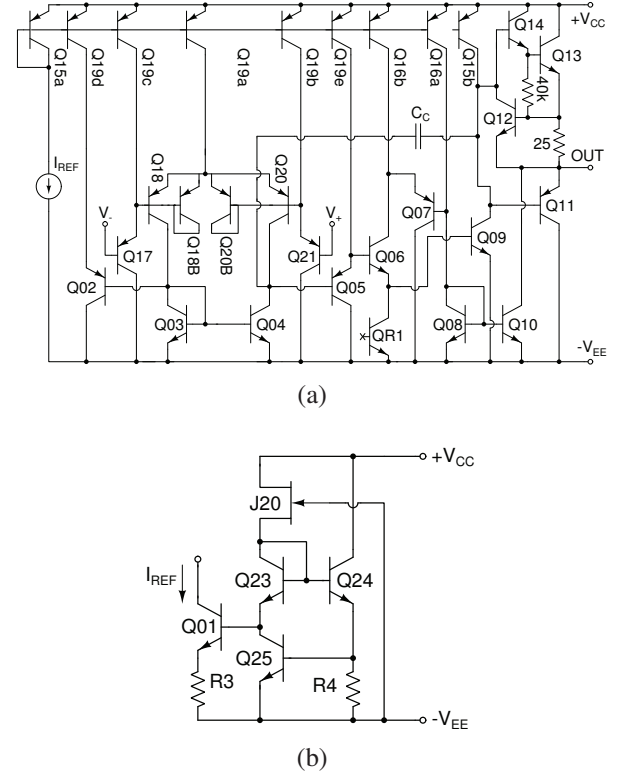


Figure 5. The LM124A. (a) Model based on the work by Savage *et al.* [33]. Q18B and Q20B are not present in this work but are present in some recent versions [34] (b) Primary current source depicted by Bonora *et al.* [35].

related to the input stage. The LM124 is a 40-years-old device and the layouts have diverged depending on the manufacturer. Slightly different versions can be found in the literature, with additional PNPs in the input differential pair (e. g., in common-collector configuration [7]–[10], [37], [38] or with shorted base and collector [34], [39], [40]). We decided to add two additional transistors, Q18B and Q20B, with shorted base and collector, to simulate a newer LM124A version.

Afterward, the transistors in the current mirrors were fitted to obtain the currents shown in the datasheet. Finally, the areas of some transistors were modified to couple the internal stages and to make the output short circuit currents about $30\text{--}40 mA$. Thus, we obtained a fully functional SPICE micromodel of the LM124A where SETs reported in the literature were obtained. With the purpose of making possible the recreation of the SPICE micromodel, Table IV shows the relative areas of the transistors. The rest of them are supposed to have a relative area of 1. A final correction was done in the C_C value. Theoretically, the SR value was $0.5 V/\mu s$. However, the SPICE simulations showed that I_Q/C_C overestimates the actual SR value, which was $0.32 V/\mu s$ in the simulations. In consequence, C_C was set to $9 pF$ to obtain an average SR value closer to $0.5 V/\mu s$.

Table V compares the values of the calculated DC & AC parameters with the LM124A SPICE micromodel to those found in the Texas Instruments' datasheet. Most of the values are on the same order and the discrepancies, such as the input offset current or the open loop gain, are explained by the fact that, in the simulations, BJTs are perfectly matched.

Table IV
RELATIVE AREAS OF TRANSISTORS IN THE LM124A MICROMODEL,
SHOWN IN FIG. 5.

Transistor	Area	Transistor	Area	Transistor	Area
Q01	2	Q15B	15	Q19B	0.6
Q10	1.25	Q16A	4	Q19C	0.6
Q11	0.5	Q16B	3	Q19D	0.6
Q15A	1	Q19A	1.1	Q19E	0.6

Table V
COMPARISON OF ELECTRICAL PARAMETERS OF THE ACTUAL LM124A
AND ITS SPICE MICROMODEL.

Parameter	Datasheet	SPICE	Units
Input offset Voltage	± 3	-0.55	mV
Power supply Rej. Ratio	65-100	107	dB
Input bias current	-20 \rightarrow -100	-99	nA
Input offset current	2	0	nA
Quiescent current ($\times 4$)	1.4 \rightarrow 2.3	1.36	mA
Short circuit current	± 40	± 35	mA
Open loop gain	100	965	V/mV
Gain-bandwidth product	1.2	1.03	MHz
Slew rate (rising)	0.5	0.39	V/ μ s
Slew rate (falling)	-0.5	-0.59	V/ μ s
Sat. volt. swing	1.5 / -0.02	1.1 / -0.02	V

The transistors where SETs can appear were identified from other works, which show sensitive zones and the shape of the transients [39].

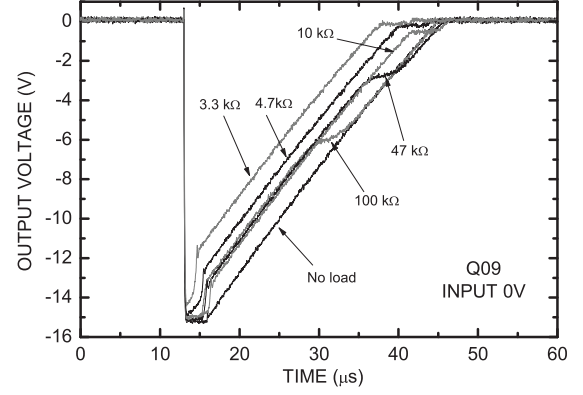
Using this method, we succeeded in building micromodels associated with the following ICs:

- 1) Op amps: LM124, μ A741, LF356, LH0042, LM725
- 2) Current-feedback op amps: LM6181
- 3) Voltage comparators: LM111, LM119, and LM139

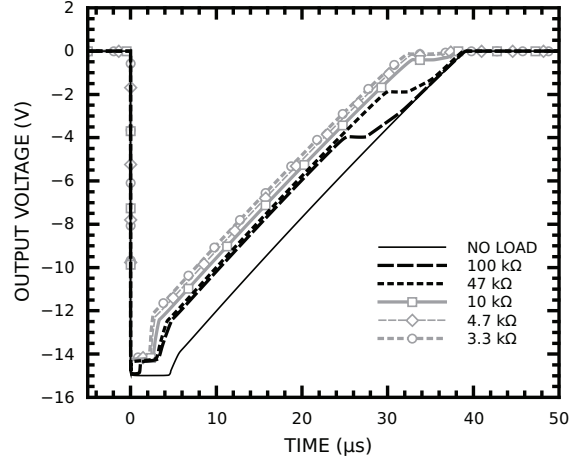
Finally, we consider important to highlight that our preferred simulation tool is NGSpice v. 26 [1]. All of the considerations reported in the previous sections were deduced from simulation in this tool. Another interesting option is the Xyce project [2], supported by Sandia Lab., although there is an important difference between them. Both are based in Spice 3f5, in which the LEVEL=1 of the BJTs admits a fourth terminal, the bulk. However, NGSpice innovated with the development of LEVEL=2, with two additional parameters, SUBS to indicate if the transistor is vertical or lateral, and ISS to compute the DC leakage current from collector (or base) to bulk. Therefore, if the simulations are performed with Xyce, LEVEL must be redefined to 1 and SUBS and ISS parameters must be removed from the code describing the transistors. The authors have verified that Xyce shows similar results in the simulations of SETs. Besides, nothing avoids to use the SPICE micromodels in other free SPICE flavors such as SPICE Opus, LTSpice, etc., but this choice has not been explored by the authors.

IV. RESULTS AND PREDICTIONS

The SPICE micromodels built with the technique depicted in the previous section has been used by the authors since 2009 to investigate SETs in analog ICs. In particular, they were used to understand the influence of the load resistors in the shape of the transients [30], [41] and to investigate the long duration pulses observed in linear voltage regulators, either series or shunt [42]–[44], due to peak detector effect.



(a)



(b)

Figure 6. Transients in the Q09 transistor of a LM124A working as a voltage follower depending on the load resistor. Actual transients in the laser facility (a) and simulation (b) [41].

Very often, strange phenomena were observed first in the simulations and verified later in a laser facility (e.g., the peak detector effect in shunt voltage regulators [43]).

Some examples of the published results are the following: Fig. 6(a) shows actual transients obtained when the Q09 transistor of an LM124 working as a voltage follower was illuminated with a pulsed laser. The shape of the transients depended on the load resistor. The second graph (Fig. 6(b)) shows the output of a simulated op amp inside the same electric network. One can see that both graphs are alike. Fig. 7(a) shows examples of actual transients in the LM111 voltage comparator as the value of the pull-up resistor increases. Fig. 7(b) shows the result of the SPICE simulations. Even though there are evident discrepancies between the experiments and the simulations (E. g., in the simulations SETs are shorter and the duration constant), other details are observed in both graphs: The higher the pull-up resistor, the smaller the transient peak, fact that leads to the SET disappearance if the pull-up resistor is large enough. Also, both graphs show a first stage where the output voltage becomes negative despite the logic power supplies being between 0-5 V.

It is important to indicate that the simulations shown in

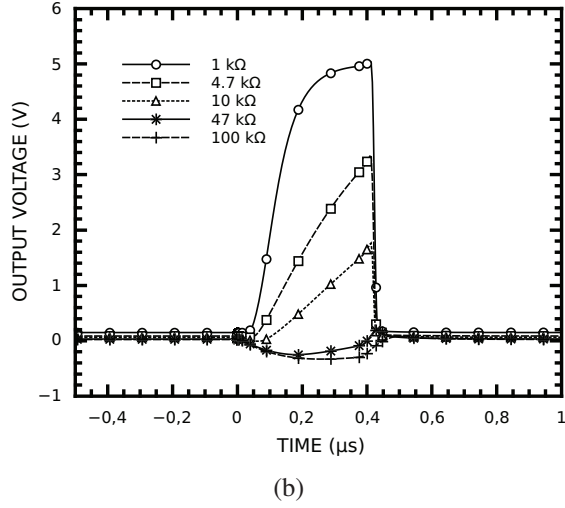
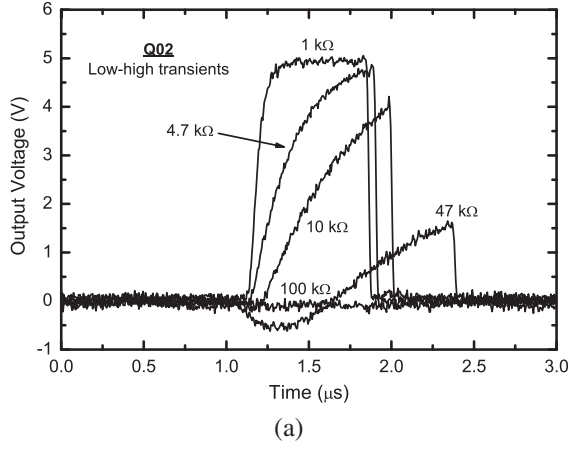


Figure 7. LOW-HIGH transients in the LM111 as a function of the pull-up resistor value. Actual transients in the laser tests (a) and simulations (b) [30].

the present manuscript are not those originally published. The reason is that there have been improvements in the models since the publication of the results: Incorporation of the bulk terminal, use of the double-exponential current source, etc., which allowed a better recreation of the transients. One can find the old simulations in [30], [41] and observe how the ongoing improvement of the models makes the simulations closer to the experimental results.

An interesting test to verify the applicability of the micro-models consists in recreating results obtained by independent research teams. Most of the tests are based on the LM124A, since op amps are more versatile than comparators.

In 2002, Sternberg *et al.* investigated how the feedback network of an op amp modified the shape of the transients [45]. Thus, the authors drew the following conclusions from experiments on the typical inverting network, with $G = -\frac{R_A}{R_B}$: First of all, the transient peak hardly depends on the values of R_A and R_B unless the resistor values are very low. Secondly, the transient is shorter if a) the value of R_B decreases with fixed gain, G ; b) $|G|$ decreases with fixed $R_T = R_A + R_B$. This behavior was corroborated by simulations. In particular, Fig. 8 validates the second conclusion.

In recent years, there has been a growing interest to in-

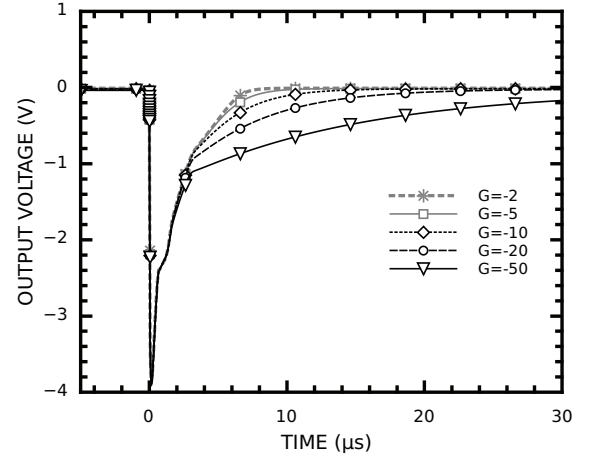


Figure 8. LM124A response with inverting configuration with transients originating in Q09 which shows the dependence on the gain value, G , with fixed $R_A + R_B = 100 \text{ k}\Omega$. This graph is related to Fig. 11 in [45].

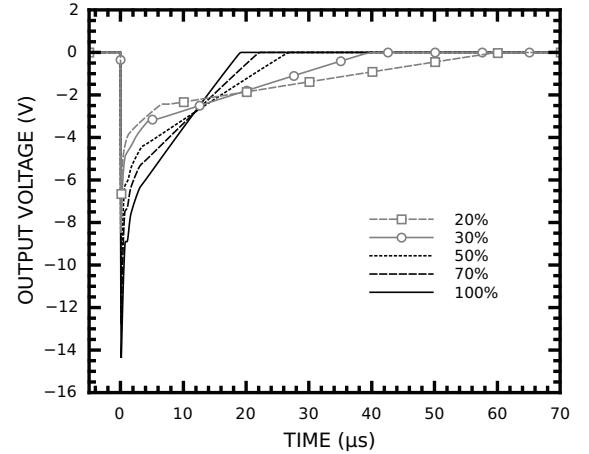


Figure 9. Evolution of transients originating in Q09 in a LM124A working as a voltage follower as β_F decreases. This graph can be compared to, e.g., Fig. 5(a) in [8] or Fig. 3 of [40].

vestigate how the accumulated radiation damage affects the transient shape. For example, it has been reported that the transients in the LM124A have a smaller peak as the radiation damage increases but the transients become longer [6], [8], [9]. The reason is the decrease of the slew rate value following the degradation of the mirror biasing the input stage. Similar predictions can be done with our SPICE micromodel. The degradation of the internal devices depends on the kind of radiation but can be roughly modeled as a steady decrease of the transistor current gain, β_F . This idea was used to perform the simulation shown in Fig. 9. For simplicity, we accepted that the degradation was identical in all the transistors independently of their nature. The op amp works even when the transistor gain is 20% of the initial value but transients become really long, as reported by other authors.

SPICE simulations show an equivalent effect in pristine ICs if $+V_{CC}$ and $-V_{EE}$, the power supply values, decrease. In other words, the recovery is faster with high values of $+V_{CC}$ and $-V_{EE}$ after injecting identical values of charge. This is

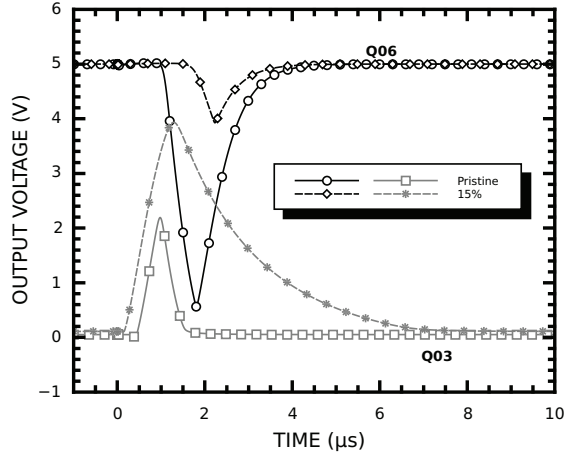


Figure 10. Evolution of the transients originating in two specific transistors, Q03 and Q06, of the LM139 voltage comparator as β_F decreases. Equivalent actual transients can be found in Figs. 9 & 11 of [46].

related to the Early effect in the transistor of the mirror biasing the input stage. As I_Q increases with $+V_{CC}$ & $|-V_{EE}|$, the slow rate also does.

There are also works investigating the effects of accumulated damage on the SETs in voltage comparators. SPICE simulations showed identical behavior to that reported by other authors [46]. In Fig. 10, we can see how two kinds of transients originating in different transistors change from pristine devices to those with only 15% of the initial β_F value. This behavior is in concordance with the results reported in [46]. An interesting effect shown by simulations and to be verified in experiments is the increasing delay between the injection of charge and the output transient, which we attribute to the degradation of the current source biasing the output stage. This current source must charge the parasitic diffusion BE capacitance of the quite large output transistor in the first stage of the HIGH to LOW transitions. As the current source output is lower, the time to charge this capacitance increases.

However, a phenomenon that does not appear with the decrease of β_F is the shift of the LOW logic output value from 0 V up to 1-2 V [46]. SPICE simulations show that it takes place when either β_F decreases or the collector parasitic resistor, R_C , grows, phenomena also expected due to the accumulated radiation damage.

The last test was the emulation of the flip-flop effect [38], observed in Schmitt triggers (Inset in Fig. 11). It has been reported that, in laser experiments, the energy needed to switch the trigger state depends on the gap between the input voltage, V_{IN} , and the upper bound of the hysteresis cycle, $\frac{R_1/R_2/R_3}{R_2/R_3} \cdot V_{CC}$. The circuit was simulated according to the authors' instructions ($R_1 = R_2 = R_3 = 91 \text{ k}\Omega$) obtaining Fig. 11. One can see that this family of hyperbola-like curves shows a similar dependence on V_{CC} and V_{IN} to those reported in [38], bearing in mind that in that paper the Y-axis showed the threshold laser energy by single photon-absorption instead of the deposited charge.

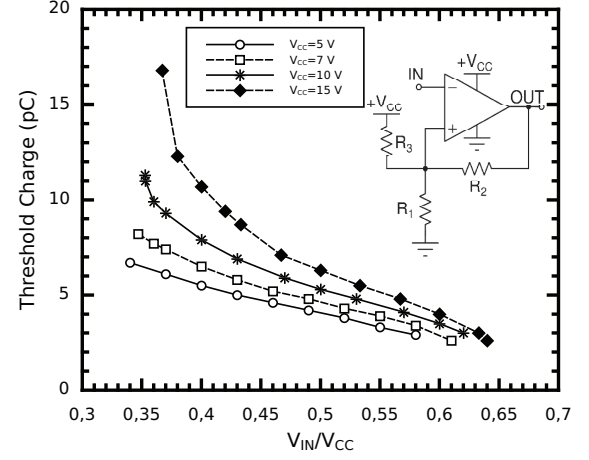


Figure 11. Flip-flop effect in a Schmitt trigger with an LM124A as core (transients originating in Q09 and the initial state being $V_{OUT} = V_{CC}$). This graph is equivalent to Figs. 12 & 17 in [38].

V. CONCLUSION

This paper has shown that it is feasible to build SPICE micromodels for analog integrated circuits from public sources of information, such as textbooks, datasheets, and scientific papers. Thus, it is possible to adapt the micromodels to emulate realistic single event transients to study how the perturbation propagates in the system where the integrated circuit works. Besides, the micromodels help to understand how parameters such as the power supplies, radiation damage, etc. affects the shape of the transients. Finally, these simulations do not require powerful machines or expensive software since they can be performed with open-source tools in a typical personal computer.

VI. ACKNOWLEDGMENTS

The authors would like to thank Dr. Isabel López for the support in the preparation of the laser tests as well as Dr. Carmen Pérez, Dr. Álvaro del Prado, and Dr. Enrique San Andrés for the fruitful discussions about SPICE in the last years. All of them are or were with the Departamento de Física Aplicada III of the Universidad Complutense de Madrid.

REFERENCES

- [1] "The NGSpice project." [Online]. Available: <http://ngspice.sourceforge.net/>.
- [2] Sandia Lab., "The Xyce project." [Online]. Available: <http://xyce.sandia.gov>.
- [3] "SPICE Opus." [Online]. Available: <http://fides.fe.uni-lj.si/spice/index.html>.
- [4] Linear Technology, "LTSpice IV." [Online]. Available: <http://www.linear.com/designtools/software/>.
- [5] Analog Devices Inc., "MT-099: Analog Circuit Simulation." [Online]. Available: <http://www.analog.com/static/imported-files/tutorials/MT-099.pdf>, 2009.
- [6] N. J.-H. Roche, L. Dusseau, J. Boch, Y. G. Velo, J. Vaille, F. Saigne, G. Auriel, B. Azais, S. P. Buchner, R. Marec, P. Calvel, and F. Bezerra, "Development of a New Methodology to Model the Synergistic Effects Between TID and ASETs," *IEEE Trans. Nucl. Sci.*, vol. 57, pp. 1861–1868, Aug. 2010.

- [7] N. J.-H. Roche, L. Dusseau, J. Vaille, J. Mekki, Y. G. Velo, S. Perez, J. Boch, F. Saigne, R. Marec, P. Calvel, F. Bezerra, G. Auriel, and B. Azais, "Investigation and Analysis of LM124 Bipolar Linear Circuitry Response Phenomenon in Pulsed X-Ray Environment," *IEEE Trans. Nucl. Sci.*, vol. 57, pp. 3392–3399, Dec. 2010.
- [8] F. Roig, L. Dusseau, A. Khachatrian, N. J. H. Roche, A. Privat, J. R. Vaille, J. Boch, J. H. Warner, F. Saigne, S. P. Buchner, D. McMorrow, P. Ribeiro, G. Auriel, B. Azais, R. Marec, P. Calvel, F. Bezerra, and R. Ecoffet, "Modeling and Investigations on TID-ASETs Synergistic Effect in LM124 Operational Amplifier From Three Different Manufacturers," *IEEE Trans. Nucl. Sci.*, vol. 60, pp. 4430–4438, Dec. 2013.
- [9] F. Roig, L. Dusseau, P. Ribeiro, G. Auriel, N. J.-H. Roche, A. Privat, J. R. Vaille, J. Boch, F. Saigne, R. Marec, P. Calvel, F. Bezerra, R. Ecoffet, and B. Azais, "Study and Modeling of the Impact of TID on the ATREE Response in LM124 Operational Amplifier," *IEEE Trans. Nucl. Sci.*, vol. 61, pp. 1603–1610, Aug. 2014.
- [10] F. Roig, L. Dusseau, P. Ribeiro, G. Auriel, N. J.-H. Roche, A. Privat, J.-R. Vaille, J. Boch, F. Saigne, R. Marec, P. Calvel, F. Bezerra, R. Ecoffet, and B. Azais, "Impact of Neutron-Induced Displacement Damage on the ATREE Response in LM124 Operational Amplifier," *IEEE Trans. Nucl. Sci.*, vol. 61, pp. 3043–3049, Dec. 2014.
- [11] S. Jagannathan, D. R. Herbison, W. T. Holman, and L. W. Massengill, "Behavioral Modeling Technique for TID Degradation of Complex Analog Circuits," *IEEE Trans. Nucl. Sci.*, vol. 57, pp. 3708–3715, Dec. 2010.
- [12] R. L. Pease, "Modeling Single Event Transients in Bipolar Linear Circuits," *IEEE Trans. Nucl. Sci.*, vol. 55, pp. 1879–1890, Aug. 2008.
- [13] Y. Boulghassoul, L. W. Massengill, A. L. Sternberg, R. L. Pease, S. Buchner, J. W. Howard, D. McMorrow, M. W. Savage, and C. Poivey, "Circuit modeling of the LM124 operational amplifier for analog single-event transient analysis," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3090–3096, Dec. 2002.
- [14] The MOSIS Service, "Wafer Electrical Test Data and SPICE Model Parameters." [Online]. Available: <http://www.mosis.com/pages/Technical/Testdata/index>.
- [15] University of Berkeley, "List of BJT SPICE parameters." [Online]. Available: http://bwrcs.eecs.berkeley.edu/Classes/IcBook/SPICE/UserGuide/elements_fr.html.
- [16] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, ch. 2, pp. 106–115. John Wiley and Sons (Asia), 5th, International student version ed., 2010.
- [17] A. L. Sternberg, L. W. Massengill, S. Buchner, R. L. Pease, Y. Boulghassoul, M. W. Savage, D. McMorrow, and R. A. Weller, "The role of parasitic elements in the single-event transient response of linear circuits," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3115–3120, Dec. 2002.
- [18] Y. Boulghassoul, L. W. Massengill, T. L. Turflinger, and W. T. Holman, "Frequency domain analysis of analog single-event transients in linear circuits," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 3142–3147, Dec. 2002.
- [19] F. Wrobel, L. Dillillo, A. D. Touboul, V. Pouget, and F. Saigne, "Determining Realistic Parameters for the Double Exponential Law that Models Transient Current Pulses," *IEEE Trans. Nucl. Sci.*, vol. 61, pp. 1813–1818, Aug. 2014.
- [20] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, ch. 10. Oxford University Press, Inc., international 6th ed., 2011.
- [21] S. Soclof, *Analog Integrated Circuits*. Solid State Physical Electronics, Prentice Hall, Inc., 1st ed., 1985.
- [22] National Semiconductor, "LM111 datasheet." [Online]. Available: <http://www.ti.com/lit/ds/symlink/lm111.pdf>.
- [23] Fairchild Semiconductor, "LM111 datasheet." [Online]. Available: <https://www.fairchildsemi.com/datasheets/LM/LM311.pdf>.
- [24] National Semiconductor, "LM119 datasheet." [Online]. Available: <http://www.ti.com/lit/ds/symlink/lm119.pdf>.
- [25] A. L. Sternberg, L. W. Massengill, R. D. Schrimpf, and P. Calvel, "Application determination of single-event transient characteristics in the LM111 comparator," *IEEE Trans. Nucl. Sci.*, vol. 48, pp. 1855–1858, Dec. 2001.
- [26] S. Buchner, D. McMorrow, A. Sternberg, L. Massengill, R. L. Pease, and M. Maher, "Single-event transient (SET) characterization of an LM119 voltage comparator: an approach to SET model validation using a pulsed laser," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 1502–1508, Jun. 2002.
- [27] National Semiconductor, "AN-74 LM139/LM239/LM339 A Quad of Independently Functioning Comparators." [Online]. Available: <http://www.ti.com/lit/an/snoa654a/snoa654a.pdf>, May 2004.
- [28] R. J. Widlar, "An IC Voltage Comparator for High Impedance Circuitry. National-Semiconductor App. Not. LB-12." [Online]. Available: <http://www.ti.com/lit/an/snoa685b/snoa685b.pdf>, January 1970.
- [29] R. J. Widlar, "Precision IC Comparator Runs from +5V Logic Supply. National-Semiconductor App. Not. AN-41." [Online]. Available: <http://www.ti.com/lit/an/snoa642b/snoa642b.pdf>, October 1970.
- [30] I. López-Calle, F. J. Franco, J. A. Agapito, and J. G. Izquierdo, "Load resistor as a worst-case parameter to investigate single-event transients in analog electronic devices," in *2011 IEEE Spanish Conference on Electron Devices (CDE)*, pp. 1–4, Feb. 2011.
- [31] Texas Instruments, "LM6181 datasheet." [Online]. Available: www.ti.com/lit/ds/symlink/lm6181.pdf.
- [32] P. Jaulent, V. Pouget, D. Lewis, and P. Fouillat, "Study of Single-Event Transients in High-Speed Operational Amplifiers," *IEEE Trans. Nucl. Sci.*, vol. 55, pp. 1974–1981, Aug. 2008.
- [33] M. W. Savage, T. Turflinger, J. L. Titus, H. F. Barsun, A. Sternberg, Y. Boulghassoul, and L. W. Massengill, "Variations in SET pulse shapes in the LM124A and LM111," in *IEEE Radiation Effects Data Workshop*, pp. 75–81, 2002.
- [34] D. Chen, S. P. Buchner, A. M. Phan, H. S. Kim, A. L. Sternberg, D. McMorrow, and K. A. LaBel, "The Effects of Elevated Temperature on Pulsed-Laser-Induced Single Event Transients in Analog Devices," *IEEE Trans. Nucl. Sci.*, vol. 56, pp. 3138–3144, Dec. 2009.
- [35] L. Bonora and J.-P. David, "An attempt to define conservative conditions for total dose evaluation of bipolar ICs," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 1974–1980, Dec. 1997.
- [36] National Semiconductor, "LM124 datasheet." [Online]. Available: <http://www.ti.com/lit/ds/symlink/lm124.pdf>.
- [37] N. J.-H. Roche, S. Perez, J. Mekki, Y. Gonzalez Velo, L. Dusseau, J. Boch, J. R. Vaille, F. Saigne, R. Marec, P. Calvel, F. Bezerra, G. Auriel, B. Azais, and S. P. Buchner, "Study of Synergism Effect Between TID and ATREE on the Response of the LM124 Operational Amplifier," *IEEE Trans. Nucl. Sci.*, vol. 58, pp. 2890–2897, Dec. 2011.
- [38] N. J. H. Roche, S. P. Buchner, F. Roig, L. Dusseau, J. H. Warner, J. Boch, D. McMorrow, F. Saigne, G. Auriel, and B. Azais, "Investigation of Flip-Flop Effects in a Linear Analog Comparator-With-Hysteresis Circuit," *IEEE Trans. Nucl. Sci.*, vol. 60, pp. 2542–2549, Aug. 2013.
- [39] S. Buchner, D. McMorrow, C. Poivey, J. J. Howard, Y. Boulghassoul, L. W. Massengill, R. Pease, and M. Savage, "Comparison of single-event transients induced in an operational amplifier (LM124) by pulsed laser light and a broad beam of heavy ions," *IEEE Trans. Nucl. Sci.*, vol. 51, pp. 2776–2781, Oct. 2004.
- [40] S. Buchner, D. McMorrow, N. Roche, L. Dusseau, and R. L. Pease, "The Effects of Low Dose-Rate Ionizing Radiation on the Shapes of Transients in the LM124 Operational Amplifier," *IEEE Trans. Nucl. Sci.*, vol. 55, pp. 3314–3320, Dec. 2008.
- [41] F. J. Franco, I. Lopez-Calle, J. G. Izquierdo, and J. A. Agapito, "Modification of the LM124 Single Event Transients by Load Resistors," *IEEE Trans. Nucl. Sci.*, vol. 57, pp. 358–365, Feb. 2010.
- [42] C. Palomar, F. J. Franco, I. Lopez-Calle, J. G. Izquierdo, and J. A. Agapito, "Peak Detector Effect in Low-Dropout Regulators," *IEEE Trans. Nucl. Sci.*, vol. 60, pp. 2666–2674, Aug. 2013.
- [43] C. Palomar, F. J. Franco, J. G. Izquierdo, I. López, and J. A. Agapito, "Characteristics of the long duration pulses in a shunt linear voltage regulator," *Nucl. Instrum. Meth. A*, vol. 737, pp. 273–280, Feb. 2014.
- [44] F. J. Franco, C. Palomar, J. G. Izquierdo, and J. A. Agapito, "An analog cell to detect single event transients in voltage references," *Nucl. Instrum. Meth. A*, vol. 770, pp. 135–140, Jan. 2015.
- [45] A. L. Sternberg, L. W. Massengill, R. D. Schrimpf, Y. Boulghassoul, H. J. Barnaby, S. Buchner, R. L. Pease, and J. W. Howard, "Effect of amplifier parameters on single-event transients in an inverting operational amplifier," *IEEE Trans. Nucl. Sci.*, vol. 49, pp. 1496–1501, Jun. 2002.
- [46] M. F. Bernard, L. Dusseau, S. Buchner, D. McMorrow, R. Ecoffet, J. Boch, J. R. Vaille, R. D. Schrimpf, and K. LaBel, "Impact of Total Ionizing Dose on the Analog Single Event Transient Sensitivity of a Linear Bipolar Integrated Circuit," *IEEE Trans. Nucl. Sci.*, vol. 54, pp. 2534–2540, Dec. 2007.