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Spintronic devices: a promising alternative to CMOS devices

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Abstract
The field of spintronics has attracted tremendous attention recently owing to its ability to offer a solution for the present-day problem of increased power dissipation in electronic circuits while scaling down the technology. Spintronic-based structures utilize electron's spin degree of freedom, which makes it unique with zero standby leakage, low power consumption, infinite endurance, a good read and write performance, nonvolatile nature, and easy 3D integration capability with the present-day electronic circuits based on CMOS technology. All these advantages have catapulted the aggressive research activities to employ spintronic devices in memory units and also revamped the concept of processing-in-memory architecture for the future. This review article explores the essential milestones in the evolutionary field of spintronics. It includes various physical phenomena such as the giant magnetoresistance effect, tunnel magnetoresistance effect, spin-transfer torque, spin Hall effect, voltage-controlled magnetic anisotropy effect, and current-induced domain wall/skyrmions motion. Further, various spintronic devices such as spin valves, magnetic tunnel junctions, domain wall-based race track memory, all spin logic devices, and recently buzzing skyrmions and hybrid magnetic/silicon-based devices are discussed. A detailed description of various switching mechanisms to write the information in these spintronic devices is also reviewed. An overview of hybrid magnetic /silicon-based devices that have the capability to be used for processing-in-memory (logic-in-memory) architecture in the immediate future is described in the end. In this article, we have attempted to introduce a brief history, current status, and future prospectus of the spintronics field for a novice.

Keywords Spintronics · Magnetic tunnel junction · Domain wall · All spin logic devices · Skyrmion

Abbreviations

2D	Two dimensions
3D	Three dimensions
AP	Antiparallel
ASL	All spin logic
CAD	Computer-aided design
CPU	Central processing unit
DI-MTJ	Double-interface magnetic tunnel junction
DMI	Dzyaloshinskii–Moriya interaction
DMTJ	Double-barrier magnetic tunnel junction
DOS	Density of state
DRAM	Dynamic random access memory
DW	Domain wall
FeRAM	Ferroelectric random access memory
FIMS	Field-induced magnetic switching
FL	Free layer
FM	Ferromagnetic
GMR	Giant magnetoresistance
HDD	Hard disk drive
IMA	In-plane magnetic anisotropy
ISHE	Inverse spin Hall effect
LIM	Logic-in-memory
LLG	Landau–Lifshitz–Gilbert
LUT	Look-up table
MOSFET	Metal-oxide-semiconductor field-effect transistor
MRAM	Magnetoresistance random access memory
MTJ	Magnetic tunnel junction
NM	Non-magnetic
P	Parallel
PCRAM	Phase change random access memory
PL	Pinned layer
PMA	Perpendicular plane magnetic anisotropy
RM	Racetrack memory
ReRAM	Resistive random access memory
SHE	Spin Hall effect

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SOI	Spin–orbit interaction
SOT	Spin–orbit torque
SRAM	Static random access memory
STT	Spin transfer torque
TAS	Thermal-assisted switching
TMR	Tunnel magnetoresistance
VCMA	Voltage controlled magnetic anisotropy

1 Introduction

Advancements in the field of fabrication technology have sustained the downscaling of CMOS technology over the past five decades due to which performance of the integrated circuits (ICs) has consistently improved following the Moore's law [1, 2]. In 2020, TSMC (Taiwan Semiconductor Manufacturing Company, Limited) is able to successfully manufacture 54 billion MOSFETs to develop Nvidia's GA100 Ampere GPU, and back in 2019, it has manufactured 39.54 billion MOSFETs for commercially available AMD's Zen2 processor architecture using 7nm process technology [3]. However, further scaling is becoming extremely difficult as the transistor size reaches few atomic layers, and the quantum effect starts to kicks-in [4]. This can lead to an increased leakage current due to the quantum tunneling and thereby increases the standby power dissipation [5–7]. This is a serious concern, especially in volatile memory, because we have to constantly supply power to retain the information stored in it. At the same time, due to a higher operating frequency, the dynamic power dissipation increases. It also scale-up heat production to its thermal limits. In addition, when the technology scales down, the size of the global interconnects becomes longer, contributing a significant amount of dynamic power with signal delay [8]. This surge in the standby and dynamic power would increase the operating power requirement in low power VLSI circuits. Though scaling down the power supply seems to a solution for the increased power dissipation, but it demands strict power monitoring and control circuitry, which must be more aggressive and robust at low voltage, and they occupy a significantly large silicon area. A more efficient technique to reduce standby power dissipation is power gating techniques [9, 10], where idle segments of main memory are partially or completely cut-off from the power rails forcing them into sleep mode. Hence zero standby power dissipation can be achieved. Prior to that, the information stored in these circuits (segments of idle main memory) are transferred to nonvolatile memory. But this technique is effective only if the circuit remains in the sleep mode for a long duration of time to achieve break-even. Also, the data transfer rate between main and nonvolatile memory is less. At the same time, catering to the needs is becoming increasingly difficult for artificial intelligence (AI) and big data demands of the low power, high performance storage, and processing units with the CMOS-only technology [11]. In order to fulfill these aggressive demands, semiconductor fabs and device engineers have come up with the variants of semiconductors such as fin field-effect transistor (FinFET) [12, 13] and carbon nanotube field-effect transistor (CNTFET) [14, 15] devices. Circuits consisting of these devices have promised to reduce the power dissipation to some extent and are widely used at present in ICs. However, there is an urge to find alternatives for the future, which leads to go beyond CMOS technology [10, 16, 17]. The semiconductor industry has been consistently putting down the road map for future technological growth by outlining the developments in materials, devices, and systems that can maintain and enhance the storage as well as the computational capacity of current ICs [18].

Spintronics is considered as one of the most promising future technology, in the impending post CMOS era [19–22]. Remarkable advancements in thin-film fabrication technology to build highly interfacial anisotropic magnetic devices along with spin transportation and spin manipulation techniques has grown enormous interests among researchers. In-fact, we are already reaping the benefits of spintronics application since 1994, after the introduction of GMR (giant magnetoresistance) read heads for hard disk drive (HDD) by IBM [23]. Spintronics technology utilizes the spin of an electron along with its charge. Spin property is an intrinsic form of angular momentum possessed by elementary particles such as electrons, neutrons, protons, neutrinos, etc. [24]. Electron spin orientation and its associated magnetic moment is employed as a state variable in spintronics, which has all the potential to offer solutions to the present-day problems faced by the mainstream charge based electronics [25–28]. Unlike in conventional CMOS technology, where the stored charge is lost due to leakage current, the spin and magnetization of an electron are retained indefinitely in spintronic devices. This imparts non-volatility nature to the spintronic device. The main sector where spintronic devices can make an immediate and huge impact is the burgeoning big data, AI and, information and communication technology's (ICT) memory domain. Figure 1 shows the present-day pyramid-like memory structure. The on-chip L1 and L2 cache consisting of static random-access memory (SRAM). Though SRAM is faster, it suffers from an increased standby power dissipation problem due to leakage current caused by scaling of the MOSFETs. Whereas, L3–L4 cache consisting of dynamic random-access memory (DRAM) suffers from depreciation of stored charge and requires regular refreshing circuits, which also increases the power hungriness of these circuits. Spintronic based magnetic random access memory (MRAM) such as spin transfer torque (STT) MRAM and spin–orbit torque (SOT) MRAM can easily overcome these problems, owing to its non-volatility, fast read and write capability, ease of scalability, and high endurance.

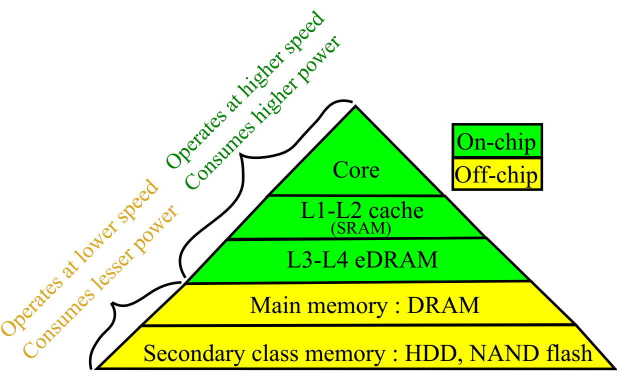


Fig. 1 The speed of the component from bottom to top increases, while the storage volume decreases. Those components are divided into on-chip (embedded with compute circuitry on the same chip) and off-chip (stand-alone as a separate chip) [29, 30]

Table 1 shows a comparison between present (typical) and up-coming (new) memory technologies. From the table, it can be concluded that spintronic based MRAM is the best among the rest of the several nonvolatile embedded memory technologies. From the processing perspective, spintronic devices are being extensively explored in an entirely new class of computer architecture such as all spin logic (ASL) [37] and logic-in-memory (LIM) (or processing-in-memory (PIM)) [38–42]. LIM structures are hybrid in nature, i.e., it employs the contemporary spintronic as well as the current CMOS devices. The most common spintronic device used in LIM is a magnetic tunnel junction (MTJ), which is an elementary device of MRAM. Due to the resistance compatibility, MTJs can be easily integrated with the current generation CMOS circuit. These circuits inherit all the characteristics of spintronic devices. Advancement in fabrication technology such as 3D [43, 44] back-end process enabled the growth of MTJs on top of the silicon layer without compromising the functionality of the circuit [45]. Circuits developed using LIM hold supremacy over the conventional CMOS designs due to its lower power dissipation, non-volatility, fast reading capability, high density, 3D fabrication adaptability, and infinite endurance [25, 37, 46–48].

In recent years due to nano-fabrication capabilities, a sub-branch of spintronics called straintronics being evolved and triggered immense interest in researchers. It explores the coupling between electron spin and its various degrees of freedom to control the magnetization not only electrically but also optically and even acoustically [49–53]. Straintronics is beyond the purview of this article hence we restrict our discussion to spintronic devices. However more information about straintronics and its applications can be found in the Refs. [54–61].

2 Spintronic devices

Figure 2 illustrates the key junctures in spintronics research. The idea of electron spin was proposed in 1925 [62], much before the first integrated circuit (which was in 1958 [63, 64]). But due to the technological limitations and lack of understanding, not much progress was made in employing it, until the discovery of GMR in 1988 [65, 66]. GMR is considered as one of the milestones in the history of physics, which led to the birth of spintronics [47]. Another milestone in the field of spintronic is the proposal of spin transistor by Datta and Das in 1990 [67], which is also called as electro-optic modulator. Though the device is proven theoretically, but due to technical challenges, fabrication of it is still under progress. However, spin transistor has inspired the proposal of wide variety of spintronic based future devices and concepts.

Major classification of spintronic devices are shown in Fig. 3 [7]. Among them, spin valve, MTJ, domain wall nano wire, all spin logic device, skyrmions are the most promising

Table 1 Benchmark table of the performance of typical memory and their comparison with emerging memory technologies [29, 31–36]

Parameters	Typical memory technology			New memory technology				
	SRAM	DRAM	Flash (NAND)	FeRAM	ReRAM	PCRAM	STT-MRAM	SOT-MRAM
Non-volatility	***No***	***No***	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Cell size (F^2)	**50 – 120**	**6 – 10**	**5**	15 – 34	**6 – 10**	4 – 19	6 – 20	6 – 20
Read time (ns)	**≤ 2**	*30*	***10^3***	**≈ 5**	1 – 20	**≈ 2**	1 – 20	**≤ 10**
Write time (ns)	**≤ 2**	*50*	***10^6***	**≈ 10**	*50*	10^2	**≈ 10**	**≤ 10**
Write power	**Low**	**Low**	***High***	**Low**	*Medium*	**Low**	**Low**	**Low**
Endurance (cycles)	**10^{16}**	**10^{16}**	***10^5***	10^{12}	***10^6***	10^{10}	**10^{15}**	**10^{15}**
Future scalability	**Good**	***Limited***	***Limited***	***Limited***	*Medium*	*Limited*	**Good**	**Good**
Retention (Yrs@55°C)	N.A	N.A	*>10*	*>10*	**>20**	*>10*	**>20**	**>20**

Fonts with bold face, italics and bold face italics font indicate the desirable, intermediate and undesirable properties of corresponding technologies, respectively

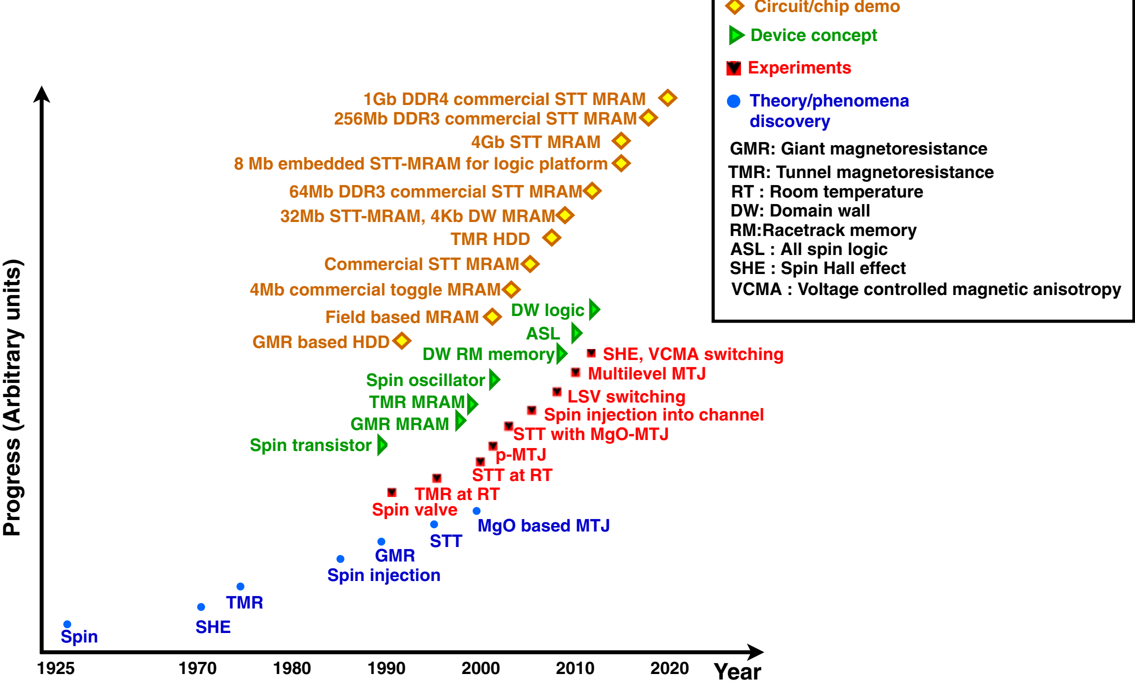


Fig. 2 Historical developments in spintronics research

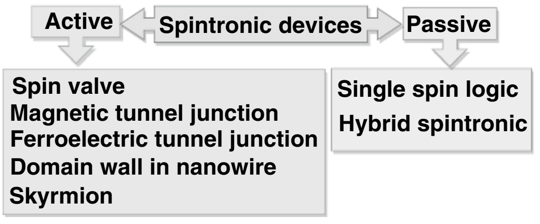


Fig. 3 Classification of spintronic devices [7]

ones due to their high performance and future scope. Hence we have focused our discussion on these devices.

2.1 Spin valve

GMR effect is a phenomenon observed in spin valves, where the electrical conductivity depends upon the relative magnetization direction of ferromagnetic materials in a FM/NFM/FM (ferromagnetic/non-ferromagnetic/ferromagnetic) structure (Fig. 4a, b). It can be understood by considering the scattering of spin-polarized electrons as it passes through the spin valve [68]. Figure 4c, d shows the conduction principle in the spin valve. In FM material, the density of states (DOS) available for spin-up and spin-down electrons are unequal, resulting in a significantly more number of majority electrons (spin is aligned in the same direction as magnetic orientation of the FM layer) compared to minority electrons (spin is aligned in the opposite direction as magnetic orientation of the FM layer). However, the DOS in NFM material is equal for both types of electrons. Hence, when the spin valve is in parallel (P) configuration, due to the arrangement of DOS (Fig. 4c) there is a free flow of majority electrons (spin-up) compared to the minority electrons (spin-down) through NFM, witnessing low resistance for the device. On the contrary, when the spin valve is in an antiparallel (AP) configuration, the arrangement of DOS (Fig. 4d) causes scattering of both spin-up as well as spin-down electrons resulting in relatively high resistance of the device. The equation for GMR is defined as,

$$\mathrm{GMR} = \frac{\triangle R}{R_P}. \tag{1}$$

where $\triangle R$ is the resistance difference between AP and P configuration, and R_P is the resistance of GMR device in P configuration. There are several applications such as GMR sensors, biological applications, space applications, etc. [69], which utilizes the GMR effect; amongst them, the use of spin-valve in the read head of HDD has revolutionized the way to store the information [23, 70]. In 1994 IBM commercially produced the first HDD by incorporating GMR read heads [23]. From 1997 to 2020, the HDD area density has surged from 0.1 Gb/in^2 to ≈ 5–6 Tb/in^2 [70, 71], which suggests that data storage density has an average growth rate 260.86 Gb/in^2 per year by the application of spintronics.

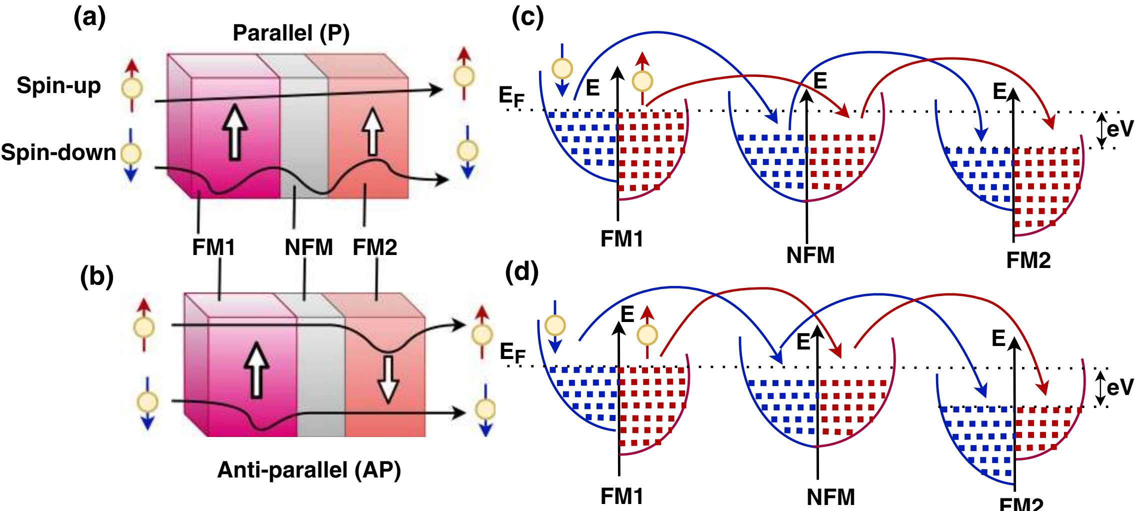


Fig. 4 Spin valve based on the GMR effect. **a** The magnetic orientation of both the FM layers are pointing in the same direction depicting a low resistance P configuration, **c** facilitating a easy flow for majority electrons (spin-up), illustrated with DOS. **b** The magnetic orientation of the FM layers are pointing in the opposite direction depicting a high resistance AP configuration, **d** resulting in a scattered flow of electrons illustrated with DOS [47]

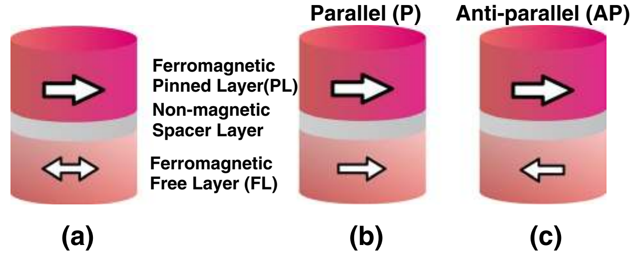


Fig. 5 Schematic of **a** VSV structure. A relative **b** low resistance (P) and **c** high resistance configuration in VSV structure [72]

Basically, there are two types of spin valve structure, vertical spin valve (VSV) and lateral spin salve (LSV). VSV structure (Fig. 5) was generally used as a sensor, which consists of two ferromagnetic (FM) layers separated by a non-magnetic (NM) layer. The magnetic orientation of one of the FM layers is pinned/fixed in a particular direction; hence it is called pinned layer (PL), whereas the magnetic direction of the other FM layer can be either parallel (P) or antiparallel (AP) to the PL. Hence, this layer is called a free layer (FL).

LSV is another variant of the spin valve, whose structure is shown in Fig. 6. It consists of a NM channel layer on which two FM layers are deposited. In this device, local measurements exhibit the magnetoresistance (MR) effect (Fig. 6a). However, non-local measurements (Fig. 6b) have also been experimentally observed [73, 74]. The non-local effects were due to the phenomena of spin injection, spin accumulation, and spin diffusion of pure spin current.

Figure 7 illustrates the difference between charge current and spin current. Unpolarized current consisting of an equal number of both spin-up and spin-down electrons, which flow in the same direction resulting in a charge current but zero spin currents (Fig. 7a). A polarized current consists of an unequal number of both majority (spin-up) and minority (spin-down) electrons, which flows in the same directions resulting in a higher magnitude charge current than spin current (Fig. 7b). The flow of only one type of electron spin in a particular direction, which is also called as a fully polarized current, results in equal magnitude charge and spin currents (Fig. 7c). When an equal number of spin-up and spin-down electrons flow in the opposite direction, which is also called as pure spin current, results in zero charge current but maximum spin current (Fig. 7d). Hence, in pure spin current, spin-up and, spin-down electrons flow in the opposite direction, which is unlike the charge current where both spin-up and spin-down electrons flow in the same direction. Hence, only spin angular momentum flows in the pure spin current. Therefore, problems associated with charge motion, such as resistive power dissipation, heat buildup, and capacitive time are eliminated in the pure spin current flow [75]. However, the generation of pure spin current is difficult, which includes methods such as spin pumping, spin generation using SHE, etc. [76]. In LSV during the non-local measurement process, upon the injection of current at the injector, there is a non-equilibrium spin accumulation in the NM material beneath the FM, i.e., a larger number of spin which are aligned with the FM are present than opposite spins. This spin imbalance creates a spin voltage (ECP-electrochemical potential) due to which spins of opposite nature flow in the

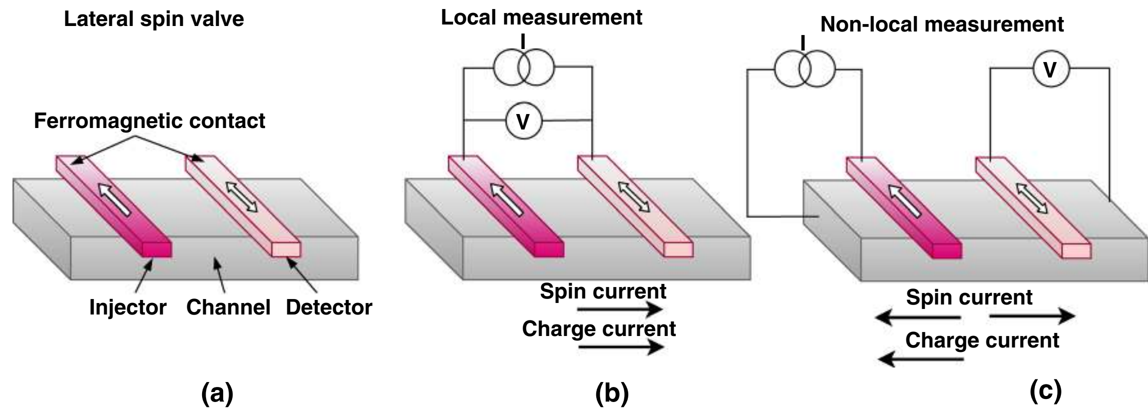


Fig. 6 **a** Physical structure of LSV consisting of FM material as injector and detector upon a NM channel. **b** Local and **c** non-local measurement setup to measure charge and pure spin current [72]

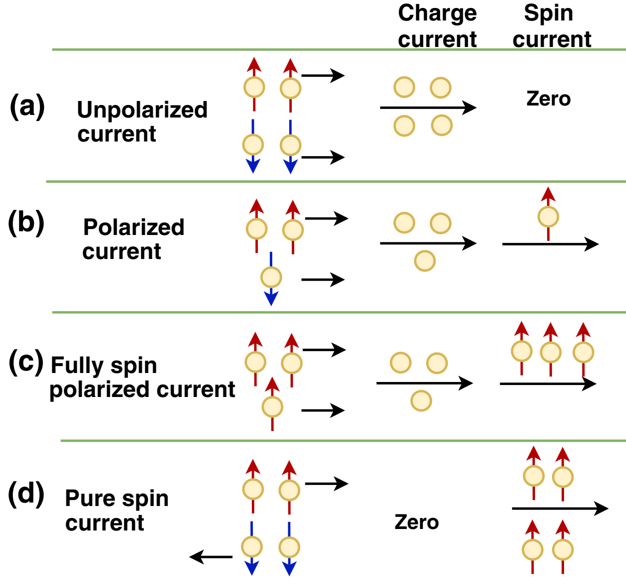
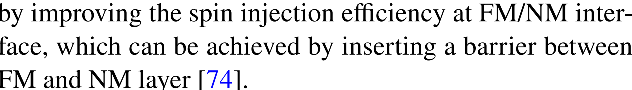


Fig. 7 Illustration of **a** unpolarized current, **b** spin-polarized current, **c** fully polarized current, and **d** pure spin current [75]

opposite direction giving rise to the generation of the pure spin current. As a result, the charge current between the injector and detector layers is zero, whereas the spin current is non-zero. If both injector and detector layers are in P configuration, then the detected voltage indicates the strength of majority electrons, or else when the injector and detector layers are in AP configuration, then the detected voltage would represent minority electrons strength. The spin current decays exponentially due to scattering as it diffuse along NM and vanishes due to spin-flip scattering. Hence the NM material channel length of L must be less than spin-flip length λ. So a variety of NM materials suitable for the spin generation have been investigated [74, 77–80]. Further, the generation efficiency of pure spin current can be enhanced by improving the spin injection efficiency at FM/NM interface, which can be achieved by inserting a barrier between FM and NM layer [74].



2.2 Magnetic tunnel junction

Magnetic tunnel junction, a basic unit of MRAM, is a multilayer magnetic nano-pillar structure, as shown in Fig. 8. If the magnetic orientation of the FM layers (both pinned and fixed layers) are in the plane of the MTJ, then it is known to be in-plane MTJ (i-MTJ), or else if the magnetic orientation of the FM layer is perpendicular to the MTJ plane, then it is called perpendicular plane MTJ (p-MTJ). A detailed explanation about i-MTJ and p-MTJ is presented later in this section. When the magnetic orientation of the free layer (FL) and pinned layer (PL) are in the same direction, then the resistance offered by the device for the flow of current is less, and that is denoted by R_P (parallel state (P) resistance). Whereas, if the magnetic orientation of FL is opposite to the PL, the device offers higher resistance (R_{AP}) to the flow of current, and therefore it is in antiparallel (AP) state. PL can also be designated as a fixed/reference layer. Compared to the VSV, in MTJ, the NM material is replaced by an insulating barrier layer. As a result of which tunnel magnetoresistance (TMR) is observed in MTJs. TMR ratio is the primary performance indicator for an MTJ, and it is defined as,

$$\mathrm{TMR} = \frac{R_{AP} - R_P}{R_P}. \tag{2}$$

where R_P and R_{AP} represent MTJ resistance in P and AP configuration. Hence, MTJ can be treated as a two-valued resistor, which plays a significant role in memory and logical applications. When MTJ is in P and AP configuration, it is assumed to be having stored bit "1" and "0," respectively. And the stored data values are nonvolatile in nature. With

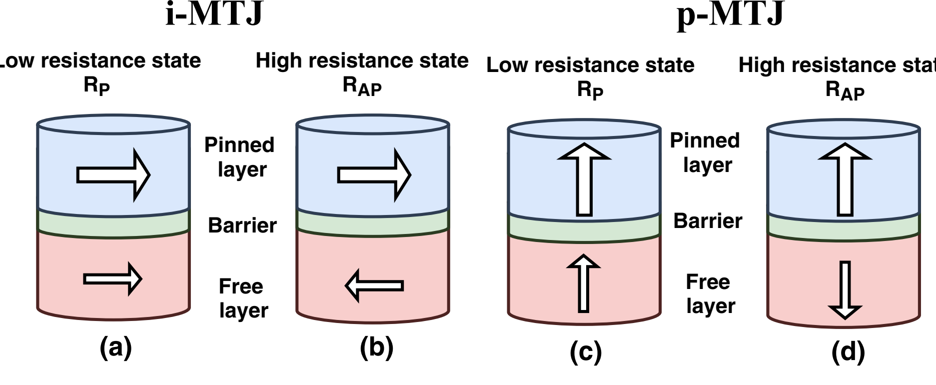


Fig. 8 Low resistance state (R_P) of **a** i-MTJ and **c** p-MTJ, where magnetic orientation of free layer and pinned layer are in the same direction. High resistance state (R_{AP}) of **b** i-MTJ and **d** p-MTJ, where magnetic orientation of free layer and pinned layer are in the opposite direction

the application of an external magnetic field or injecting a suitable current in a particular direction, P and AP (vice versa) configuration of the MTJ can be switched between each other. The first-ever reported TMR ratio was 14% in 1975 with Fe/Ge/Fe structure at 4.2 K [81]. Achieving a high TMR at room temperature is desirable to ensure the faithful working of MTJ devices when used in circuit applications. Due to technical challenges in fabrication methods, not much progress happened to increase the TMR at room temperature until 1994, where amorphous Al_2O_3 was used to achieve 11.8% [82] and 18% [83] TMR. The largest TMR achieved was 70.4%, reported with amorphous Al_2O_3 at room temperature till date [84]. Another noticeable breakthrough was achieved by obtaining TMR of 70% at room temperature by considering crystalline MgO as barrier material [85]. To date, the highest TMR achieved with the MgO barrier at room temperature was 604% in 2008 [86]. Figure 9 shows the developmental road map of TMR ratio with different insulating barriers for MTJ devices. It is predicted to achieve a TMR ratio of 1000% with Heusler + MgO [87] and spinel (Mg–Al–O) [88] barrier MTJ devices in the year 2024 and 2032, respectively, with moderate exploration.

TMR effect can be considered as a spin filtering process that arises due to the band structure of MTJ [68]. A simple interpretation of TMR can be performed using the DOS diagram, as shown in Fig. 10. In P configuration, the majority spins from one FM (FM1) layer can easily tunnel across the barrier to fill up the majority and minority states of another FM (FM2) layer, respectively. However, in the AP configuration, majority spins, and minority spins of one FM (FM1) layer tunnel across the barrier to fill up the minority and majority states of another FM (FM2) layer, respectively. Here the assumption is that no spin-flip occurs during the tunneling process [68]. Tunneling is a quantum mechanical process. In the light of classical physics, electrons should not be able to cross over the insulating barrier. However, according to quantum physics, electrons also possess wave-like properties along with particle-like properties. With sufficient voltage across a thin insulating barrier, the electrons move across and appear on the other side of the thin barrier. This

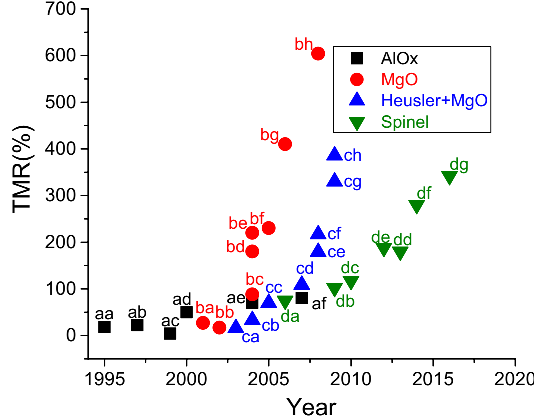


Fig. 9 Developments in TMR ratios at room temperature. MTJ were reported with; AlOx barrier (aa-af) [82–84, 89–92], MgO barrier (ba-bh) [85, 86, 93–95, 95–98], Heusler + MgO barrier (ca-ch) [99–106], Spinel barrier (da-dg) [107–113]

is called tunneling, and it is due to the wave-like property of electrons [68].

Magnetic anisotropy: Magnetic anisotropy is another crucial characteristic of MTJ. It is the directional dependence of magnetic material's properties. Magnetic moment of the material tends to align its-self along with its easy axis, in the absence of an external magnetic field or voltage. Easy-axis is the preferred direction along which the magnetic material can be magnetized. With reference to the easy axis, magnetic anisotropy is divided into in-plane magnetic anisotropy (IMA) and perpendicular plane magnetic anisotropy (PMA). Subsequently, the IMA and PMA based MTJ can be depicted as i-MTJ and p-MTJ, respectively. Formerly due to limited knowledge and technological barrier, multilayered bulk spintronic devices that exhibited IMA (such as i-MTJ) behavior was developed and studied. However, the technological advancements in thin-film technology have enabled the fabrication of superior PMA spintronic devices (such as p-MTJ). The nexus between thin film magnetism and MTJ devices is inextricable, and magnetic anisotropy plays a crucial role in the

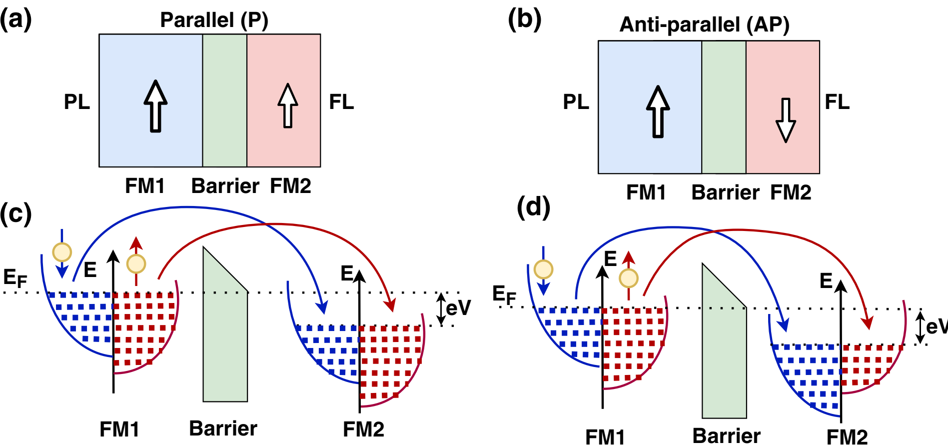


Fig. 10 Illustration of spin dependent tunneling in MTJ from the perspective of DOS. When MTJ is in **a** P configuration, **c** spin-up and spin-down electrons from FM1 tunnel across the barrier to FM2, and occupy their respective subband with the same spin orientation. When MTJ is in **b** AP configuration **d** spin-up and spin-down electrons from FM1 tunnel across the barrier to FM2, and occupy spin-down and spin-up subbands, respectively

behavior of multilayered MTJs. In general, for multilayer structures, effective magnetic anisotropy K_{eff} arises from two components; volume contribution K_{v} and interface contribution K_{s}, and is represented by Eq. 3 [114],

$$K_{\mathrm{eff}} = K_{\mathrm{v}} + \frac{2K_{\mathrm{s}}}{t}. \tag{3}$$

where t is the thickness of the magnetic layer. This relationship depicts the weighted average of magnetic anisotropy energy of interface atoms and inner volume atoms in the multilayer structure. In bulk materials, anisotropy is dominated by the volume component of the equation, whereas, in the thin films, the surface term is dominant; because the thickness becomes very small. In thin-film materials, below a particular thickness called critical thickness (t_{CO}), interface anisotropy K_s is more dominant than volume anisotropy K_v, because the thickness becomes very small. On the contrary, in bulk materials, where the thickness is above t_{CO}, anisotropy is determined by K_v component. Critical thickness is defined by Eq. 4,

$$t_{\mathrm{CO}} = \frac{-2K_s}{K_v} \tag{4}$$

Figure 11 depicts the difference between IMA and PMA pictorially with respect to the t_{CO} and K_{eff}. Since the easy axis of i-MTJ is in the plane of FL; it is realized in elliptical shapes, whereas p-MTJ is circular shaped. A more detailed explanation for the dependence of IMA and PMA upon k_s and k_v can be found in [114, 115]. A comparison between i-MTJ and p-MTJ is briefly illustrated in Table 2.

2.2.1 MTJ writing techniques

Changing MTJ resistance either from R_{AP} to R_P or vice versa, can be achieved by switching the magnetic orientation of the FL. MTJ writing process is also known as switching/

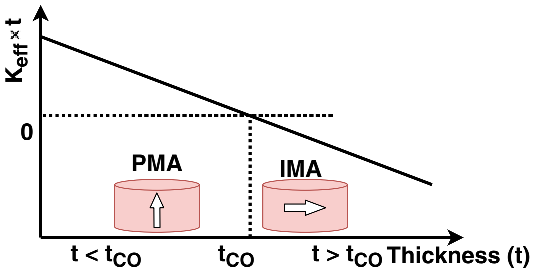


Fig. 11 Illustration of magnetic anisotropy in multilayered nanomagnets w.r.t thickness of the layer. Magnetic material exhibits PMA (IMA) property below (above) t_{CO}

storing the data in MTJ. Following sections discuss the various mechanisms adopted for MTJ writing.

2.2.1.1 Field-induced magnetic switching (FIMS)

FIMS is the first generation MRAM write technique, where an external magnetic field is needed to switch the orientation of FL of MTJ [26]. The magnetic field was generated by passing a current through orthogonal write lines (bit and digit lines) as illustrated in Fig. 12a. The orthogonal currents flowing in bit line a digit line produce an easy-axis and hard-axis switching fields, respectively, and thereby switch the MTJ. Switching from P to AP and AP to P configuration depends upon the flow of the current direction. Though this writing technique has advantages during sensing, it suffers from problems such as half selectivity, high power consumption, low density, and limited scalability. The current needed to produce a magnetic field for MTJ writing is high ($\gtrsim 10$ mA), which increases the power consumption; meanwhile, the electromigration effect limits scalability, which hampers the efforts to achieve low density. Besides, the half-selectivity problem hindered its commercialization. Here, in an array of MTJs, the external field generated would influence the neighboring MTJs to toggle the magnetic orientation of FL. This results in erroneous switching of other neighboring

Table 2 Comparison between i-MTJ and p-MTJ in terms of its basic magnetic anisotropy properties (Color figure online)

Particulars	In-plane magnetic anisotropy	Perpendicular plane magnetic anisotropy
Free layer dimension		
Dominant anisotropy	Shape	Volume (magneto-crystalline)
Magnetic moment equilibrium direction	In-plane	Perpendicular (out-of) plane
Switching current	Larger	Smaller
Scaling	Difficult and not desirable	Easy and desirable
Thermal stability	Low	High
Shape	Elliptical	Circular

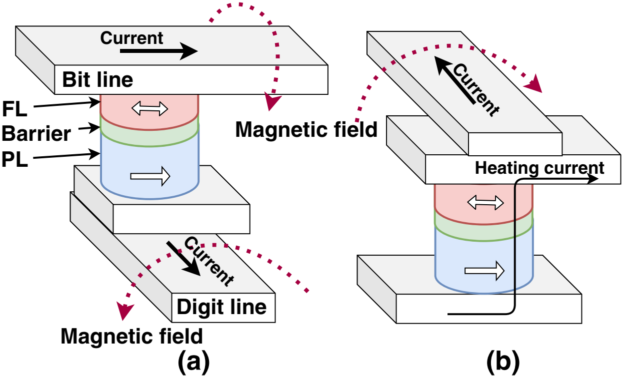


Fig. 12 Schematic for **a** FIMS and **b** TAS mechanism

MTJs in that array. To alleviate this problem, a novel toggle switching mode was proposed by Freescale. Based on this writing technique, they launched the first commercial 4 Mb MRAM product [116]. Though the toggle switching approach addressed the concern of the half-selectivity problem, it did not resolve the issue of high power consumption, low density, and limited scalability.

2.2.1.2 Thermal-assisted switching (TAS) TAS is an improved writing technique compared to FIMS [117]. Writing using TAS is as shown in Fig. 12b, where a heating current is passed through the MTJ that needs to be written, and hence it reduces writing magnetic field strength. In this way, a single current line is sufficient to generate the magnetic field. Thus it significantly reduces writing energy and circuit area. Due to its lower power, higher density, and higher thermal stability TAS was employed in MRAM [118, 119], look-up table (LUT) [120]. However, the requirement of relatively longer cooling duration after being switched has limited the application of TAS in high-speed logic applications.

2.2.1.3 Spin transfer torque STT is considered as a major milestone in the field of spintronics. Independently it was proposed by Berger [121]and Slonczewski [122] in 1996. Later it was experimentally observed in deep sub-micron sized low resistance $CoFeB/Al_2O_3/CoFeB$ MTJ structure in 2004 [123]. A simple s-d model [68] shown in Fig. 13a describes the STT switching mechanism. Conduction electrons (s-electrons) interact with electrons that hold the local magnetic momentum (d-electrons), through exchange interaction (s-d interaction). The total spin angular momentum of this s-d interaction is conserved. Hence, during transport, if the spin angular momentum of the s-electrons is higher than the d-electrons, due to s-d interaction, the spin angular momentum of s-electrons would be transferred to the d-electrons. From Fig. 13b, when the electrons flow from the PL to the FL, s-electrons are spin-polarized and aligned in the magnetic direction of the PL. These are called majority s-electrons. Upon reaching the FL, the spin angular momentum of these electrons is transferred to the d-electrons of the FL to conserve the total spin angular momentum. A large torque called STT is applied, which forces the magnetic orientation of the FL to be aligned toward PL. Hence, if the MTJ was in AP configuration earlier, it switches to P configuration. On the contrary, when the elections flow from FL to PL (Fig. 13c), the transfer of spin angular momentum between reflected minority s-electrons and d-electrons of FL causes the magnetic orientation of FL to be aligned toward PL. As a result of which the MTJ switches from P to AP configuration. So a bidirectional STT write current (I_W) is employed to switch the MTJ between P and AP configuration. FL magnetization state can change only when the torque applied is strong enough, which depends upon the critical current density (J_{cr}). Large current more than J_{cr} can quickly switch the FL magnetization but with a significant power dissipation. J_{cr} is defined by Eq. 5 [122],

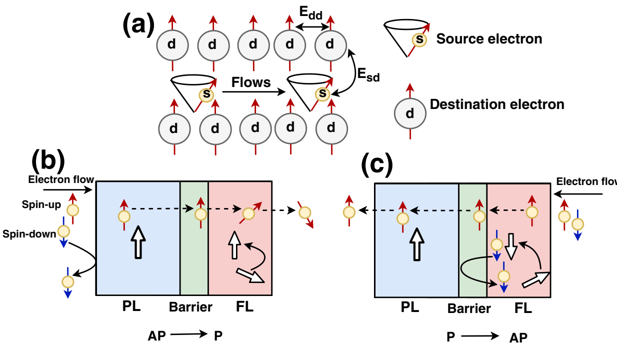


Fig. 13 Schematic representation of STT switching mechanism. **a** A simple s–d model to describe the spin-transfer effect. s-Electrons flow among the localized d-electrons and contribute to a charge and spin current, while d-electrons create a single large local magnetic moment because of strong d–d exchange interaction. s–d exchange interaction causes a precession of s- and d-electrons. Since d-electrons create a single large spin moment, the precession angle of the d-electron system is considerably smaller than that of s-electrons. **b** When s-electrons flows from PL to FL to change the MTJ resistance from R_{AP} to R_P, **c** whereas s-electrons flow from FL to PL to change the MTJ resistance from R_P to R_{AP} [68, 124]

$$J_{cr} = \left(\frac{\alpha}{\eta}\right)\left(\frac{2e}{\hbar}\right)M_S t_F H_{\text{eff}} + 2\pi M_S. \tag{5}$$

where α is Gilbert damping constant, η is the STT efficiency parameter, e is electron charge, $\hbar$ is reduced Planck constant, M_S is the saturation magnetization, t_F is thickness of the FL and H_{eff} is effective magnetic field. Dynamics of STT switching behavior is described by the modified Landau–Lifshitz–Gilbert (LLG) equation [125, 126] which is defined in Eq. 6,

$$\frac{\partial \mathbf{m}}{\partial t} = -\gamma\mu_0 \mathbf{m}\times\mathbf{H}_{\text{eff}} + \alpha\mathbf{m}\times\frac{\partial \mathbf{m}}{\partial t} - \frac{\gamma\hbar J\mathbf{P}}{2et_F M_S}\mathbf{m}\times(\mathbf{m}\times\mathbf{m_r}). \tag{6}$$

Where $\mathbf{m}$ is initial magnetic moment, γ is gyromagnetic ratio, μ_0 is the vacuum permeability, $\mathbf{P}$ is spin-polarization, $\mathbf{m_r}$ is unit vector along the PL magnetization, J is write current density. Three types of torques influence $\mathbf{m}$, viz., field-induced torque, Gilbert damping torque, and STT, as shown in Fig. 14. Field-induced torque causes $\mathbf{m}$ to precess around $\mathbf{H}_{\text{eff}}$. Gilbert damping torque reduces the precession angle θ and pushes $\mathbf{m}$ toward $\mathbf{H}_{\text{eff}}$ and thereby leads the relaxation of precession. STT is either P or AP to Gilbert damping torque, which depends upon the polarity and density of the current. When STT and Gilbert damping torques are AP, with J_{cr} mentioned in Eq. 5, switching of FL takes place. Since STT requires only a bidirectional lower current density ($10^6 \sim 10^7$ A/cm^2) and a simple writing mechanism, it is much superior to FIMS and TAS in terms of power dissipation. The issue of half selectivity and the requirement of heating current is completely eliminated in the STT

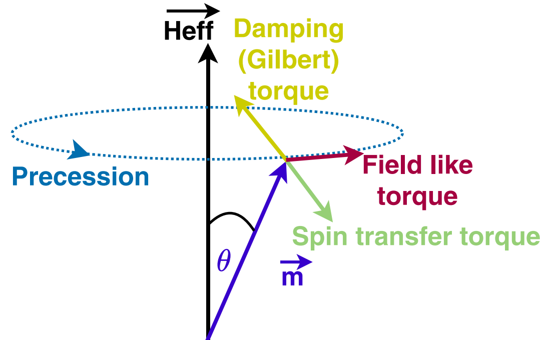


Fig. 14 Magnetization dynamics described in Eq. 6

mechanism. It also promises scaling of the STT-MTJ based circuits, to achieve a higher density. Due to all these advantages, the STT switching mechanism is widely used both in memory, logic, and hybrid circuit design. All these have facilitated the launch of MRAM based commercial products [127].

Magnetic anisotropy plays a vital role in the STT switching mechanism. Compared to p-MTJ, the i-MTJ poses several problems when used in circuit applications, such as short retention time of the stored data, lower thermal stability, and a relatively higher critical current (I_{CO}) needed to switch the magnetic orientation of FL [128, 129]. As the size of i-MTJ decreases, it provides lower energy barrier and lowers thermal stability which is illustrated in Eqs. 7 and 8, respectively, as,

$$E_{\parallel} = \frac{\mu_0 M_s V_F H_{K\parallel}}{2}. \tag{7}$$

$$\Delta_{\parallel} = \frac{E}{k_B T} = \frac{\mu_0 M_S V_F H_{K\parallel}}{2k_B T}. \tag{8}$$

Where $H_{K\parallel}$ is in-plane anisotropy field, V_F is FL volume, k_B is Boltzmann's constant and, T is temperature. Energy barrier and thermal stability for p-MTJ is defined in Eqs. 9 and 10, respectively, as,

$$E_{\perp} = \frac{\mu_0 M_S V_F H_{K\perp}}{2}. \tag{9}$$

$$\Delta\perp = \frac{E\perp}{k_B T} = \frac{\mu_0 M_S V_F H_{K\perp}}{2k_B T}. \tag{10}$$

Where $H_{K\perp}$ is perpendicular plane anisotropy field. As $H_{K\perp}$ is much higher than $H_{K\parallel}$, p-MTJ is more thermally stable than its counterpart. Another important factor which favors p-MTJ is I_{CO} which is given in Eqs. 11 and 12 for i-MTJ and p-MTJ, respectively, as,

$$I_{C0\parallel} \simeq \alpha \frac{\gamma \mu_0 e}{\mu_B P} M_s V_F \left(H_{K\parallel} + \frac{M_s}{2} \right). \quad (11)$$

Where μ_B is the Bohr magneton.

$$I_{C0\perp} = \alpha \frac{\gamma \mu_0 e}{\mu_B P} M_s V_F H_{K\perp}. \quad (12)$$

Comparison between Eqs. 11 and 12 elicits that STT must overcome additional $M_s/2$ factor in i-MTJ for satisfactory performance. Therefore p-MTJ requires lower write current than i-MTJ. The CoFeB/MgO-based STT p-MTJ has exhibited high performance with a TMR of 120% at room temperature with; a small size of 40nm diameter, a good Δ of 40, and low I_{CO} of 49 µA [130]. Recently, 8 Mb sized STT-MRAM with TMR of 180% and a data retention period of 10 years has been embedded with a 28nm logic platform [131]. With a compact cell structure, a high-density 4Gb STT-MRAM with a 90nm pitch has also been demonstrated [132]. Lu et.al., has embedded fully functional STT operated p-MTJ macro (1 Mb, × 32/× 64 IO) in 40nm, which is highly energy efficient for low power IoT applications [133]. Emulation of ARM-core-based CPU running applications like MPEG and video game on Linux OS shows an 80% reduction in power consumption without any performance penalty with STT-based p-MTJ cache compared to its conventional SRAM counterpart [134]. Companies like Everspin Technologies have already commercialized 256 Mb STT-MRAM (DDR3) and 1 Gb STT-MRAM (DDR4) memory [127]. This has catapulted the expectation to implement p-MTJ devices in realistic future memory and hybrid circuit applications.

In recent years, many efforts are underway to investigate the methods to reduce the I_{CO} at the same time, improve the thermal stability Δ and switching speed of MTJ structures [129, 135–142]. Variants of MTJ structures have also been proposed in the literature [140–142] (depicted in Fig. 15). It consists of multiple polarizer layers to enable an easier and quicker STT switching. The polarizer 2 layer in Fig. 15a is aligned in-plane of the MTJ, whereas, in Fig. 15b, it is slightly canted [140]. The insertion of Cu/NM spacer between FL and polarizer 2 would tilt the easy axis of the FL due to the STT originated from the spin-polarized current. When the FL slightly off from its easy axis, it can be easily switched through the spin-polarized current generated by PL. The structural modification presented here reduced the incubation delay and thereby enhanced the switching speed by at least 50% compared to that of regular STT-MTJ structures [140]. Figure 15c shows the variant of canted polarizer 2 layer with the magnetic orientations of polarizer layers that are non-collinear with the FL. Working on STT switching mechanism, it facilitates either improvement or delay in the switching speed, depending upon the angle between polarizer 2 and FL [141]. A more effective

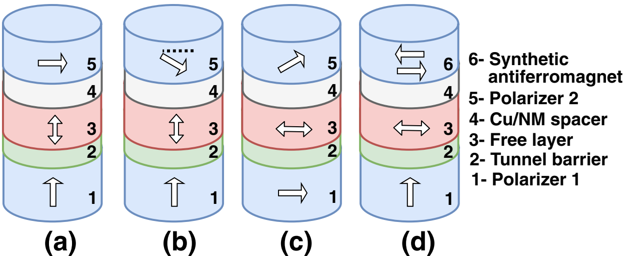


Fig. 15 Variants of conventional MTJ, depicting MTJ stacks with multiple polarizer layers [46, 140–142]

method to achieve MTJ switching was reported in Ref. [142] (Fig. 15d), wherein a synthetic antiferromagnetic layer was used. In this arrangement, a orthogonal switching torque (OST) was developed, which facilitate the fast switching of MTJ with a speed < 500 ps at 0.7V. However, this structure suffers from the issue of thermal reliability, wherein write error are common under the influence of temperature fluctuations [46].

The results obtained with the recently developed double-interface MTJ (DI-MTJ) structures are more encouraging from the thermal stability point of view [135–139]. Figure 16a shows the structure of DI-MTJ is consisting of MgO/CoFeB/Ta/CoFeB/MgO. Compared to the conventional CoFeB/MgO /CoFeB single-interface MTJ (SI-MTJ) (Fig. 16b), DI-MTJ has additional MgO-CoFeB layers. In the fabricated DI-MTJ structure, a thermal stability of $\Delta = 95$ was reported [135]. In comparison, the thermal stability of the SI-MTJ structure was found to be $\Delta = 51$. Hence, there is an improvement in Δ by 1.9 times in DI-MTJ compared to SI-MTJ. This increase in Δ can be attributed to the increase in the total area of the CoFeB layer in DI-MTJ. However, there was no significant reduction in the I_{CO}. Here the chosen diameter of MTJ was kept at 70 nm [135]. Later, the study of I_{CO} was conducted (for sub-40 nm MTJ diameter) with a steady decrease in the diameter of DI-MTJ from 56 to 11 nm [136]. It was encouraging to note that, as there is a reduction in the DI-MTJ diameter, the value of I_{CO} also got reduced. Also, it was observed that there was no degradation in Δ until the DI-MTJ diameter reached 30nm. However, below 30 nm, Δ was found to be reduced with a decrease in the diameter. On the contrary, the ratio of Δ/I_{CO} continues to increase with decreasing DI-MTJ diameter, which suggests that the effective damping constant decreases with the device dimensions. In the DI-MTJ structure electrode above the upper MgO was non-magnetic, and hence, the impact of STT or TMR was absent on the storage layer. Hence, a double-barrier MTJ (DMTJ) structure was proposed, whereby adding an additional PL on the top of the second MgO layer, as shown in Fig. 16c, d [137–139]. Depending on whether the storage/free layer is chosen as a composite ferromagnetic layer (Fig. 16c) or a synthetic

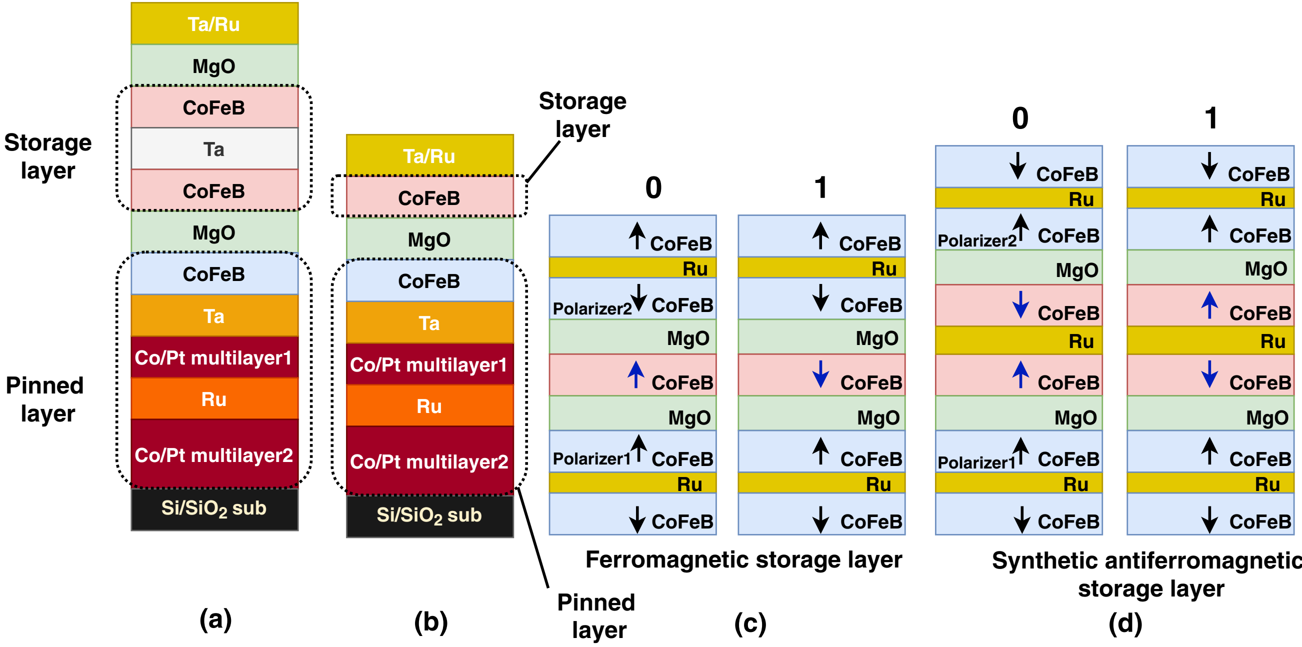


Fig. 16 Schematic of **a** double-interface magnetic tunnel junction and **b** single-interface magnetic tunnel junction [136]. MTJ stack structure representing double-barriers MTJs with **c** single ferromagnetic and **d** synthetic antiferromagnetic storage layers [138]

antiferromagnetic layer (Fig. 16d), the magnetic alignment of the two polarizing layers should be in AP or P configuration, respectively. This would increase the efficiency of the MTJ device due to the STT contributions from both bottom and top PL. Most importantly, the I_{CO} was reduced by a factor of 10 [137]. Lower I_{CO} in DMTJ compared to single-barrier MTJ (SMTJ) can be elicited with two distinct reasons. First is the presence of two PL, which provides spin torque to the FL from both the bottom and top PL; this is a factor 2x improvement. Second, since two PL are set in AP to each other, one of the PL always favors AP configuration for the FL, which provides AP to P spin torque. In recent works [143, 144], shape anisotropy is revisited for DI-MTJ devices, and a high thermal stability of $\Delta = 80$ is obtained for device size smaller than 10nm. This was achieved by dramatically increasing the thickness of the CoFeB (FM material) storage layer in the order, or larger than the MTJ diameter. Hence with minor modifications in the existing device structure, a high thermal stability could be maintained for 10nm p-MTJs that works on STT switching mechanism. In Ref. [144], it was estimated that thermal stability up to $\Delta = 60$ could be maintained for p-MTJ with 4nm diameter, based on the experimental data and micromagnetic simulations. Further, it was suggested that a low damping material can be used for thick FM material, which can considerably reduce that write current. In this structure, the thick FM material with its interfacial part which is in contact with tunnel barrier provides high TMR, whereas its bulk part provides low Gilbert damping, which is an additional advantage apart from high thermal stability. In addition, this concept can be extended to in-plane ultrafine MTJs working based on spin Hall-assisted STT switching mechanism [145]. In order to achieve a higher value of Δ and reduced I_{CO} a more diligent engineering in CoFeB-MgO interface is necessary.

2.2.1.4 Spin Hall effect (SHE) Recently much research is focused on achieving high-performance MTJ, which facilitates miniaturization. Though p-MTJ shows satisfactory thermal stability at the sub-volume (< 40 nm) level, a high write current and slow switching speed still remain a matter of concern. Incubation delay is the cause for reduced switching speed in STT operated MTJs, and it is explained as follows. Initially, when the current is turned ON, STT is not acting because the spin orientation of electrons and FL magnetic orientations are collinear at equilibrium. STT is applied only when there is a slight miss-alignment between electron spin orientation and FL magnetic orientation. The induction of this small angle is caused due to the thermal fluctuations, which are highly stochastic in nature. Hence, there a is random incubation time preceding the switching of FL [146]. Therefore, an incubation delay limits the STT switching speed. To tackle this uncertainty in the switching time due to incubation delay in STT-MTJs, generally the write time is kept longer than the ideal switching time. This means STT write current flows even after the completion of STT-MTJ switching. It causes wastage of energy in the write circuitry during STT-MTJ writing process. Hence, apart from structural modifications at the device level, there

are several attempts made at circuit level to reduce the wastage of write power or energy dissipation for STT process as reported in the literature [147–159]. Besides wastage of write energy and switching delay, there is a high risk of MTJ dielectric breakdown due to the flow of bidirectional STT current. Also, since MTJ is a two-terminal device, read and write path is the same for the MTJ devices. Because of which there is a possibility of erroneously writing into the MTJ when read current flows through it.

To overcome the shortcomings of the STT switching method, an advanced SHE-assisted switching mechanism is introduced for MTJ devices. SHE can be applied for both i-MTJ (Fig. 17a and p-MTJ Fig. 17b devices [160–162]. SHE is analogous to the anomalous Hall effect (AHE), where a relativistic spin–orbit coupling (SOC) in an FM material placed in the presence of an external magnetic field produces an asymmetric deflection of electrons based on their spin direction [163, 164]. Due to the difference in the majority and minority carrier electrons (w.r.t spin-up and spin-down) in FM material, an application of charge current produces a transverse spin current. Another requirement for the AHE is the preference of the external magnetic field. Perhaps, the generation of pure spin current in heavy metal (HM) without the application of an external magnetic field is known as SHE. SHE was predicted in 1971 by Dyakonov and Perel [165] based on Mott scattering [166], and about thirty years later, it was revived by Hirsch [167] in 1999. Experimental demonstration of SHE in Pt at room temperature attracted much interest for its possible application to generate substantial spin current [168] in the field of spintronics. There are two distinct mechanisms proposed for SHE: One is extrinsic, and the other is intrinsic. Earlier SHE was believed to be arisen due to extrinsic mechanism, i.e., due to skew scattering of s-electrons [169, 170]. But later, studies have shown that intrinsic mechanisms such as Rashba effects also cause SHE [171, 172].

Figure 18 illustrates the SHE switching mechanism in i-MTJ. It consists of a structure where FL of MTJ is placed on top of the HM strip. HM material has a high atomic number and possesses large spin–orbit interaction (SOI: interaction between spin angular momentum and orbital angular momentum). When unpolarized electrons (charge current density $\mathbf{J}_C$) pass through HM, due to strong SOI, electrons with opposite spins scatter in the opposite direction, creating spin current density ($\mathbf{J}_S$). Hence, a spin current (I_S) is generated from the charge current (I_C) in the HM. The direction of $\mathbf{J}_S$ is transverse to that of $\mathbf{J}_C$. Further, electron spin polarization $\boldsymbol{\sigma}$ is transverse to the direction of both $\mathbf{J}_S$ and $\mathbf{J}_C$. $\mathbf{J}_S$ thus generated is injected into the FL to exert a torque known as SOT, onto the magnetic orientation of FL, and thereby changes its direction [72, 173]. Equations 13 and 14 define the $\mathbf{J}_S$ and I_S .

$$\mathbf{J_S} = \theta_{\mathrm{SH}}(\boldsymbol{\sigma} \times \mathbf{J_C}). \tag{13}$$

$$\mathbf{I}_S = \theta_{\mathrm{SH}}\frac{A_S}{A_C}I_C\boldsymbol{\sigma}, \tag{14}$$

where θ_{SH} is the spin Hall angle, A_S and A_C are the cross-sectional areas through which spin and charge current flow, respectively. If A_S is much larger to A_C we can generate I_S larger than I_C with small θ_{SH}. This is because electrons that travel through HM can repeatedly scatter between HM and FL exerting many units angular momentum [174, 175].

The SOI, which causes SHE, is also responsible for producing a inverse spin Hall effect (ISHE). ISHE is a process that converts the $\mathbf{J}_S$ into $\mathbf{J}_C$. A spin current consisting of opposite spins electrons, traveling in the opposite direction along $\mathbf{J}_S$, is parallel and antiparallel to $\boldsymbol{\sigma}$. SOI bends these two types of electrons in the same direction to generate a transverse $\mathbf{J}_C$ [168]. The direction of $\mathbf{J}_S$, $\mathbf{J}_C$, and $\boldsymbol{\sigma}$ are all perpendicular to each other, as shown in Fig. 19, and their relationship is given by Eq. 15.

$$\mathbf{J}_\mathrm{C} = D_{\mathrm{ISHE}}\mathbf{J}_\mathrm{S} \times \boldsymbol{\sigma}. \tag{15}$$

Where D_{ISHE} is coefficient representing the efficiency of material to produce ISHE. As mentioned previously, switching of FL magnetic direction can be controlled by altering

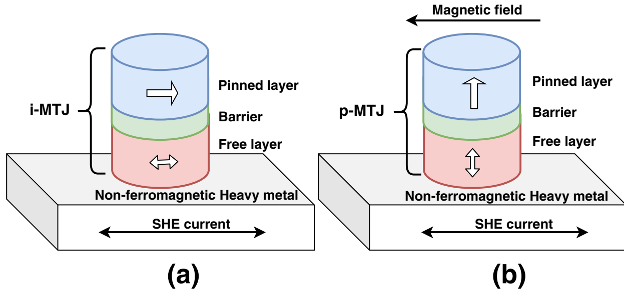


Fig. 17 Three-terminal SHE **a** i-MTJ and **b** p-MTJ device structure [47]

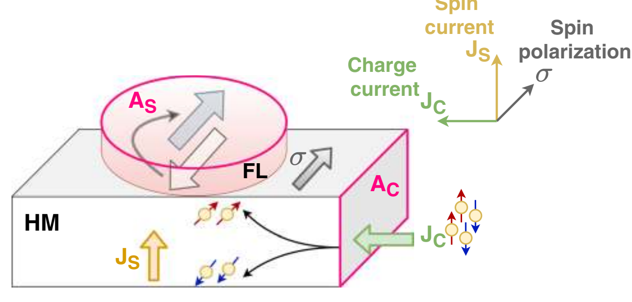


Fig. 18 SHE converting charge current to pure spin current in HM with strong spin–orbit coupling. The direction of $\boldsymbol{\sigma}$, $\mathbf{J}_C$, and $\mathbf{J}_S$ are all perpendicular to each other [72]

the flow of charge current direction in the case of i-MTJs [160, 161]. But this working principle is not applicable for p-MTJ devices because the direction of electron spin in HM and anisotropy of FL are not collinear. Employing an external magnetic field provides a solution to this problem [162] (Fig. 17). Though the generation of an external magnetic field is feasible, its application is undesirable from a practical point of view. Because it poses hurdles such as increased design complexity, reduced sensitivity to process variation, and reduction in the thermal stability due to the lowering of the barrier between stable states, directly affecting the retention time. This hinders the applications of commercial magnetic field-assisted SHE p-MTJ devices. As an alternate solution, SHE-assisted STT (SHE + STT) (Fig. 20) switching mechanism was proposed in [176]. In this case, switching the magnetic direction of FL in p-MTJ is performed by two components, viz., SHE current (J_{SHE}) and STT current (J_{STT}). J_{SHE} and J_{STT} flows along Y- and ±Z-direction, respectively. When p-MTJ needs to be switched from AP to P configuration, J_{SHE} flowing in Y-direction creates a spin accumulation at the FL-HM interface. This exerts a SOT onto the FL magnetic orientation, causing it to tilt toward X-Y plane from its initial −Z-direction. At the same time, J_{STT} flowing in the −Z-direction exerts STT and switches the orientation of FL from XY-plane to Z-direction. On the contrary, to achieve P to AP configuration, only the direction of J_{STT} is reversed (i.e., from −Z to Z), keeping J_{SHE} unchanged. Hence, switching the magnetic orientation direction of FL in p-MTJ can be controlled by altering the STT current direction, whereas the SHE current direction is fixed. SHE + STT switching mechanism significantly increases the writing speed in SHE p-MTJ devices. As depicted in Fig. 21, a short SHE current (0.5 ns) is sufficient enough to eliminate the incubation delay, and it assists STT to switch the FL of the p-MTJ device. Whereas in the absence of assistance from SHE, STT would switch the p-MTJ at 7 ns. This suggests that there is an improvement of 92.85% in the switching speed for SHE + STT compared to STT only switching mechanism [176]. Along with high switching speed, writing energy can also be reduced significantly owing to the low

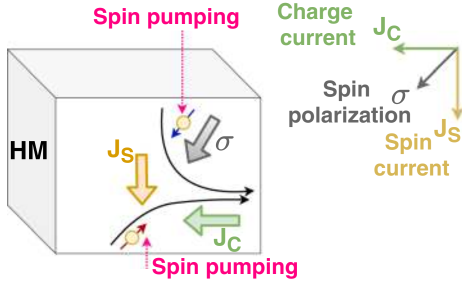


Fig. 19 Schematic illustration of ISHE, where a $\mathbf{J}_S$ is converted to $\mathbf{J}_C$ [168]

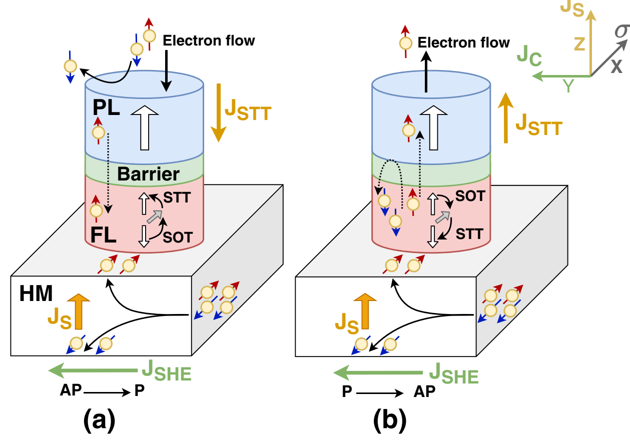


Fig. 20 SHE-assisted STT MTJ switching mechanism. To switch MTJ from **a** AP to P J_{SHE} is in Y- and J_{STT} is in -Z-direction. On the contrary to switch MTJ from **b** P to AP J_{SHE} is in Y- and J_{STT} is in Z-direction

resistance and strong SOI in HM materials. This is achieved by reducing the supply voltage. Further, a lower magnitude of reading current is established in order to read the bits stored in p-MTJs, which bifurcates reading and writing paths. As a result of which the risk of dielectric breakdown is eliminated compared to STT-MTJ. Overall, SHE + STT mechanism-based p-MTJ devices are superior to STT only p-MTJ devices in terms of lower latency for read and write data, lower write energy, higher reliability, and reduced risk of dielectric breakdown.

However, p-MTJs working on SHE switching mechanism discussed so far require the assistance of either an external magnetic field or STT current to change the configuration of FL. But the recent investigations have revealed the possibility of SHE-MTJ switching only by the application of current-induced SOT [177, 178]. This was achieved by carefully engineering the layers of the MTJ structure. In

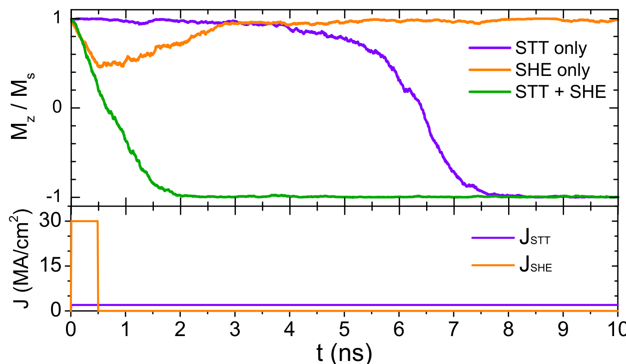


Fig. 21 Magnetization trajectories along with the applied current pulses for STT, SHE and STT + SHE switching mechanism [176]. Reproduced from [176]

Ref. [177], an interesting SOT switching mechanism was demonstrated, viz., current-induced SOT without the assistance of either an external magnetic field or the STT current for SHE-MTJ devices. It consists of a two-terminal stacked structure (Fig. 22a), called Hall bar, consisting of NM metal, FM metal, and oxide from bottom to top (Ta/CoFeB/TaO). In this structure, a minor lateral asymmetry is introduced along the in-plane direction. This lateral asymmetry develops out-of-plane field-like SOT ($\overrightarrow{H_z^{FL}}$), assisting the switching of SHE-MTJ, without the assistance of either magnetic field or STT current. The lateral symmetry was broken to obtain asymmetry by varying the thickness of the insulating layer (TaO), and the field-like SOT, which assists in the switching, depends upon the direction of the charge current flowing in NM material, Ta (It is in the perpendicular direction). Though many theories have been proposed to explain the current-induced SOT mechanism in Hall bar, the following explanation is suitable for the present-day context, i.e., microscopically, $\overrightarrow{H_z^{FL}}$ stems due to the lateral oxidation gradient at the interface of magnetic material and the insulating layer, which induce Rashba-like SOC perpendicular to an effective electric field. The formation of electric field may be due to the redistribution of charges near the CoFeB/TaO interface, depending on the oxygen content. However, a more detailed investigation is necessary to understand the origin of $\overrightarrow{H_z^{FL}}$. Further, the application of this switching mechanism with conventional two-terminal MTJ for memory and logic is not readily possible because it requires a unique wedge-shaped device, which could be obtained by the varying thickness of the insulating layer.

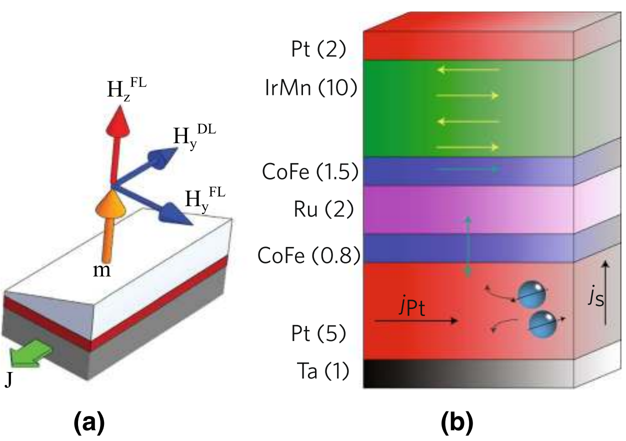


Fig. 22 Two-terminal MTJ devices utilizing Rashba-like SOC. **a** New perpendicular effective field induced by the laterally asymmetric structure. New field is induced due to the breaking of lateral symmetry, which determines the Z component of magnetization for particular direction current. Hence, facilitating the deterministic switching without the necessity of an external magnetic field [177]. **b** Schematic illustration of the SOT switching of a multilayer stacked PMA structure [178]

Similar attempts were also reported in [178], where only SOT was employed to switch the magnetic orientation of FL in SHE-MTJ without the assistance of any external magnetic field or STT current. Here, the working principle of modern hard disk read heads (exchange bias) and MTJ (inter-layer exchange coupling across a thin spacer) was combined to implement SOT switching in a two-terminal structure as depicted in Fig. 22b. Ru spacer layer used in this structure provides a strong interlayer exchange coupling (IEC), and in conjunction with the bottom Pt layer, improves the PMA of FL (CoFe). The symmetry-breaking is achieved by exchange coupling the FL, via a Ru spacer, to an in-plane exchange biased PL (CoFe). It was suggested that the phenomenon of domain nucleation followed by thermally assisted SOT-driven domain wall propagation (originated from Neel type) implements the switching action in this stack. These devices were expected to find their application in SOT oscillators, memory, sensors, and domain wall motion. The concept of domain wall motion is explained in the subsequent Sect. 2.3. However, still more investigations on the SOT-MRAM need to be conducted for commercial applications.

2.2.1.5 Voltage-assisted switching Properties of magnetic materials such as coercivity, magnetization, exchange bias, Curie temperature, magnetoresistance, and magnetic anisotropy are affected by electric fields generated due to the applied voltage [6]. Recently adopted MTJ switching, known as voltage-assisted switching technique, the electric field generated by the applied voltage is utilized to manipulate the magnetic anisotropy of FL and thereby assists in MTJ switching [179–193]. It is also called as voltage-controlled magnetic anisotropy (VCMA) switching mechanism for MTJs. The thickness of FM material plays an important role in the VCMA switching behavior of MTJs, along with the choice of the barrier, FM material, and its crystal orientation [6]. The thickness of FL is more (> 3 nm) in MTJs, which work based on STT, SHE, or SHE + STT switching mechanisms. In this case, magnetic anisotropy is independent of the FL/insulator interface [82, 83, 97, 98]. In this case, the effect of the electric field is negligible due to the screening of electrons. On the contrary, due to the thin FL thickness (1.6 nm) of VCMA-assisted MTJs, the interface anisotropy between FL/insulator is affected by the applied electric field [124, 130, 194]. There are five different mechanisms for the voltage control magnetization of FM material, which are based on the characteristics of FM and barrier materials, viz., carrier modulation, strain effect, exchange coupling, orbital reconstruction, and electrochemical effect [195]. In our paper, we deal with ferromagnetic/insulating junction (CoFeB/MgO) with ultra-thin FL (CoFeB). Hence, the carrier modulation mechanism is applicable for our explanation. In this case of VCMA-MTJ switching mechanism, since CoFeB is 3D ultra-thin metal with MgO

interface, the application of an electric field smaller than 1MV/cm causes large modification in the magnetic anisotropy due to modulation in the carrier density and electron occupancy by changing the orbital occupancy of Fe-3d close to the MgO layer [186, 195]. This assists in switching the magnetic orientation of the FL. VCMA mechanism can be explained in simple terms as follows; an electric field is applied across the MTJ terminals to accumulate electron charges at the FM material/insulator interface, which brings a change of occupation of atomic orbitals at the interface. This, in conjunction with SOI results, change in magnetic anisotropy. Hence, the change (reduction) in the magnetic anisotropy enables the magnetization switching at lower power [196–198].

Figure 23 illustrates the VCMA effect of p-MTJ switching. The uniaxial anisotropy of MTJ (i.e., MTJ is either in P or AP configuration) is separated by an energy barrier (E_b). In conventional MTJ switching, the height of E_b is unaltered, and electrons must possess enough energy to jump over to the other side. On the other hand, in VCMA-assisted MTJs switching, height E_b is controlled by applying a voltage across the MTJ. For example, when the applied voltage (V_b) is greater than or equal to the critical voltage (V_c), E_b height disappears, facilitating electrons to easily move onto the other side and thereby switching the MTJ. This lowered E_b height significantly reduces the switching energy. After the completion of switching, V_b is turned off ($V_b = 0$). Hence, E_b is restored back to the former height. If $0 < V_b < V_c$, E_b height is modestly lowered but does not completely vanish off. On the contrary, the application of negative V_b would raise the height of E_b. Hence, E_b can be modeled as a function of V_b and is defined Eq. 16 [199],

$$E_b(V_b) \approx \left[K_i(V_b) - 2\pi M_s^2 (N_z - N_{x,y}) t_f\right] \cdot A. \tag{16}$$

Where $K_i(V_b)$ is the voltage-dependent interfacial PMA, M_s is the saturation magnetization, t_f is the thickness of the FL, V_b is the bias voltage, A is the sectional area of the MTJ, N_z and $N_{x,y}$ are the demagnetization factors of the MTJ in the perpendicular and in-plane directions. The V_c, which is minimum voltage required to completely eliminate E_b is defined by Eq. 17

$$V_c = \Delta(0) k_B T t_{\text{ox}} / \xi A, \tag{17}$$

where $\Delta(0)$ is thermal stability under zero voltage, k_B is the Boltzmann constant, T is temperature, t_{ox} is the thickness of the oxide layer, and ξ is the VCMA coefficient.

VCMA switching technique can be applied for both i-MTJ as well as p-MTJ devices. Figure 24 illustrates the VCMA switching mechanism for two-terminal i-MTJ. When a voltage pulse $V_b \geq V_c$ is applied across the MTJ terminals, the magnetic orientation of the FL changes from stable state to meta-stable state (i.e., perpendicular to the in-plane). At the same time, an external magnetic field is applied, which acts on the FL magnetic orientation, facilitating it to turn into an in-plane state. Subsequently, the V_b is removed, and thereby switching of i-MTJ is established. Therefore, the external magnetic field assists in achieving an in-plane stable state for the i-MTJ. Here the application of V_b alone does not guarantee deterministic switching in VCMA-MTJ. Because when $V_b \geq V_c$, E_b disappears, resulting in the oscillation of FL magnetic orientation between P and AP configuration. In order to eliminate the uncertainty of MTJ state in this condition, assistance from the external field is quite necessary [192, 193]. One of the important points to note here is that the generation of V_b is unipolar in nature to suppress E_b. Because when the amplitude of V_b gets reversed, E_b

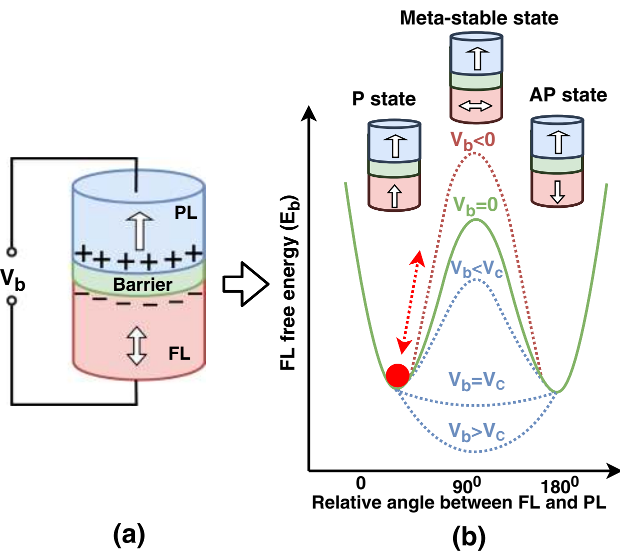


Fig. 23 **a** VCMA-MTJ device structure. **b** Energy barrier height variation corresponding to different voltages (V_b) [199]

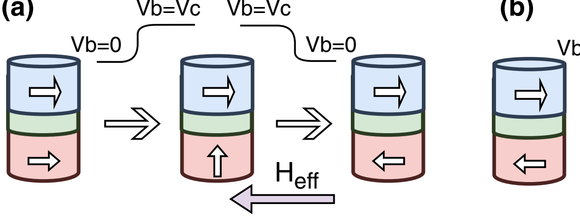


Fig. 24 Voltage-assisted switching in i-MTJ. V_b forces the FL magnetization into a metastable state, which then relaxes to a stable state, i.e., **a** P to AP and **b** AP to P, with the assistance of an external magnetic field, subsequently V_b is then removed

increases rather than decreasing as depicted in Fig. 23. As previously discussed, establishing an external magnetic field always brings-in a complexity in circuit development from the commercial point of view and hence generally needs to be evaded.

VCMA p-MTJs are more attractive due to their higher thermal stability, better scalability, and lower power than i-MTJs [128, 130, 200, 201]. Various switching strategies such as precessional VCMA, precessional VCMA-assisted STT, thermally activated VCMA-assisted STT, and precessional VCMA-assisted SHE switching mechanisms have been reported for the VCMA p-MTJ devices [179, 183, 202–205]. In precessional VCMA switching technique for p-MTJ, unlike in i-MTJ switching, where an external magnetic field needs to be established for deterministic switching, a precise voltage pulse V_b with a particular duration could establish an exact MTJ state switching, without the assistance of an external magnetic field [199]. It requires a study of the previous pulse width to choose a precise pulse duration for deterministic VCMA-MTJ switching [199]. This can also be treated as one of the main drawbacks of this switching regime. With the aid of an external magnetic field or additional write verifying algorithms, this problem can be resolved. As an alternate solution for switching the VCMA p-MTJ deterministically, a more convenient thermally activated switching regime is preferred [199]. In this method, $0 \leq V_b \leq V_c$ is set, which causes the magnetization of FL to be in the damped back state. In this stage, application of the external magnetic field or STT current would deterministically switch the VCMA-MTJ state. As we have already discussed previously, the generation of the external magnetic field increases the design complexity and limits the scaling. Hence, the application of current to produce STT is preferred for VCMA-MTJ switching. Other variants of p-MTJ switching based on VCMA are VCMA-assisted STT and VCMA-assisted SHE. In precessional VCMA-assisted STT (precessional VCMA-assisted SHE) switching regime, an STT (SHE) current, which assists to switch the MTJs after the application of V_b produce STT (SHE) effect is also called as VCMA + STT (VCMA + SHE) switching mechanism [199, 201, 206]. Circuits developed with VCMA + STT were found superior to precessional VCMA, VCMA + SHE in terms of speed, power, and reliability [183, 199, 206–209]. In general, VCMA-MTJs possess advantages over STT-MTJs in terms of faster read-write speed and lower read-write energy. For example, energy dissipation of ~ 6 fJ/bit is demonstrated with the VCMA switching mechanism in 50 nm diameter CoFeB/MgO/CoFeB MTJ with 0.5ns speed [189]. Further, Ref. [191] demonstrated VCMA switching with 2.8-nm-thick MgO barrier with an energy consumption of ~ 6.3 fJ/bit. In terms of scalability, with VCMA + MTJs, we can achieve twice the density of STT-MTJs. Due to all these advantages, VCMA-MTJs have attracted much attention both for academia and industry for memory and logic-based application.

2.3 Magnetic domain wall nanowire

Ferromagnets are divided into domains with their magnetic vector orientated in different directions, as a result of which their total magnetization becomes zero [210]. Domain wall (DW) is an interface that separates neighboring magnetic regions or domains which are unparallel to each other in a nanowire [211–214]. Typically DW is a few nanometers wide (Fig. 25) within which the magnetization rotates from one direction to another. Binary information is stored in these domains in the form of a magnetization vector. This information is read by sensing the magnetic orientation direction. The DWs are mobile in nature, i.e., it can be pushed by sending current pulses flowing through nanowire. This phenomenon is called a current-induced domain wall motion (CIDWM) (Fig. 25).

In 1978, Berger first proposed the idea of CIDWM [215]. Further, in 1984 he explained the reaction force on the wall due to the reflection of electric currents in a thin film [216]. CIDWM can be explained by the s-d model. When a spin-polarized current-carrying s-spin electrons cross the DW (DW are caused due to localized d-spin magnetization), there is an adiabatic reversal of s-spin electrons which would induce a reaction torque onto the DW (localized d-spin magnetization) satisfying the conservation of angular momentum, which results in the motion of the DW. Many applications, such as logic gates [217–219], magnetic memory [220], reconfigurable logic [221, 222], full-adder (FA) [223], and nano-oscillator [224] were developed using the concept of DW.

CIDWM-based magnetic memory is also called racetrack memory (RM) [92, 225], which was originally proposed by

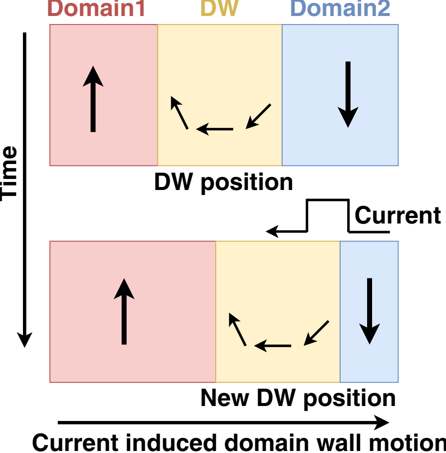


Fig. 25 Spin torque-driven DW motion [34]

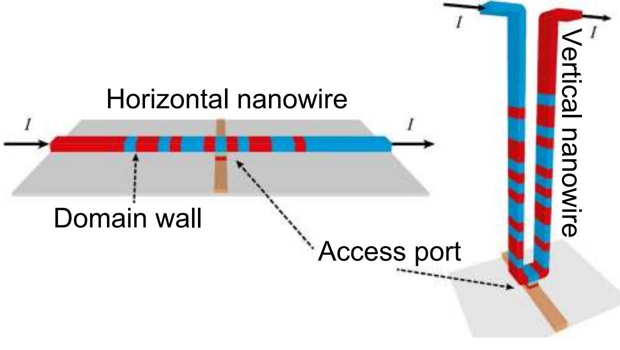


Fig. 26 Horizontal and vertical RM with access port [33]

Table 3 Comparison of RM with HDD Memory [33]

Parameters	RM	HDD
Cell size (F^2)	≤ 2	0.5
Write endurance	$\geq 10^{16}$	$\geq 10^{16}$
Read time (ns)	3–250[a]	2×10^6
Write/erase time (ns)	3–250[a]	2×10^6
Read energy	Low	Medium
Write energy	Low	Medium
Leakage power	Low	Low
Retention period	Years	Years

[a]Including shift latency

Parkin back in 2002 [225], and its working principle was demonstrated in 2008 [220, 226]. RM can be built either horizontally or vertically as 3D "U"-shaped nanowires Fig. 26. In the horizontal arrangement, conventionally, the information is shifted horizontally, whereas the "U"-shaped vertical arrangement of the nanowire is viable due to advancements in 3D fabrication technology. This vertical arrangement is considered as a breakthrough, where a forest of such nanowires is arranged, which tremendously increases the storage capacity in RM. Such an arrangement of RM with large data storage capacity and minimum footprint is advocated to replace the current memory structures at different levels such as SRAM and DRAM cache [220, 227–232], GPU register [233–235], and off-chip (stand-alone) memory [236] owing to its non-volatility, high read/write speed, and lower read/write energy. Diligent efforts needed to investigate the feasibility of replacing the main memory by RM. However, the literature suggests that within a decade, RM is an alternative for the present-day slow secondary memory such as HDD and flash [33, 34, 227, 237, 238]. Table 3 shows the comparison between RM and HDD, which shows that RM is superior to HDD in terms of read/write time and energy. Further, since read/write (storage) and shifting (movement) of these data is achieved with the aid of current pulses, there are no mechanical moving parts in RM, as in the case of HDD. So there is zero physical friction during operation. Hence, RM is expected to last much longer time with high endurance and data retention capacity. Hence, it has been recommended to replace the present secondary memory in the near future [33, 34, 237, 238].

Size of the domain length is not fixed, it could be long or short, and its position depends upon natural pinning sites of the material. In order to fix the length and position of domains, fabrication of the artificial pinning sites is established. These artificial pinning sites are created along the RM by various methods such as by modification of RM size, material property, and edge patterning along the RM edges. This also enhances the stability of DW from external disturbances [124]. Recently, pinning and stabilization of DWs were achieved by developing staggered nanowire structures [239]. RM is read by using MTJ based sensors that employ the concept of TMR. MTJ is placed either in contact [220] or in proximity with RM [240]. Though there are several techniques to write RM such as the self-field effect of current passed along the neighboring nanowires, or by using the fringing fields from the controlled motion of a magnetic DW [240], the STT method is predominantly used [124, 241]. Instead of using separate points for RM read and write operation, a common point known as the access port can be used as depicted in Fig. 26. A low current is used to read the bit stored in the RM, whereas a relatively larger current could be used to switch the magnetization state (write operation) of DW [33]. However, with a single access port, simultaneous read and write operation cannot be performed. Installation of more than one access ports for the RM ensures multiple read and write operations simultaneously, which can increase the operational speed significantly at the cost of the increased complexity of read/write circuits. Recently, a voltage-controlled DW writing (injection) technique is also been investigated for strain-mediated multiferroic heterostructures with good write speed (~ 3.4 ns) and ultra-low energy consumption per write ($\sim 52.48\,\mathrm{mJ/m^2}$) [242]. The main feature of CIDWM is the movement of DW along the direction of electron flow, which is opposite to the flow of current. However, recent experimental observations in ultra-thin multilayer asymmetric PMA nanowire have revealed the movement of DW along the direction of electron flow [243–245]. Further, CIDWM occurs at high speed and low current density [237]. Since these nanowires are structurally different with HM/FM/OM (oxide material) nanowire structure, the explanation for CIDWM due to STT alone does not hold good. Further, DW motion opposite to the electron flow is difficult to be understood. Hence, a new mechanism called chiral spin torque (CST) was proposed, which en-composes an additional torque, i.e., SOT [244, 246–250]. In these systems, DW was driven by the current in ultra-thin PMA nanowires by the combination of

Dzyaloshinskii–Moriya interaction (DMI) and SHE. The DMI is generated in FM materials due to the breaking of symmetry at the HM/FM interface, which gives rise to an effective internal magnetic field. This field locks the chirality of DW to Neel type. Simultaneously, a spin current is generated due to SHE in the HM, which enters into FM exerting Slonczewski-like torque. This torque, in concert with the internal magnetic field due to DMI, favors the movement of DW at high speed and low current density. An attempt is made by Emori et al. [244] to explain the controversial movement of DW opposite to the flow of electrons. Though it is believed that DMI together with Slonczewski-like torque executes the CIDWM in ultrathin multilayer asymmetric PMA nanowire, an additional torque due to the Rashba field has also been noted to be existing [245, 249, 250]. There were several theoretical models developed to describe the role of the Rashba field in CIDWM. However, these models could only explain the DW motion opposite to the electron flow. Hence, a comprehensive role of the Rashba field in DW motion along the electron flow is still under investigation [244]. Recently, a significant breakthrough in RM is achieved by using two coupled synthetic antiferromagnet (SAF) structures, where DW motion is governed by exchange coupling torque (ECT) derived from the exchange field of a much higher magnitude than the DMI field [237, 251]. In this structure, a DW velocity of > 750 m/s has been observed. Further, the SAF structure eliminates the emanating magnetostatic stray fields that would otherwise common with magnetic layers of RM, causing unwanted interaction between DW. One of the major concerns in RM is the threshold current density, which is responsible for DM motion. The minimum threshold current density needed for DW operation with the CST phenomenon is 1.5×10^8 A/cm^2 [246]. Though in the SAF structure, the speed of DW motion improved, there is no reduction in threshold current density. Reduction in threshold current density can be achieved by reducing the defects and roughness of the material, and it is still under investigation [33]. Hence, DW devices are still evolving, and many research groups are working on fundamentals for their real-world technological applications.

2.4 All spin logic device

The discretion that spin current transport dissipates almost zero power dissipation compared to charge current has led the proposal of ASL in 2010 [252]. ASL devices consist of input and output magnets to store the binary information (Fig. 27). A NM channel facilitates spin transportation to the next stage. Isolation layer provides a separation between devices and an interface between the nanomagnets and channel for injecting spin-polarized electrons. Input and output magnets can have two possible stable states, depicted by the left- and right-pointing arrows. When a supply voltage is provided to the input magnet, spin accumulation takes place at the channel entrance inducing a non-equilibrium magnetization. As a result, spin diffusion takes place along the channel, creating a spin current. This spin current (I_{spin}) flows along the channel by transferring angular momentum without charge flow. A positive supply would result in I_{spin} with opposite magnetization as that of the input magnet. Because, during positive supply, those injected electrons from GND, which are having the same spin orientation as that of the input magnet, would be moved toward supply. In comparison, the electrons with the opposite spin direction would be reflected back to the channel. On the contrary, negative supply would result I_{spin} with the same magnetization direction as that of the input magnet. In due course, I_{spin} propagates through the channel and exerts STT on to the output magnet, when it exceeds the switching threshold. As a result of which magnetization direction of the output magnet toggles. Hence, by controlling the polarity of supply voltage, we can either perform inverter or buffer function using the ASL device [37, 252]. One of the important points here is the selection of material and length of the channel. If the channel length is more than spin diffusion length, then spin-flip would take place, hampering the functionality of ASL devices. There are various applications developed using ASL devices such as full adder [254, 255], Boolean logic gates [255–257], and arithmetic logic unit [258]. A detailed review of ASL devices can be found in Refs. [37, 255, 259–261]. It also provides a comparison of realistic microprocessors based on ASL with its CMOS counterpart in terms of system-level power requirements.

2.5 Hybrid magnetic/silicon devices

Recent developments in the field of material science have enabled the development of unique structures, where the advantages of both magnetic as well as silicon-based devices are combined to obtain hybrid magnetic/silicon devices. A novel four-terminal spintronic hybrid magnetic/silicon device (Fig. 28) was proposed in Ref. [262], where

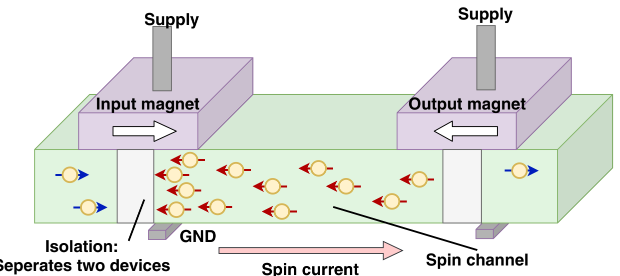


Fig. 27 Schematic of ASL-based inverter [37, 253]

nonlinear transport effect of zener diode (a semiconductor device) and AHE of FM materials were coupled in a single unit. This device possesses a high magnetoresistance (MR) ratio of $2 \times 10^4\%$ at room temperature with a magnetic field of 1mT. It incorporates the advantages of both semiconductor and FM material. It was noted that the MR ratio could be changed by device dimensions of FM material, which can play a crucial role in practical applications developed based on these devices. Furthermore, Boolean logic operations such as AND/NAND and OR/NOR have also been performed, which demonstrate the feasibility of these novel devices to implement LIM circuits.

However, while scaling down the process, a complex four-terminal structural connection mechanism and the application of the stray field lowers the overall performance in the device proposed by Ref. [262]. Further, the material used in the semiconductor (zener diode) to solve the resistor mismatching also limits the sensitivity of the magnetic field. Hence, its improved version, called diode-enhanced GMR structure, which enhances the MR ratio with high magnetic field sensitivity, has recently been developed in Ref. [263] as shown in Fig. 29. With this hybrid magnetic/silicon multilayered structure, a high MR ratio of up to 6947% was reported with a small magnetic field of 50 Oe. A highly reliable, reconfigurable logic structures such as AND and OR have also been implemented and experimentally demonstrated by amplifying the total resistance change of two GMR strips in the different magnetic configurations. These devices are expected to be employed in future LIM architecture to reduce the power dissipation of the circuit and lower data traffic between memory and processor block compared to von-Neuman architecture.

Another novel magnetic device (Fig. 30a) was proposed by coupling the magnetic multilayered structure (magnetic film composed of Ta/CoFeB/MgO), which utilizes AHE and semiconductor materials to employ negative differential resistance (NDR) phenomenon [264]. Using this device, a novel LIM structure was also developed for reconfigurable logic operations such as AND/NAND, OR/NOR. The LIM applications developed with this device are expected to work

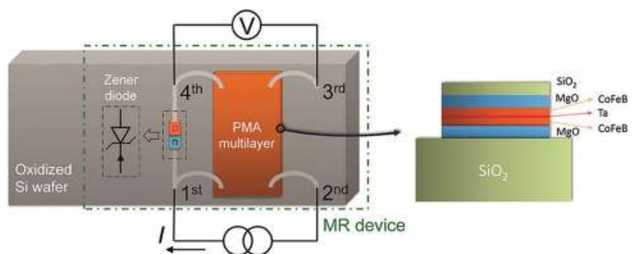


Fig. 28 Schematics of MR device structure, MR measurement setup, and magnetic multilayer. The pin configuration of the zener diode is indicated in the inset [262]

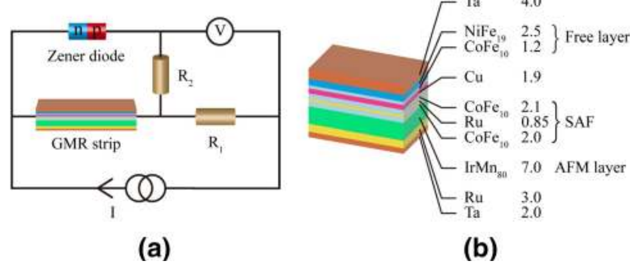


Fig. 29 a Schematics of diode-enhanced GMR structure, which enhances the MR ration up to 6947%. b Multilayered stack of GMR film [263]

at a high speed of GHz range with low energy consumption compared to conventional von-Neumann architecture. However, the high-frequency performance of these LIM structures has not been studied until recently. An attempt is carried out in the literature [265] to investigate the switching speed of LIM structure and found that Ta/CoFeB/MgO multilayers and NDR components can be switched at 42–468 ns range. It is suggested that further reduction in switching speed in this LIM structure is not possible because switching speed depends on the internal resistance of the NDR component. The resistance of the NDR device below 90Ω is not feasible, which corresponds to Shoucair's theory [266]. Hence, a novel spintronic device (Fig. 30b) is proposed, where the NDR semiconductor component is replaced by an insulator-to-metal transition (IMT) material such as VO_2 [265]. LIM structure developed with this found to be having a high switching speed, i.e., 1 to 10 ns, which also produces reliable output (output ratio > 1000%) at low work magnetic field of < 20 mT.

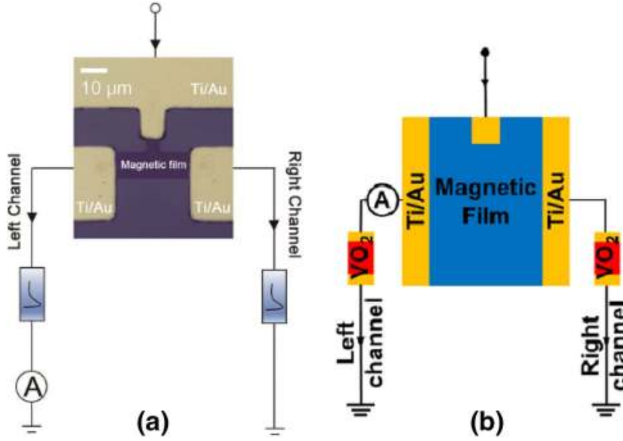


Fig. 30 Schematics of hybrid magnetic/silicon device structures. a Magnetic film (Ta/CoFeB/MgO) is coupled with NDR (Ti/Au) semiconductor [264]. b Magnetic film (Ta/CoFeB/MgO) is coupled with IMT (VO_2) [265]

Recently, a new hybrid magnetic/silicon device called rectified-tunnel magnetoresistance (R-TMR) (Fig. 31) has been constructed with the combination of PMA DI-MTJ and a Schottky diode [267]. A high on/off ratio (> 100) is obtained by suitably manipulating the alternating current (AC) and direct current (DC). Further, a high speed (1 GHz) and low energy (80 fJ) novel LIM scheme has been proposed. Based on the TMR effect and AC/DC regulated capability for reconfigurable logic operations such as AND/NAND, OR/NOR are implemented. This work is expected to promote more practical applications based on LIM structures.

2.6 Skyrmions

Skyrmions was named after Tony Skyrme, a nuclear physicist who studied the concept of nonlinear theory for interacting pions in the early 1960s to reveal that topological stable field configurations do occur as particle-like solutions [268, 269]. Nowadays, a skyrmion is used in different contexts such as elementary particles to the liquid crystal, quantum Hall effect in Hall magnets and Bose–Einstein condensates, to describe similar mathematical objects [270–272]. Though the magnetic skyrmions were reported in 1974 [273], experimental observations were made later in 2009 [272, 274, 275]. DMI is the main mechanism that generates the skyrmions with chiral spin structures, having a vortex-like swirling configuration (Fig. 32), both in bulk and thin films of FM materials. DMI between two atoms having spins S_1 and S_2 is described by Eq. 18,

$$H_{DM} = -\overrightarrow{D_{12}}.(\mathbf{S}_1 \times \mathbf{S}_2), \tag{18}$$

where $\overrightarrow{D_{12}}$ is DMI vector, as shown in Fig. 33, the chiral spins can rotate either along the radius or circumference to form vortex configuration, in FM films with perpendicular anisotropy. The pattern of spin rotation is decided by the DMI vector. Due to the indirect exchange mechanism [277] between 3-site, i.e., between two atomic spins $\mathbf{S}_1$ and $\mathbf{S}_2$ with the neighboring atom having large SOC, interfacial DMI has been predicted [278]. The DMI hence generated is perpendicular to the plane of the triangle, which is made of these three sites. From Fig. 33, we can notice that at the interface between perpendicular plane magnetic anisotropy FM and large SOC material, large perpendicular DMI $\overrightarrow{D_{12}}$ is observed between $\mathbf{S}_1$, $\mathbf{S}_2$, and atom of large SOC material. Beginning from FM state where $\mathbf{S}_1$ parallel to $\mathbf{S}_2$, tilting of $\mathbf{S}_1$ with respect to $\mathbf{S}_2$ by rotating around the $\mathbf{D}_{12}$ is regulated by DMI. The size and speed of the skyrmion are controlled by the ratio of $|D_{12}|$ and exchange coupling. Larger, the value of the ratio represents faster rotation and smaller size of skyrmions.

In B20 MnSi crystal, current-induced rotation of a skyrmion lattice was observed in 2010 [279]. Here, both the magnetic field and a temperature gradient are necessary to initiate and control its rotation [280]. Recently, attempts have been made to calculate the velocity of skyrmions with the correlation of current-induced motion of the skyrmion lattice in MnSi and deviation of the Hall resistivity by Schultz et al. [281]. This study also reveals the fact that the STT mechanism is responsible for the motion of skyrmions,

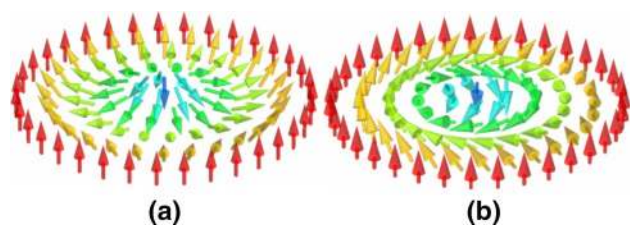


Fig. 32 Skyrmions in a 2D ferromagnet with uniaxial magnetic anisotropy along the vertical axis. **a** Moving along a diameter, the magnetization rotates by 2π around an axis perpendicular to the diameter (**b**) and by 2π around the diameter [276]

Fig. 31 **a** Schematic of the R-TMR device. **b** Stack schematic of PMA MTJ [267]

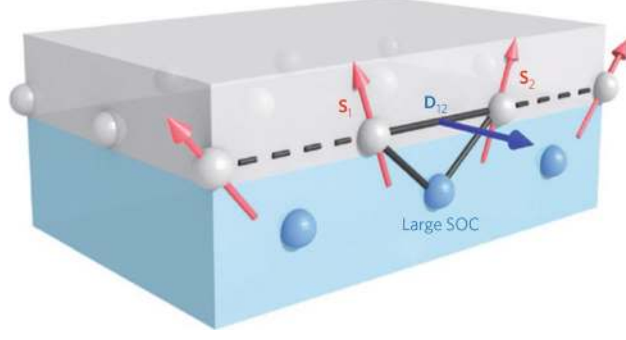


Fig. 33 DMI $\mathbf{D}_{12}$ related to the triangle composed of two magnetic sites ($\mathbf{S}_1$ and $\mathbf{S}_2$) and an atom with a large SOC is perpendicular to the plane of the triangle [270]

which is the same as that for DWs. The current densities needed for the motion of the skyrmions are 10^5 to 10^6 lesser than it would be needed for DWs. This has encouraged to develop magnetic skyrmion based RM. Hence, similar to RM based on DW, magnetic skyrmion based RM can also be used, where information is coded in the skyrmion based magnetic nanoribbon [270, 282–287]. The information density in skyrmion based RM is almost double than that of DW-based RM [274]. But the speed of skyrmions is lesser than DWs for the same current density. The recent experimental results suggest that skyrmions can be moved by SOT [288–290]. However, during the motion of skyrmions along nanoribbon, the skyrmion Hall effect (SKHE) would drive the skyrmions away from the center toward the walls, which leads annihilation [291–293]. Detailed investigation of SKHE and measures to handle it has been discussed in Ref. [294]. Experiments were also being attempted for the generation of skyrmions on demand, in simple FM thin films such as cobalt-based materials, by means of homogeneous DC current and without requiring DMI [295]. Utilizing the current-induced skyrmion motion, recently, attempts were made to develop logical operations [296, 297], skyrmion-based microwave detectors [298], STT nano-oscillators [299, 300], random bit generator [301, 302], and artificial synapses for neuromorphic computing [303], unconventional computing devices [304]. The ultimate miniature size of the skyrmion with the ability to displace it for lower electric current density makes skyrmions as one of the most favorite candidates for several types of spintronic storage and logic devices. Intense research in skyrmions has already triggered an emergence of separate branch, known as skyrmionics [305]. However, the lower speed of skyrmions remains a major concern that needs to be addressed in the future.

3 Conclusion

In this paper, a review of spintronic devices that are expected to become a mainstream technology in future microelectronics is presented. Beginning with different types of spin-valve devices and its working principle, we reviewed conventional MTJs along with recently developed different types of MTJ devices such as DI-MTJ and DMTJ. We described the main characteristics of spintronic devices such as GMR and TMR effects along with different parameters that influence these effects. We have also described various writing techniques adapted for MTJs such as FIMS, TAS, STT, SHE, and VCMA, along with their switching dynamics. Further, we have discussed in detail the pros and cons of each writing technique and steps taken to overcome the cons. Finally, a brief discussion is also presented about the emerging spintronics devices such as DW, ASL devices, skyrmions, and hybrid magnetic/silicon devices, which might help beyond the present-day commercial MRAMs.

In the present-day scenario, conventional CMOS-based devices which utilize charge of the electrons are reaching their limits due to the scaling of technology node, chasing Moore's law. As a result, there is an increase in static power due to leakage, which also increases the overall power dissipation in low-power high-speed portable devices. This is a serious concern that needs to be addressed immediately, to cater to the needs of ever-demanding modern information and communication technology. Spintronic is a whole new paradigm where the spin of an electron is exploited along with its charge. Though the concept of electron spin was realized in the 1920s only, challenges in fabrication technology have hindered the development of spintronic devices and circuits. Spintronic devices hold supremacy in terms of their non-volatility, scalability, ease to read and write, and high endurance over the CMOS devices.

Among all the spintronic devices, MRAMs are considered to be more superior in the memory sector. Plenty of the literature available to elicit that there is much research focused on this area. As mentioned in this paper, successful commercialization of embedded MRAM memory products by the leading spintronic companies is an example to bolster our argument. But one of the main concerns is the speed and energy required for MTJ writing. Though the conventional STT writing technique is simple, the high write current density and lower writing speed due to incubation delay are the biggest hindrances for them to replace the current primary memory technology. To tackle this issue, three-terminal MRAM, which works on SHE, has been explored. MRAMs working on SHE + STT switching principle utilize two types of current, viz., STT and SHE current, and have significantly increased the MTJ writing speed by eliminating the incubation delay. Though this increases the speed of MTJ writing, the concern of energy dissipation remains. The VCMA switching technique is a contemporary method that has promised to address this issue of high energy dissipation during writing. But the still diligent effort is needed to develop materials with large VCMA coefficients at room temperature.

On the other hand, evaluation of RM, which works on the principle of CIDWM, is being advocated for various levels in memory stacks, which includes not only secondary memory (HDD and off-chip memory) but also the main memory such as cache and registers in computer architecture. However, there is a lot of concerns such as current density, bit read, and write speed that needs to be addressed for the RM to be used as main memory. But RM has shown all the potential to be used as secondary memory to replace the current slow, nonvolatile storage within a decade. A lot of research is focused on understanding and utilizing the

recently discovered phenomenon called skyrmions, in nanoelectronic circuits.

Spintronic devices are expected to be utilized not only in the memory sector but also in the recently buzzing new paradigm of normally-off/instant-on computer architecture known as PIM. Here, spintronic devices would also facilitate the processing of information/data apart from storing them. Hence, computational capability is embedded into the memory. There are various hybrid MRAM/CMOS-based circuits that are being investigated to implement this concept and are most promising by nullifying the static power dissipation in standby mode. These hybrid circuits also have a significantly smaller footprint with almost infinite endurance than their CMOS only counterparts. However, the main con of hybrid architecture is the higher delay and considerably high quantum of energy consumed during the MRAM writing process. As explained in this review paper, writing techniques such as SHE + STT and VCMA + STT have addressed this concern to some extent. However, the commercialization of this PIM architecture for low power high-speed circuits is a far-sighted vision, and this idea is still in its early developmental stages. Off late different hybrid magnetic/silicon structures have been proposed with a significantly high MR ratio. Experimental demonstration of reconfigurable logic operations using these hybrid devices for LIM applications has attracted much attention.

It is a challenging task to realize spintronics-based devices for pan electronic circuits in the current scenario. It requires precise knowledge of material engineering, quantum physics, fabrication, and testing methods to build a prototype of spintronic devices. Application of these spintronic devices for memory and hybrid circuits can be developed by modeling these devices using programming languages such as Verilog-A and integrating them with the current CMOS technology with CAD tools like Cadence. But there is a significant gap between simulated models and actual prototypes that were developed. Further, a comprehensive description of spin, spintronics, and their related phenomena, such as spin scattering, spin transfer, spin-wave, and spin–orbital interactions, is still physically and mathematically subtle. At the same time, efforts in materials for thin-film structures which can be engineered artificially are required to increase the speed and lower the threshold current with which the data bits can be manipulated. Hence, the field of spintronics is still in its nascent stage and needs much research both from academia and industry to resolve this gap by exploring new materials for spintronic devices, their fabrication methods along with novel computer architecture to integrate with the present-day microelectronics to develop low-power, high-speed, and high-density circuits.

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