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Spoked-ring microcavities: enabling seamless integration of nanophotonics in unmodified advanced CMOS microelectronics chips

Mark T. Wade[*a], Jeffrey M. Shainline[a], Jason S. Orcutt[b], Rajeev J. Ram[b], Vladimir Stojanović[c]
and Miloš A. Popović[†a]

[a]Department of Electrical, Computer and Energy Engineering, University of Colorado, Boulder, Colorado 80309, USA
[b]Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA
[c]Department of Electrical Engineering and Computer Science, University of California, Berkeley, California 94720, USA

ABSTRACT

We present the spoked-ring microcavity, a nanophotonic building block enabling energy-efficient, active photonics in unmodified, advanced CMOS microelectronics processes. The cavity is realized in the IBM 45nm SOI CMOS process – the same process used to make many commercially available microprocessors including the IBM Power7 and Sony Playstation 3 processors. In advanced SOI CMOS processes, no partial etch steps and no vertical junctions are available, which limits the types of optical cavities that can be used for active nanophotonics. To enable efficient active devices with no process modifications, we designed a novel spoked-ring microcavity which is fully compatible with the constraints of the process. As a modulator, the device leverages the sub-100nm lithography resolution of the process to create radially extending p-n junctions, providing high optical fill factor depletion-mode modulation and thereby eliminating the need for a vertical junction. The device is made entirely in the transistor active layer, low-loss crystalline silicon, which eliminates the need for a partial etch commonly used to create ridge cavities. In this work, we present the full optical and electrical design of the cavity including rigorous mode solver and FDTD simulations to design the Q-limiting electrical contacts and the coupling/excitation. We address the layout of active photonics within the mask set of a standard advanced CMOS process and show that high-performance photonic devices can be seamlessly monolithically integrated alongside electronics on the same chip. The present designs enable monolithically integrated optoelectronic transceivers on a single advanced CMOS chip, without requiring any process changes, enabling the penetration of photonics into the microprocessor.

Keywords: monolithic integration, CMOS photonics, integrated optics, active silicon photonics, modulators, resonators.

1. INTRODUCTION

In the past few years, research in integrated optics has developed promising approaches to fully CMOS compatible photonics. Two main types of integration have emerged: monolithic integration and hybrid integration. In monolithic integration, all devices, both electronic and photonic, are made on a single silicon wafer utilizing a single fabrication flow. In most cases, the laser is the only off-chip component. There remains debate regarding whether the off-chip laser is a viable approach to achieve energy-efficient, high-performance systems [1]. The main strength of monolithic integration is using existing commercially available CMOS processes and fabrication facilities, bypassing the need to flip-chip bond or wafer bond a photonics wafer and an electronics wafer, thus reducing complexity and cost. Another advantage is direct connection of photodiodes to receivers in the CMOS device layer with low capacitance, allowing significantly improved energy efficiency over hybrid methods that may require higher capacitance through silicon vias (TSVs). Hybrid integration offers the advantage of optimizing fabrication for electronics and photonics independently, which typically results in drastic customization from a typical CMOS flow for the photonics chip. However, this

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[*] E-mail: mark.wade@colorado.edu
[†] E-mail: milos.popovic@colorado.edu, Telephone: +1 (303) 492-5304
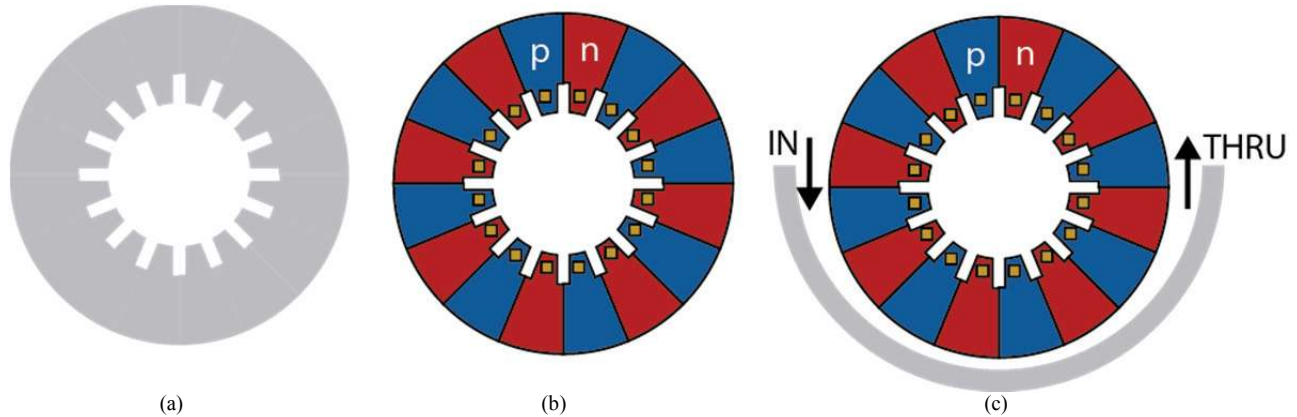
Fig. 1. **Schematic of the spoked-ring microcavity**: (a) passive cavity; (b) formation of interleaved junctions for a modulator, with inner radius vias; (c) extended interaction length input coupler to excite only the fundamental mode.

approach requires some type of bonding between the electronics wafer and the photonics wafer which is both complicated and costly, and inevitably places some separation between the photonic devices and their electronics interfaces, increasing energy cost for the most demanding applications.

In this paper, we focus on the design and implementation of a novel optical cavity mainly aimed towards enabling high quality, active photonics in advanced CMOS processes that utilize the monolithic approach to photonic integration. By "active photonics," we mean photonic devices that require tight optoelectronic integration. Examples are tunable resonators with integrated electrical microheaters that enable tunable filters [2, 3], as well as optical microcavities that include electrically driven semiconductor junctions enabling modulators and detectors. The specific process that we are using is IBM's 45nm SOI12S0 [4]. It is a partially-depleted thin silicon-on-insulator (SOI) CMOS process that has already achieved wide commercial success with IBM's Power7 processor (used in the IBM Watson and Blue Gene/Q supercomputers), the Cell Broadband Engine (used in the Sony Playstation 3 as well as in supercomputing), and the IBM Espresso CPU (used in Nintendo's Wii U game console). Although thin SOI CMOS supports state of the art transistor performance, it presents challenges to a designer interested in implementing active optical devices. This includes an insulator oxide below the active layer that is too thin to confine guided optical modes, various dopants and silicidation steps standard in transistors that introduce optical loss into optical waveguides and resonators, and design rules adapted to Manhattan geometry transistor circuits rather than curvilinear photonics. Previous work has shown that these challenges can be overcome, and that this process supports the basic suite of photonic components needed to enable complex photonic circuits [5, 6].

In Sec. 2, we present the challenges involved in designing photonics in thin SOI microelectronics processes, and we introduce the spoked-ring microcavity as a universal optoelectronic building block that can achieve high performance while staying within the constraints of the process. In Sec. 3, we present the detailed design flow of the spoked-ring optical cavity including mode solver and finite-difference time-domain simulations (FDTD) for the design of the waveguide-cavity excitation geometry and the electrical contacts. In Sec. 4, we present details of integrating photonic devices in a standard microelectronics CAD toolset using a process design kit (PDK) that was intended solely for electronics design.

2. PHOTONICS IN THIN SOI AND THE SPOKED-RING CAVITY

12SOI has a transistor body silicon layer thickness that is <100nm whereas typical custom SOI wafers used for silicon photonics have a device layer thickness of >200nm. Since the process does not have a partial etch, ridge structures that are often used to create optical modulators [7] cannot be made out of the crystalline body silicon. The polysilicon transistor gate, also sub-100nm in thickness, can be patterned atop a crystalline body silicon slab to construct a ridge-like waveguide and was previously shown to enable injection-mode microring modulators [5]. However, the polysilicon in 12SOI is highly optically lossy (order of 100dB/cm) which translates to broad linewidth resonances. This in turn requires injection-mode operation and thus lowers the energy efficiency and speed of modulation. Since the polysilicon is

unusable for applications requiring low optical loss, the optical devices must be made entirely in the thin crystalline body silicon layer. In an SOI process, the crystalline silicon forms the active region (source/drain and channel) of the electrical transistors. Thus, in our approach, electrical circuits and photonic circuits are made in the same physical layer, and they can be tightly integrated on the same silicon die. Working in thin SOI introduces another significant design constraint when designing active photonic components: the set of doping profiles native to the process were designed for transistor performance. This limits the available options for doped optical waveguides and cavities to enable optoelectronic devices. We show that native doping profiles enable efficient optoelectronic devices, eliminating the need for process customization. Finally, efficient optoelectronic devices call for high fill factor carrier plasma modulation. One efficient geometry available in custom photonics processes is a vertical junction [8]. In thin SOI CMOS, the active layer is too thin to support vertical junctions. As a result, lateral junctions with one or more of the dopant concentrations optimized for transistors are what must be used. Recently, a depletion modulator based on a "wiggler-mode" racetrack microcavity, which is compatible with a single-lithographic layer and low-resolution junctions, was demonstrated in bulk CMOS [9]. Some disadvantages of this resonator are its limited Q demonstrated so far, dead regions that ensure imperfect optical field overlap with the junction, and large cavity size which increases junction capacitance and energy consumption. In the following, we introduce an optical cavity that is compatible with SOI CMOS design constraints, and that maximally employs the high mask resolution for dopants made available in a 45nm CMOS process. By enabling implementation in unmodified SOI CMOS, it enables many active optoelectronic applications in microchips that support highly complex circuits with millions of transistors in a modern process.

Figure 1(a) shows a schematic representation of what we have termed the "spoked-ring" microcavity. The width of the ring is wider than the single-mode width, so multiple higher order spatial modes are guided. However, the higher order modes have significant electric field on the inner portion of the ring which has "spoked" electrical contacts that result in high optical loss for those modes, suppressing them by spoiling their Q. When designed properly, the fundamental mode is guided as a whispering-gallery mode, similar to microdisks, and the field does not extend to the inner portion of the ring. Since the fundamental mode does not "feel" the contacts, high-Q resonances are maintained.

One use for the cavity is to create depletion-mode carrier plasma modulators for efficient communication links. Figure 1(b) shows how a depletion modulator can be implemented with this cavity. Lateral junctions are created using interleaved radially extending p and n doped sections. As previously stated, only dopant concentrations that already exist in the process can be utilized. Fortunately, the transistor n-well and p-well dopants have concentrations of ~5e17 cm^{-3} which is sufficient to make modulators and other active devices without accruing too much optical loss. Ideally, the

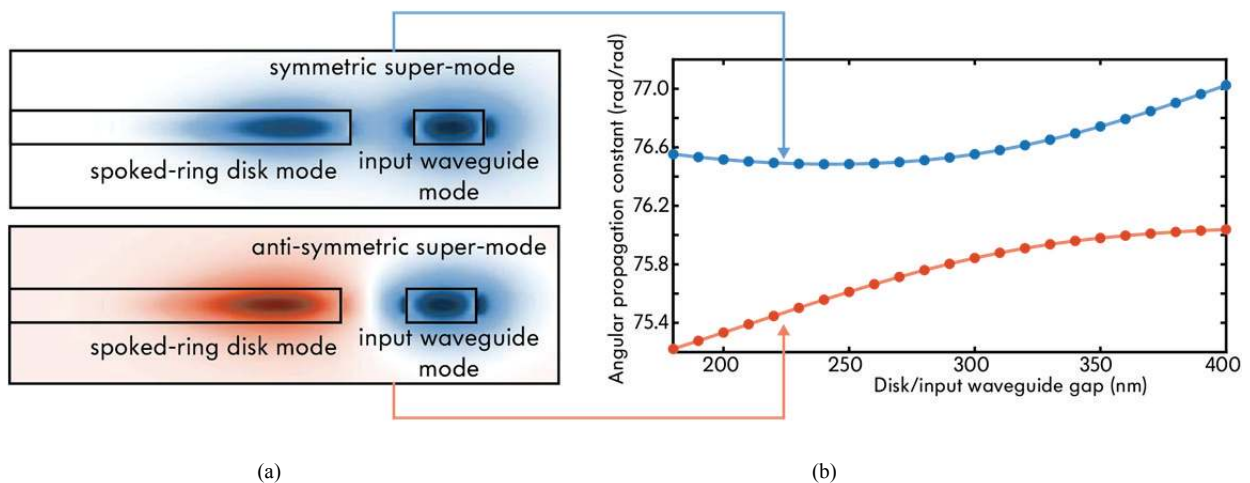(a)   (b)

Fig. 2. **Supermodes of disk/waveguide system** – (a) Spatial electric field mode profiles of the symmetric (top) and anti-symmetric (bottom) supermodes. (b) Angular propagation constant anti-crossing between symmetric and anti-symmetric supermodes. This splitting occurs when there is efficient coupling between the disk and the waveguide indicating phase-matching. Similar plots that vary the outer radius of the disk and the width of the input coupling bus

interleaved junctions would be narrow enough to fully deplete the active regions under reverse bias, thereby introducing the maximum perturbation to the refractive index and achieving the maximum resonance shift for a given voltage. In practice, the design rules for the dopant masks limit the minimum width of the p and n doped sections of the waveguide. For 12SOI, the resolution is ~200nm. This resolution still allows the creation of narrow p and n regions, and a typical design can include >80 junctions. The widest depletion width at reverse bias in typical operation is >150 nm, so a fairly efficient design can be obtained, where over half the cavity sees active carrier density modulation.

Since the cavity is multimode, the optical input coupling of light from the waveguide to the cavity must be carefully designed to avoid excitation of higher order modes. This is achieved by having a long interaction length input coupler which phase-matches the input coupler with the angular propagation constant of the spoked-ring's fundamental mode. The extended interaction length, weak input coupler allows an input excitation in one waveguide to create a long polarization current in the adjacent perturbing waveguide. The spatially extended polarization current then has a small spread in k-space, and thus it selectively excites only the fundamental mode, to which it is well matched in k-space (i.e. in propagation constant). If an output coupler is needed for a specific purpose, the extended coupler does not need to be used since only the fundamental mode is excited in the cavity, and the coupling is single-mode to single-mode. Leaving the resonator, the higher-order-mode excitation is a second order coupling effect, and typically negligible.

The spoked-ring cavity geometry meets all of the constraints of a thin-SOI microelectronics process, and can be seamlessly integrated into existing CMOS processes. In the next section, a design flow for the spoked ring cavity is presented.

3. DESIGN FLOW OF SPOKED-RING CAVITY

The design of the spoked-ring cavity involves a combination of mode solver and FDTD simulations. First, a 2D cylindrical mode solver [10] is used to calculate the geometry of the ring. At this point, a disk supporting whispering-gallery modes is used since the fundamental mode of the disk will be nearly identical to the fundamental mode of the final structure. The bending loss versus radius is calculated to ensure the radiation limited intrinsic Q is high enough to not degrade the performance of the device. Next, a second waveguide, the input waveguide, is included in the mode solver simulations. As with any coupled waveguides, the supermodes of the two-waveguide system are analogous to symmetric and antisymmetric modes, with some deformation because of the curved geometry. The propagation constants of the 'symmetric' and 'antisymmetric' supermodes differ by an amount equal to the coupling between the
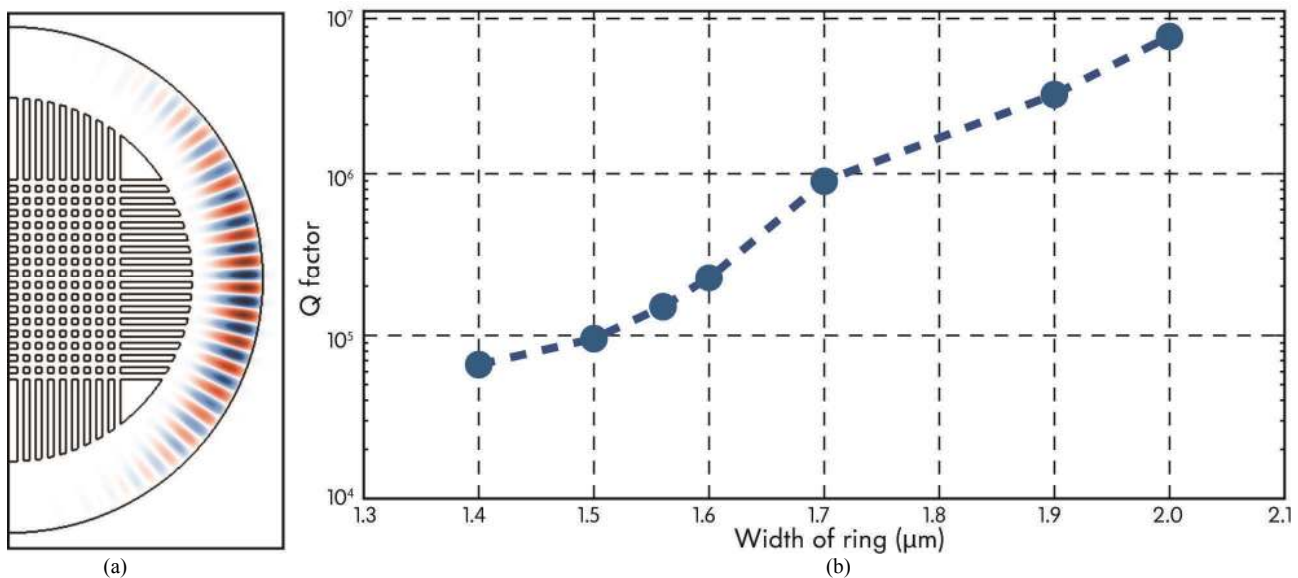

Fig. 3. **Spoked-ring width versus Q** – (a) 3D FDTD simulation showing the fundamental mode avoiding the contacts. (b) Radiation quality factor versus the width of the ring (outer radius fixed at 5μm). As the width decreases, the fundamental mode scatters more light and the Q degrades. Narrowing the ring leads to reduced RC time constants for driving the reverse-biased junctions from the electrical contacts at the inner radius, at the cost of broader linewidth resonances.
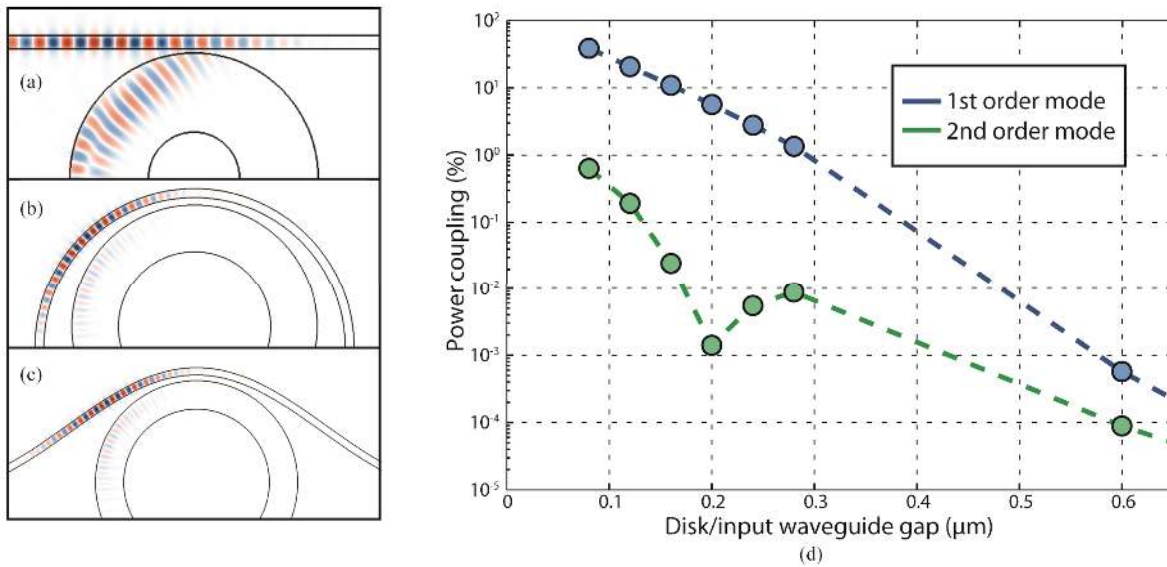
Fig. 4. **FDTD simulations showing various coupling schemes to the spoked-ring cavity** – (a) Point coupling scheme where the input coupling waveguide is straight and is brought in close proximity to the spoked-ring microcavity. This approach excites higher-order modes and is lossy. (b) Phase-matched approach. The input coupling waveguide has a radius of curvature larger than that of the spoked-ring cavity. This approach efficiently excites the fundamental mode and does not introduce significant loss. (c) Sinusoidal-coupler approach. This method still achieves phase matching between the input waveguide and the spoked-ring cavity, and it minimizes straight to bend loss by slowly changing the radius of curvature along the input waveguide. It is also simpler to implement in a layout. (d) Power coupling from bus to ring vs. gap from the FDTD simulation shown in part (c). Coupling to the 1st order mode is about two orders of magnitude stronger than coupling to the 2nd order mode over the range of relevant coupling strengths.

waveguides. With coupled waveguides, the coupling between the two waveguides is efficient only if the propagation constants are matched. The complicating factor is that each waveguide, in addition to coupling, sees a shift in its own 'uncoupled' propagation constant due to presence of the other waveguide [11]. In a pair of straight, symmetric waveguides, the two waveguides see the same self-shift, so a pair of identical waveguides stays matched. With bent waveguides, the angular propagation constants should match to achieve efficient coupling. This is trickier in the cylindrical geometry. First, one must look for dimensions of each of the disk and the wrapping waveguide that give the same propagation constant. However, the self-coupling shifts to the propagation constants of each of the disk and waveguide will now in general be different. Thus, one needs to correct for that to ensure that phase matching has been achieved in the coupled geometry. This could be done by coupled mode theory, but is more directly addressed by solving the coupled system in the mode solver. The angular propagation constant of the supermodes is plotted versus the gap between the microdisk and the input waveguide, while keeping the radii of the disk and the input waveguide constant, in Fig. 2(b), and the anti-crossing shows the gap at which the angular propagation constants match and efficient single-mode excitation occurs. To determine the range of geometries that result in phase-matching and efficient coupling, similar plots are generated that vary the radii and keep the gap constant.

Next, rigorous 3D finite-difference time-domain (FDTD) simulations are run to verify the results from the mode solver simulations and to design the position of the "spokes." To ensure extra loss is not being introduced by the electrical contacts, the fundamental mode is launched into the simulation domain and propagates around the spoked-ring. By calculating the transmission from input to output, the electrical contacts can be placed far enough from the mode to minimize loss. This simulation is shown in Fig. 3. Fig. 3(a) shows that the spokes do not scatter the fundamental mode. Fig. 3(b) shows the radiation quality factor of the resonator as a function of ring width. As expected, the Q decreases as the contacts get closer to the optical mode. For some applications, the designer might choose to be more aggressive with the location of the spokes. For instance, in a modulator configuration, the width of the spoked-ring cavity directly corresponds to the series resistance and the junction capacitance of the diodes. If the spoked-ring cavity width is narrowed, both the resistance and capacitance are decreased which decreases the RC time constant of the diode. At some
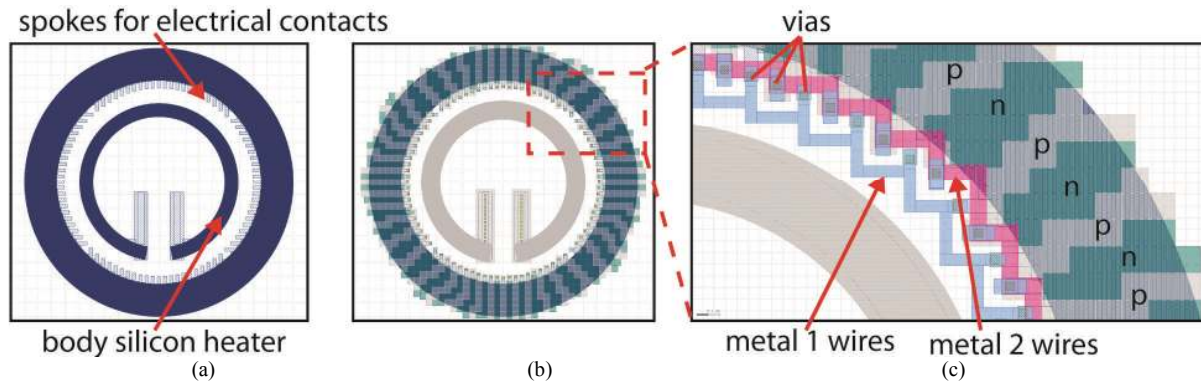
Fig. 5. **Layout of spoked-ring cavity and modulator.** (a) Passive body silicon structure showing the silicon spokes that will be used for electrical contact. The inner circular silicon structure is an integrated heater for thermal tuning. (b) Layout view of the doping shapes to create a carrier-plasma optical modulator. The silicon heater is blanket doped with high concentration dopants to create a low resistance heater that can be driven by on-chip circuits. The p/n regions are discretized to ~200nm grid to meet design rules imposed by the process. (c) Zoom in of the modulator showing a close up of the p/n regions and the electrical wiring. The minimum width and pitch of the metal layers are of critical importance to allow the tightly packed wiring.

point, however, the contacts will introduce loss to the fundamental mode and broaden the resonance. Thus, there is a tradeoff between energy efficiency (related to the linewidth of the resonance) and speed of the device.

Figures 4(a) and 4(b) show snapshots of FDTD simulations comparing a point coupler that excites higher order modes and an extended coupler that only excites the fundamental mode. Figure 4(c) shows a more convenient layout implementation to achieve the phased-matched coupling. As shown in the figures, the extended coupler is critical to achieving a low-loss efficient coupler. To adjust the amount of power coupled from the input waveguide to the spoked-ring cavity, the interaction length can be extended or the gap between the spoked-ring and the input waveguide can be adjusted. Although changing the gap affects the phase matching, FDTD simulations showed that the effect is small for perturbations around a particular design. Thus to arrive at design variants, we adjust the coupling strength with the gap alone which simplifies the layout. Figure 4(d) shows the power coupling to the fundamental mode and the second order mode as a function of the gap between the spoked-ring cavity and the input waveguide, for the design in Fig. 4(c). For typical coupling strengths per unit length, i.e. typical gaps, the total coupling to the fundamental mode is almost two orders of magnitude higher than the unwanted coupling to the second order mode.

Once the cavity is designed, the next step is to implement it in a standard microelectronics CAD flow for this process.

4. ZERO-CHANGE CMOS PHOTONICS

Advanced CMOS processes were developed entirely for electronics. This includes the complex tools that are used to design, synthesize, layout, and verify electronic circuits. For a given process, the designer receives a process design kit (PDK) that contains details of many aspects of the process including transistor models, front end (silicon layers) and back end (metal layers and dielectrics) information, design rules, fabrication mask sets, and the process flow. The entire PDK has been written and developed to be as convenient as possible for circuit designers. This infrastructure presents challenges and needs to be adapted for making customized structures like photonics.

To design an electronic-photonic chip in an advanced process, one must use the existing toolset that has been developed for the electronics industry. Since the IBM 12SOI process is an electronics only process, its PDK provides no guidance on how to make optical structures, and making simple structures is obfuscated by the steps involved in turning a layout (which uses "design" layers) into a mask set. For example, if one simply draws a rectangle of body silicon in the layout, the resulting structure that is fabricated in the 12SOI process will be heavily doped by default, because it is presumed to be part of a transistor. For photonics, additional dopant blocking shapes are added. Many photonic structures involve smooth bends which introduce numerous design rule violations, since the design rule set was developed for electronics which are typically comprised of rectangular shapes. In our early attempts at implementing photonics in advanced CMOS, in this work and e.g. [5,12,13], close communication with foundry engineers was required to ensure that

apparent design rule violations that arise in photonics are artifacts of the electronics oriented PDK and do not introduce manufacturability problems. As silicon photonics becomes more prevalent, it is likely that the advanced processes will officially support photonics in their PDK, and many of these difficulties will be alleviated.

Fig. 5 shows a spoked-ring modulator layout. Fig. 5(a) shows the body silicon structure. This includes the spoked electrical contacts as well as an electrically contacted circular strip of silicon that is doped and used for thermal tuning. The mask shapes that form the p/n regions are shown in Figs. 5(b) and 5(c). Figure 5(c) shows a close-up of the p/n junctions and the wiring between the many p/n regions to connect all p shapes together and all n shapes together.

This microcavity was employed to demonstrate the first depletion mode modulators realized in an unmodified CMOS process [14]. The first generation of devices demonstrated 5 Gbps operation with a -3 to +0.6V drive voltage swing, and 40 fJ/bit energy consumption. For monolithic photonic-electronic integration in advanced CMOS, the spoked-ring cavity was shown to meet all of the constraints imposed by the process, and it opens the door to designing complex photonic-electronic systems.

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