# SRAM Cell Design for Stability Methodology

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**Abstract**

SRAM stability during word line disturb (access disturb) is becoming a key constraint for $V_{DD}$ scaling [1]. Figure 1 illustrates the access disturb mechanism. In this paper we present a design methodology for SRAM stability during access disturb. In this methodology, the SRAM Access Disturb Margin (*ADM*) is defined as the ratio of the magnitude of the critical current to maintain SRAM stability ($I_{CRIT}$) to the sigma of $I_{CRIT}$. Using *ADM* as a figure of merit, this methodology enables one to project the cell stability margin due to process variations, e.g. $V_T$ variation, during design of a SRAM cell. Using statistical analysis, the required stability margin for an application requirement such as array size and available redundancy can be estimated. Direct cell probing and array test can be used to verify that the stability target is met.

**SRAM Stability Margin Parameter**

Static [voltage] noise margin, as measured by the opening in the butterfly curve (Fig. 2) has often been used as a metric for SRAM stability [2]. Two drawbacks of the static noise margin are the inability to measure it with automatic inline testers and the inability to generate statistical information on SRAM fails. Alternatively, the SRAM "N-curve" [3] provides a way to satisfy both needs. Inline parametric testers can measure the voltage and the current on one internal node of the same test structure used for the butterfly curve. Measured and simulated N-curves with both the word line and bit line held at $V_{DD}$ are shown in Figures 3 and 4. In Fig. 4, intercept 1 is determined by the SRAM pull down to transfer ratio (SRAM $\beta$ ratio), while intercept 2 is related to the pull down to pull up relative strength (inverter $\beta$ ratio). With the bit line held at $V_{DD}$ , if intercept 1 crosses intercept 2 when the word line turns on, the SRAM cell flips; making the cell unstable during word line disturb. The delta between intercept 1 and 2 can thus be interpreted as the static noise margin, or the critical voltage to maintain the SRAM stability ($V_{CRIT}$). One can also characterize the cell stability by the peak current ($I_{CRIT}$), or the total area of the "barrier height" between intercept 1 and 2 in the unit of power ($P_{CRIT}$). As seen in Fig. 4, all three measures of stability are degraded when process variation is included in the simulation. We have confirmed by a Monte Carlo simulation that bits that fail due to $V_T$ variation have margin parameters equal to zero. Figure 5 and 6 show $P_{CRIT}$ and $I_{CRIT}$ as a function of $V_T$ variations of the individual transistors in an SRAM. Note that in Fig. 6, $I_{CRIT}$ has a relatively linear relationship with $V_T$'s. To enable linear analysis and extrapolation, we chose $I_{CRIT}$ as the margin parameter.

**SRAM Design for Stability Methodology**

To obtain the stability margin, we start with the canonical form:

$$\delta I_{CRIT} = \sum_i \frac{\partial I_{CRIT}}{\partial x_i} \delta x_i , \qquad (1)$$

in which $x_i$ can be any parameter whose variation is of interest. In this work we focus on the $V_T$ variation as the first order effect ($x_i$=$V_{T,i}$). We find that no specific $V_T$ correlation between transistors in an SRAM cell best describes the data, but one should note that some correlation could be expected depending on the cell layout details. The total variation of the margin parameter is given by:

$$\sigma_{I_{corr}} = \sqrt{\sum_i \left( \frac{\partial I_{CRIT}}{\partial x_i} \sigma_{x_i} \right)^2} \quad \text{, and } ADM = \frac{I_{CRIT}}{\sigma_{I_{corr}}} . \qquad (2, 3)$$

Figure 7 illustrates the concept in a two-dimensional plot. In Fig. 7, the dotted lines represent the probability contours, and the solid lines represent the margin parameter as a measurement function. The portion of the distribution with margin less than 0 is considered unstable. The number of unit vectors from point A (the nominal point) to point B (the tangential point) gives the *ADM* in the unit of sigma. If the margin parameter is a completely linear function of the $V_T$'s, (3) is an exact measure of the number of sigmas in the distribution. To verify the theory, one can either simulate the N-curve or apply direct SPICE simulation along the path from A to B. Indeed, Table 1 shows excellent agreement between both simulations with time-domain circuit simulation failing right after point B. Due to the linear behavior of $I_{CRIT}$, the *ADM* predicted by (3) is within 5% of the simulations along the path from A to B.

As a design guideline, a look-up table can be generated by assuming that the $V_T$ distribution is Gaussian and the failing bits follow a Poisson distribution. Table 2 prescribes the relationship between the required *ADM*, the array size, the stability-limited yield, and the required redundancy. As an example, a chip with 1M array without redundancy will need an *ADM* of 5.2 for 90% stability-limited yield. Table 3 shows an example of using the proposed *ADM* methodology for design iteration. One can quickly assess the stability using *ADM* by adjusting SRAM design parameters. Using Tables 2 and 3, one can decide between design solutions and technology solutions to satisfy a final product stability requirement.

**SRAM Stability Verification**

The designed SRAM stability can be verified by the $I_{CRIT}$ distribution in parametric test as shown in Fig. 8. The center and the spread of the distribution give the *ADM* of the cell. The proposed methodology is confirmed by the strong correlation of the $I_{CRIT}$ and the pull-down $V_T$ mismatch (Fig. 9). Parametric test provides the advantages of feedback early in the BEOL processing and diagnosis of layout sensitivities. However, this measurement can not be performed on an array and thus does not capture the within array variation.

A desirable functional test technique should provide the flexibility for stability test at a small functional block so one can increase the block size as the yield improves. Lower $V_{DD}$ increases the sensitivity to stability fails, but for small arrays the required $V_{DD}$ reduction creates peripheral circuit fails. This problem can be overcome by suppressed array $V_{DD}$ test. Lowering only the array $V_{DD}$ creates the maximum disturb because the storage charge is reduced while the disturb voltage is kept constant. Figure 10 shows the characteristics of stability fails in a 0.5M SRAM block. The good agreement between the measurement and the Monte Carlo simulation is another confirmation of the proposed *ADM* methodology. To extract the SRAM stability margin from Fig. 10, one should note that the y-axis intercept, where $V_{DD,array}$=$V_{DD,peri}$, is an indication of the *ADM*.

**Conclusion**

We present a methodology that enables the design and verification of SRAM cells for stability. In this methodology, we define a figure of merit for stability, the Access Disturb Margin (*ADM*). $I_{CRIT}$ is used as the critical parameter due to its linear behavior with respect to $V_T$ variation. The *ADM* is defined as the ratio of the magnitude of $I_{CRIT}$ to the sigma of $I_{CRIT}$. The methodology is demonstrated by considering the effect of $V_T$ variation on word line disturb. One can apply the same methodology to account for other process variations and other SRAM parameters of interest such as write-ability. This methodology also provides a standard for communication between designers and technologists, easing the optimization of a solution for an SRAM application.

**References**

[1] D. Burnett, VLSI Symposium 1994
[2] A. Bhavnagarwala, JSSC, April 2001
[3] For example, US Patent 6,341,083

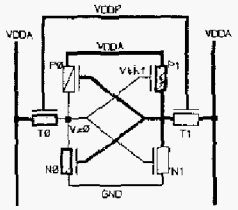


Figure 1. SRAM access disturb mechanism: transistors N0, N1, T0, and P1 have first order effect on cell stability when node $V_{Z0}$ is at ground. Cell flips when $V_{Z0} > V_{TH1}$.

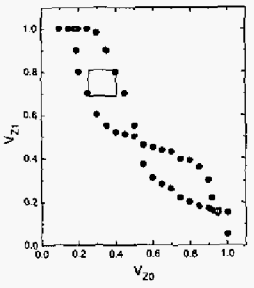


Figure 2. SRAM butterfly curve

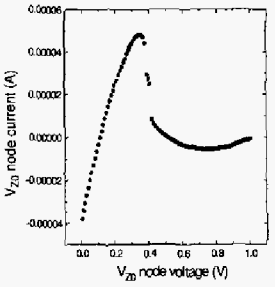


Figure 3. SRAM N-curve (25C)

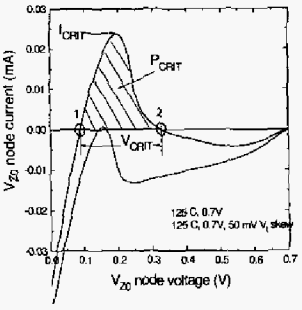


Figure 4. Simulated SRAM N-curve with and without $V_T$ variation and the definitions of the stability parameters.

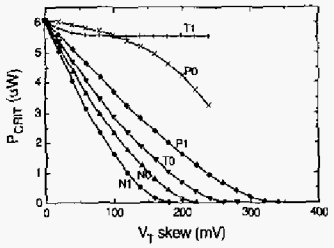


Figure 5. Simulated $P_{CRIT}$ as a function of individual device $V_T$ variation. Transistor naming convention follows Fig. 1.

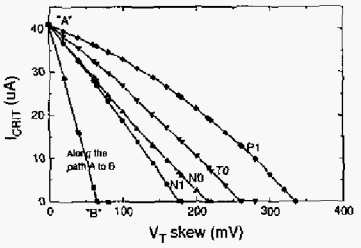


Figure 6. Simulated $I_{CRIT}$ as a function of individual device $V_T$ variation. Also shown is $I_{CRIT}$ simulated along the path from A to B in Fig. 7.

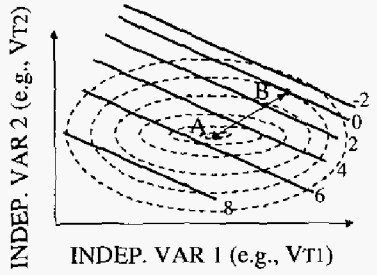


Figure 7. Two-dimensional illustration of the probability distribution and the measure function.

| ADM | Float BL | Col(ff) | Analysis | Comments |
|---|---|---|---|---|
| 4.45 | No | Don't care | ADM method | BL biased to Vdd directly |
| 4.86 | No | Don't care | ADM method | BL connected to Vdd thru equalizer |
| 4.86 | No | Don't care | Time-domain SPICE | BL connected to Vdd thru equalizer |
| 4.89 | Yes | 102 | Time-domain SPICE | BL connected to Vdd thru equalizer |
| 5.05 | Yes | 51 | Time-domain SPICE | BL connected to Vdd thru equalizer |

Table 1. Comparison of the SRAM stability margin by the *ADM* method and by time-domain SPICE simulation. All simulations are performed at fast-fast corner. The *ADM* methodology accurately reflects the BL resistance effect. Due to its DC nature, the *ADM* methodology does not reflect the BL capacitance effect.

| SRAM stability margin due to Vt variation | Maximum SRAM size in a chip w/ yield target 90% | Redundancy bits needed for 1M array w/ 90% yield target | Redundancy bits needed for 10M array w/ 90% yield target |
|---|---|---|---|
| 3 | 77 | ~1400 | ~ 14000 |
| 3.5 | 437 | ~ 250 | ~ 2400 |
| 4 | 3.2K | 38 | ~ 330 |
| 4.5 | 30K | 6 | 42 |
| 5 | 350K | 1 | 5* |
| 5.2 | 1M | 0 | 2 |
| 5.5 | 5.3M | 0 | 1 |
| 6 | 102M | 0 | 0 |
| 6.5 | 2.5B | 0 | 0 |

*90% of the time, 5 or fewer bits are bad | DJF/BW/CW

Table 2. An example look-up table for *ADM*-based design trade-offs that correlated *ADM*, array size, yield, and redundancy.

| ADM | Example SRAM at 90% yield | Vdd (V) | Model corner | Temp (C) | Design option w.r.t. reference cell |
|---|---|---|---|---|---|
| 4.33 | | 0.7 | TT | 125 | |
| 4.33 | | 0.65 | FF | 125 | |
| 4.61 | | 0.7 | FF | 125 | NFET Vt + 55 mV |
| 4.82 | | 0.85 | FF | 125 | Increase pull-down NFET width by 0.04 |
| 4.96 | | 0.7 | FF | 125 | Half BL length |
| 5.24 | > 1 M | 0.7 | TT | 125 | NFET Vt + 55 mV |
| 5.59 | > 5 M | 0.7 | FF | 125 | NFET Vt + 110 mV |
| 6.07 | > 100 M | 0.7 | TT | 125 | NFET + 110 mV |
| 7.54 | > 10 G | 1 | 0.5 | 25 | |

Table 3. Design exercise of SRAM stability using *ADM* methodology. One can obtain quick feedback on design sensitivity such as device width, transistor $V_T$, etc.

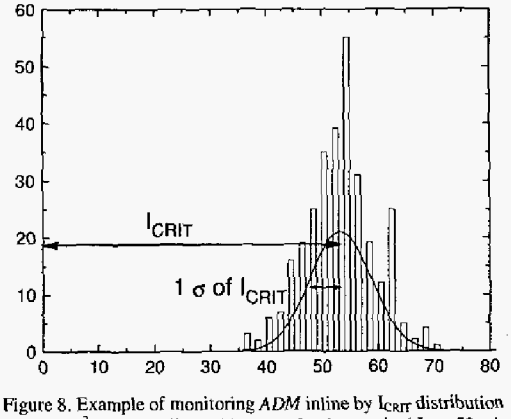


Figure 8. Example of monitoring *ADM* inline by $I_{CRIT}$ distribution for a 1 $m^2$ SRAM cell. In this example, the nominal $I_{CRIT}$ 53 A and the variation is 6.52 A gives *ADM* ~ 8 (room temperature).

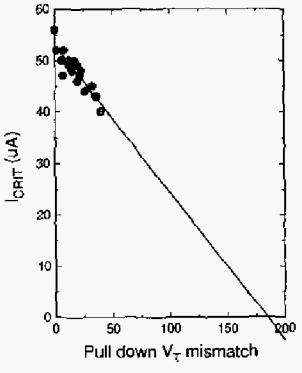


Figure 9. Correlation between $I_{CRIT}$ and pull-down $V_T$ mismatch.

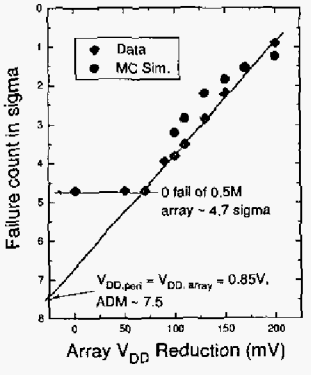


Figure 10. Comparison of array test and Monte Carlo simulation, and extracting the *ADM* from the suppressed $V_{DD}$ array test.