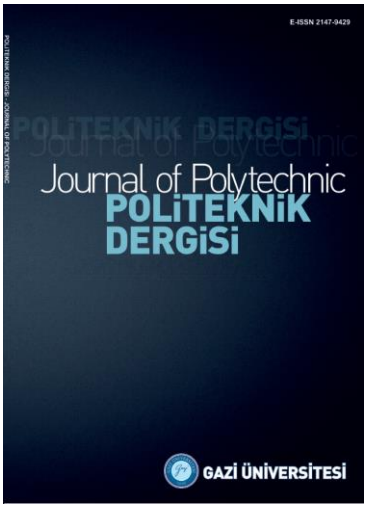

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SRF based output voltage control of 3-Level 3-Phase 4-Leg AT-NPC inverter

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SRF Based Output Voltage Control of 3-Level 3-Phase 4-Leg AT-NPC Inverter

Araştırma Makalesi / Research Article

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ABSTRACT

This paper proposes a synchronous reference frame (SRF) based high performance output voltage controller for the 3-level 3-phase 4-leg (3P4L) advanced T-type neutral point clamped (AT-NPC) inverter operated in stand-alone mode. 3-phase inverters for stand-alone operation are required to provide 3-phase balanced nominal voltage under different load types such as unbalanced linear and non-linear loads. 3P4L inverters working with these types of load allow controlling zero sequence voltage by additional fourth leg. The main contribution of this work is the control of the 3-level 3P4L AT-NPC inverter with an LC-type filter modeled based on the output voltage and capacitor current feedback in the synchronous coordinate system. According to obtained capacitor current decoupled model, double loop PI controller is adopted to control the output voltage of the inverter. An inner capacitor current feedback loop is employed to provide fast dynamic response and active damping of the capacitor current. Finally, transient and steady state operation performance of the controller have been tested with PSIM simulation studies considering different load types. Simulation results validate that the proposed SRF based double loop PI controller ensure high dynamic response and high quality output voltage with less than 3% total harmonic distortion (THD) value for the 3-level 3P4L AT-NPC inverter.

Keywords: 3-level, 4-leg, AT-NPC inverter, carrier-based PWM, voltage control.

3-Seviyeli 3-Fazlı 4-Kollu AT-NPC Eviricinin SRF Tabanlı Çıkış Gerilimi Denetimi

ÖZ

Bu çalışma bağımsız modda çalışan 3-seviyeli 3-fazlı 4-kollu (3P4L) gelişmiş T-tipi nötr noktası bağlantılı (AT-NPC) evirici için senkron referans yapı (SRF) tabanlı yüksek performanslı çıkış gerilim denetleyicisi önermektedir. Bağımsız işletim için 3-fazlı eviriciler, dengesiz doğrusal ve doğrusal olmayan yükler gibi farklı yük türleri altında 3-fazlı dengeli nominal gerilim sağlamak zorundadır. Bu tür yüklerle çalışan 3P4L eviriciler, ilave dördüncü kol tarafından sıfır sıralı gerilimi kontrol etmeye izin verirler. Bu çalışmanın ana katkısı, senkron koordinat sisteminde çıkış gerilim ve kondansatör akım geri beslemesine dayalı olarak modellenmiş LC tipi filtreye sahip 3-seviyeli 3P4L AT-NPC eviricinin kontrol edilmesidir. Elde edilen kondansatör akımı ayrıştırılmış modele göre, eviricin çıkış gerilimini kontrol etmek için çift çevrimli PI denetleyicisi adapte edilmiştir. Hızlı dinamik cevap ve kapasitör akımının aktif sönümlenmesi için kapasitör akım geri beslemeli bir iç döngü kullanılmıştır. Son olarak, denetleyicinin geçici ve kararlı durum çalışma performansı, farklı yük türleri dikkate alınarak PSIM benzetim çalışmaları ile test edilmiştir. Benzetim sonuçları, önerilen SRY tabanlı çift döngülü PI denetleyicinin, 3-seviyeli 3P4L AT-NPC evirici için %3'den daha düşük toplam harmonik bozulma (THD) değerine sahip yüksek dinamik cevap ve yüksek kaliteli çıkış gerilimi sağladığını doğrulamaktadır.

Anahtar Kelimeler: 3-seviye, 4-kol, AT-NPC evirici, taşıyıcı tabanlı PWM, gerilim kontrolü.

1. INTRODUCTION

Inverters have been widely used in many power electronics applications, such as uninterruptable power supply (UPS), renewable energy systems and electrical vehicle, which need converting DC power to AC power. In several 3-phase inverter applications, 3-phase 4-wire (3P4W) inverters are employed to supply 1-phase, unbalanced and non-linear loads [1], [2]. In 3-phase inverter applications, these load types result in zero sequence voltage and current. To handle zero sequence current, conventional split DC-link capacitors can be used at the DC side of 3P4W inverter. In this case, neutral current flows throughout the DC-link capacitor, which requires huge capacitance to handle the neutral current [3]. Another way to obtain neutral point for the zero sequence current in 3P4W inverter is that a delta/star or delta/zigzag connected transformer is used at the load side. However, this is not chosen in many applications because of transformer's dimensions, losses and cost [2]. Therefore 3-phase 4-leg (3P4L) inverter, generated with an additional fourth leg (or neutral leg), is employed in 3-phase applications to provide neutral connection and to control zero sequence voltage.

Other challenging tasks for today's inverter applications are high efficiency, low complexity and low cost. Even though the complexity and cost concerns are partially satisfied with 2-level topology, low efficiency and high filter requirements are disadvantages for this topology.

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For these disadvantages, 3-level topologies are a good solution. Among the 3-level topologies, neutral-point clamped (NPC) inverter is well-known topology and widely preferred in industrial applications [4], [5]. The classical 3-level NPC topology is widely used for medium voltage applications. Because it is necessary to place switching devices in series in the topology, higher conduction losses occur due to the increase in these devices in the conduction path. Another type of the NPC topology is T-NPC, which is more convenient for low-voltage applications and more efficient than the NPC inverter [6], [7]. Compared to the 3-level NPC topology, the T-NPC employs an active bidirectional switch to the dc-link voltage midpoint and gets along with two diodes less per bridge leg. The T-NPC topology combines the positive aspects of the 2-level converter such as low conduction losses, small part count and a simple operation principle with the advantages of the 3-level converter such as low switching losses and high output voltage quality [4]. In T-NPC topology, a bidirectional switch at the midpoint leg is formed by using two conventional insulated gate bipolar transistors (IGBTs) with two antiparallel diodes. Power dissipation in these switches is high since there are two semiconductors in the current path as an IGBT and a diode at the midpoint leg. On the other hand, a bidirectional switch can be designed with only two RB-IGBTs, which do not require diodes [8]. The disadvantage of the T-NPC topology can be removed using an AT-NPC topology due to the employment of the highly efficient RB-IGBT at the midpoint leg. The advanced type of T-NPC (AT-NPC) was proposed in literature with high efficiency and reliability [9]. Because of these advantages, 3-level 3P4L AT-NPC inverter structure, whose detailed analysis and principles are excluded from the scope of this study, is employed with the LC-type filter as in Figure 1. As can be shown in the figure, the additional fourth leg is employed to provide neutral point for 1-phase loads and to control zero sequence voltage under unbalanced or non-linear load conditions.

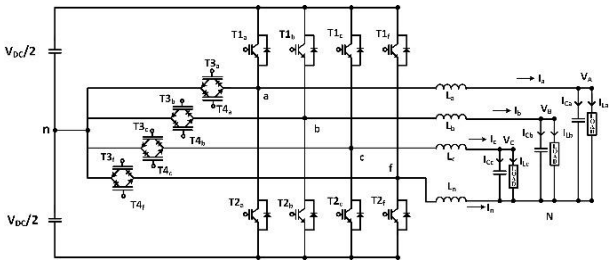

Figure 1. 3-level 3P4L inverter structure

To control the 3-level 3P4L AT-NPC inverter system with low total harmonic distortion (THD) under 1-phase/3-phase, linear/non-linear and balanced/unbalanced load types, double-loop proportional-integral (PI) controller is designed in this study. Although, PI controller has the advantages such as widely used and easy to implement, it does not enable to track sinusoidal reference signal and has not enough controller band width to satisfy high dynamic response in inverter applications. For these reasons, double-loop PI controller based on coordinate transformation in synchronous reference frame (SRF) [10] is used to eliminate steady-state error [11], [12]. In multi-loop based voltage control, either output filter inductor or output filter capacitor current is sampled for inner current loop variable to obtain fast transient response in literature. In reference [13], different feedback and feedforward multi-loop voltage control of 2-level 3-phase 3-leg inverter for the capacitor and the inductor currents feedback are analyzed and it indicates that capacitor current based control is the superior performance. Moreover, reference [14] proves that capacitor current based model is more independent of load variation than inductor current based. Therefore, in this paper, capacitor current based control is adopted as in reference [15] to control 3-level 3P4L AT-NPC inverter with high controller bandwidth and low THD under aforementioned load types.

2. MODELING AND OUTPUT VOLTAGE CONTROL OF THE INVERTER

A proper model of the inverter system should be obtained to achieve high performance output voltage control. The switching-model can represent detailed dynamics and characteristics of the inverter. However, the average-model of the inverter system is more ideal than the switching-model for controller design employed in this study, because the switching-model contains the non-linear structure of the power switches. For the proposed system given in the Figure 1, output voltages (v_{jf}), pole voltages (v_{jn}) and offset voltage (v_{fn}) can be written as:

$$v_{jn} = \frac{E}{2} d_j \tag{1}$$

$$v_{jf} = v_{jn} - v_{fn} = \frac{E}{2}\left(d_j - d_f\right) = \frac{E}{2} d_{jf} \tag{2}$$

where $j \in \{ a, b, c \}$ and d_j is duty ratio of each leg that range from 0 to 1. According to Eqs. (1) and (2), matrix form of output voltage can be expressed as:

$$\begin{bmatrix} v_{af} \\ v_{bf} \\ v_{cf} \end{bmatrix} = \frac{E}{2} \begin{bmatrix} d_{af} \\ d_{bf} \\ d_{cf} \end{bmatrix} \tag{3}$$

From the Figure 1, Eqs. (4)-(6) can be easily written using the Kirchhoff voltage and current laws.

$$L \frac{d}{dt} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = L_n \frac{d}{dt} \begin{bmatrix} I_n \\ I_n \\ I_n \end{bmatrix} - \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} + \frac{E}{2} \begin{bmatrix} d_{af} \\ d_{bf} \\ d_{cf} \end{bmatrix} \tag{4}$$

$$\frac{d}{dt} \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \frac{1}{C} \begin{bmatrix} I_{Ca} \\ I_{Cb} \\ I_{Cc} \end{bmatrix} \tag{5}$$

$$I_a + I_b + I_c = -I_n \tag{6}$$

where V_{AN}, V_{BN}, V_{CN} are capacitor voltages, I_a, I_b, I_c are filter inductor currents, I_n is neutral filter current and filter inductors L_a, L_b, L_c have same value L.

The obtained time-varying *a-b-c* coordinate model is transformed to *d-q-0* coordinate (SRF) by using T_T matrix and Eq. (8).

$$T_T = \frac{2}{3}\begin{bmatrix} \cos(wt) & \cos(wt-\frac{2}{3}\pi) & \cos(wt+\frac{2}{3}\pi) \\ -\sin(wt) & -\sin(wt-\frac{2}{3}\pi) & -\sin(wt+\frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (7)$$

$$T_T \frac{dX_{a,b,c}}{dt} = T_T \frac{dT_T^{-1}}{dt} X_{d,q,0} + \frac{dX_{d,q,0}}{dt} \quad (8)$$

Using Eqs. (4)-(6) with Eqs. (7), (8), SRF based model of the inverter is obtained as:

$$\frac{d}{dt}\begin{bmatrix} I_d \\ I_q \\ I_0 \end{bmatrix} = \frac{E}{2} G \begin{bmatrix} d_d \\ d_q \\ d_0 \end{bmatrix} - G \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} + w \begin{bmatrix} I_q \\ -I_d \\ I_0 \end{bmatrix} \quad (9)$$

$$\frac{d}{dt}\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = w \begin{bmatrix} v_q \\ -v_d \\ 0 \end{bmatrix} + \frac{1}{c}\begin{bmatrix} I_{Ca} \\ I_{Cb} \\ I_{Cc} \end{bmatrix} \quad (10)$$

$$G = \begin{bmatrix} 1/L & 0 & 0 \\ 0 & 1/L & 0 \\ 0 & 0 & 1/(L+L_n) \end{bmatrix} \quad (11)$$

In the above model, it can be concluded that *d*-channel and *q*-channel have capacitor current cross coupling terms with wCV_q, $-wCV_d$ and have inductor voltage cross coupling terms with $-wLI_q$, wLI_d. The state-space model including the cross coupling terms can be obtained as Eq. (12);

$$[\dot{I}_d\ \dot{V}_d\ \dot{I}_q\ \dot{V}_q]^T = A * [I_d\ V_d\ I_q\ V_q]^T + B * [D_d\ D_q]^T$$
$$[V_d\ V_q]^T = C * [I_d\ V_d\ I_q\ V_q]^T \quad (12)$$

In Eq. (12), the model has $4x4$ state matrix (A) and output matrix (B) and has $4x2$ input matrix (C), moreover; it has four transfer functions v_d/d_d , v_q/d_q, v_d/d_q, v_q/d_d, the last two of which are coupling transfer functions. If the channels can be coupled completely, the coupling transfer functions would be zero. To simplify the controller design, the decoupling of inductance voltage terms is omitted, because the effect of it is little. Additionally, capacitor current decoupling terms can be added to capacitor current references for the decoupling. Hence the capacitor current based state-space model can be simplified as in Eq. (13);

$$\begin{bmatrix} \dot{I}_c \\ \dot{V}_c \end{bmatrix} = \begin{bmatrix} -1/RC & -1/L \\ 1/C & 0 \end{bmatrix}\begin{bmatrix} I_c \\ V_c \end{bmatrix} + \begin{bmatrix} V_{dc}/2L \\ 0 \end{bmatrix} D_{dq0}$$
$$V_{dq0} = [0 \quad 1]\begin{bmatrix} I_c \\ V_c \end{bmatrix} \quad (13)$$

,where R represents output load impedance, D_{dq0} represents duty ratio of each channels. The inverter produces the output voltage based on reference signals (v_d^*, v_q^*, v_0^*). The reference signals for the reactive and zero components of the output voltage (v_d^*, v_q^*) are set to zero, thus the reactive and zero components of the output voltage are regulated to zero. Therefore, only the active component (v_d^*) contributes to the actual output voltage. According to this simplified model, PI controller is employed in outer closed-loop voltage control for each channel in the control structure. Although zero steady-state error is achieved with integrator of the outer voltage loop, control bandwidth is so low that cause slow transient response under unbalanced voltage and load disturbance. To improve performance of the controller, inner closed-loop current feedback is employed with proportional gain. The outputs of the proportional controller are transformed to *a-b-c* coordinate and used as each phase's line to neutral reference voltages (v_{af}^*, v_{bf}^* , v_{cf}^*) as can be seen in Figure 2.

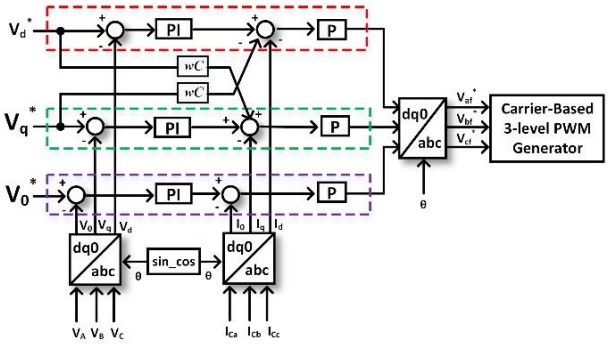

Figure 2. SRF based proposed control block diagram

In Figure 3, double loop voltage control strategy is given. In there, $G_{VC}(s)$ is outer loop voltage controller transfer function, $G_{CC}(s)$ is inner loop current controller transfer function and $G_p(s) = H_i(s) * H_v(s)$ is simplified plant transfer function, where C is capacitance of the filter, L is inductance of the filter and R is equivalent resistance of the filter inductance.

$$G_{VC}(s) = K_{p1} + \frac{K_I}{s} \quad (14)$$

$$G_{CC}(s) = K_{P2} \quad (15)$$

$$G_p(s) = H_i(s) * H_v(s) = (\frac{1}{sC})\ (\frac{\frac{4}{LC}sC}{s^2 + \frac{1}{RC}s + \frac{1}{LC}}) \quad (16)$$

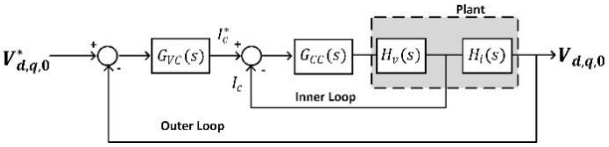

Figure 3. Double loop voltage control strategy

The controller parameters are designed according to requirements of stability and high dynamic response. In voltage loop, the gain K_{p1} and K_I are obtained as 0.8 and 30, respectively. In current loop, the gain K_{p2} is obtained as 60. Using these parameters, the frequency response of the open loop voltage control system with the controllers is given in Figure 4. It shows that the gain and phase margin are sufficient to fulfill the requirement of high dynamic response and stability.

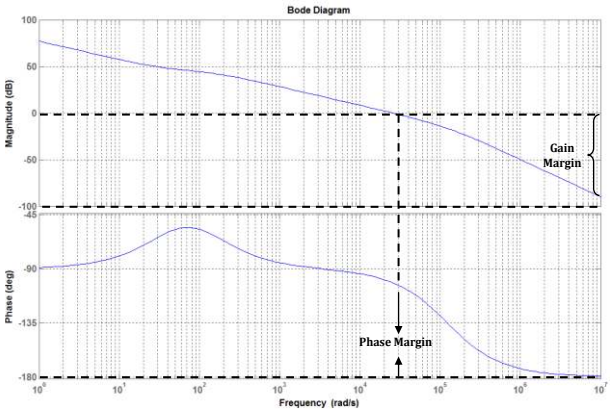

Figure 4. Frequency response of open loop voltage control system with controllers

After obtaining the voltage reference signals at the output of the controller, the carrier-based 3-level pulse-width modulation (PWM) method is used to generate switching signals is depicted in the Figure 5. Since the 3P4L topology has not current path between *n* point and *f* point as shown in the Figure 1, which is different from 3P4W with split DC-link capacitors topology, there is extra degree of freedom in the selection of v_{fn} [16]. Thus, selection of the offset voltage gives some advantages, which are higher DC-link voltage utilization, optimization of switching losses and reduced DC-link capacitor. The offset voltage selection can be achieved by controlling of gate signal of the fourth leg [1], [5]. To utilize the advantages that are mentioned above, offset voltage can be calculated as in Eq. (17).

$$v_{fn} = \begin{cases} -\frac{v^*_{min}}{2}, & v^*_{max} > 0 \\ -\frac{v^*_{max}}{2}, & v^*_{min} > 0 \\ -\frac{v^*_{min}+v^*_{max}}{2}, & elsewhere \end{cases} \quad (17)$$

The calculated offset voltage is added to phase reference voltages to obtain modulation signal of each leg as can be seen in Figure 5. And then, modulation signals are compared with triangular carrier wave that yields 3-level PWM signals for each leg.

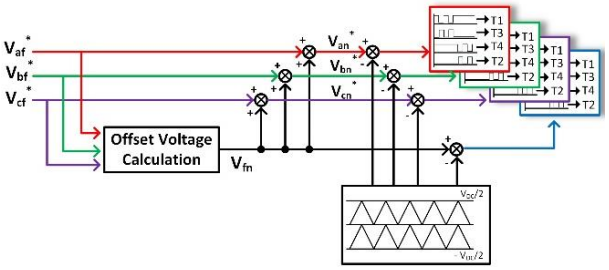

Figure 5. 3-level carrier-based PWM technique

3. SIMULATION RESULTS

The performance of the control algorithm designed for 3-level 3P4L AT-NPC inverter system is extensively evaluated for the different load types in PSIM software simulations. The results of the simulations are presented for three different load types, which are unbalanced load, 1-phase or 2-phase load and non-linear load. PSIM simulation block diagram of the 3-level 3P4L AT-NPC inverter system is shown in Figure 6. The inverter system is created with Fuji Electronic 4MBI300VG-120R-50 RB-IGBT module and with LC-type filter as can be seen in this figure. The inductor value in the LC filter is designed with the consideration of limiting the current ripple to 20% of the rated amplitude. The required minimum inductance is calculated as in (18), [17]. For the design of the LC filter capacitance value, the cut-off frequency of the LC filter is selected typically about 1/10~1/5 of the switching frequency f_{sw} to attenuate the switching ripple. The parameters of the system are summarized in Table 1.

$$L_j = \frac{\frac{V_{DC}}{2} - V_{jN}}{2\Delta I_j} \frac{d_j}{f_{sw}} \quad (18)$$

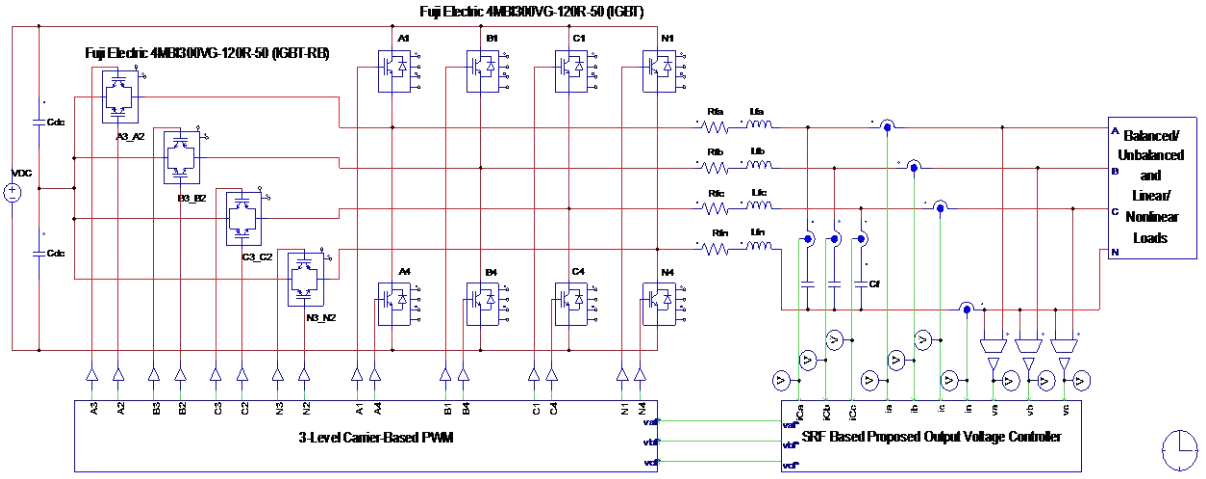

Figure 6. PSIM simulation block diagram of the 3-level 3P4L AT-NPC inverter system

Table 1. System parameters

Parameter	Value & Unit
Rated Power S	35 kVA
Output Voltage $V_{f\text{-}n}$	220 V_{rms}
Output Frequency f	50 Hz
DC-Link Voltage V_{dc}	700 V
DC-Link Capacitor C_{dc}	2200 µF
Filter Capacitance C_f	30 µF
Filter Inductance L_f	2 mH
Simulation Step Time T_s	20 µs
Switching Frequency f_s	5 kHz

In the first case, the control algorithm is tested under linear unbalanced load type. The load connected to the inverter output is 10 Ω, 5 Ω and 12 Ω for each phase leg. Figure 7 shows performance of the system under unbalanced linear load. As can be seen in the Figure 7a, the output voltages of each phase are balanced and its THD values are 1.58%, 1.56% and 1.55%, respectively. The neutral current caused by unbalanced load flows throughout fourth leg.

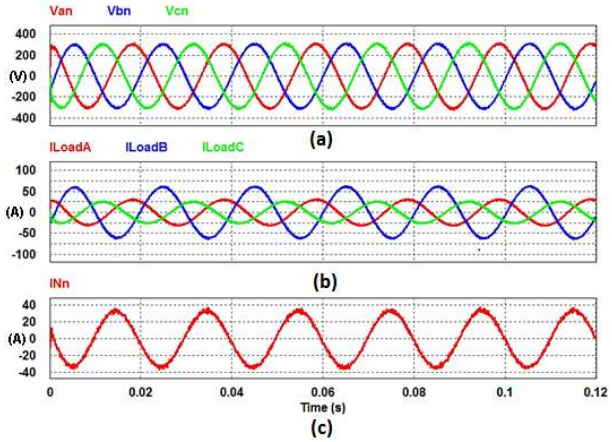

Figure 7. Simulation result of the 3-level 3P4L AT-NPC inverter system with unbalanced 10 Ω, 5 Ω and 12 Ω loads **(a)** output voltages **(b)** inverter currents **(c)** neutral current

In the second case, 1-phase or 2-phase loads are connected at the output of the inverter. In this case, the system start with unbalanced 2-phase loads and then one of the loads is disconnected at 0.06 s. The result about this case is shown in Figure 8. It shows that, the designed controller has fast dynamic response and it provides the 3-level 3P4L AT-NPC inverter system working with 1-phase or 2-phase loads. Moreover, the output voltage is balanced and its THD values are 1.80%, 1.74% and 1.76%, respectively.

In the final test case, 1-phase rectifier with RC load is connected to each phase leg of the inverter output. The load currents have 80.1% THD value. As can be seen in Figure 9, the controller provides the 3-level 3P4L AT-NPC inverter system to work balanced output voltage under non-linear load type. For this case, THD values of the inverter output voltages are 2.58%, 2.55% and 2.58%, respectively.

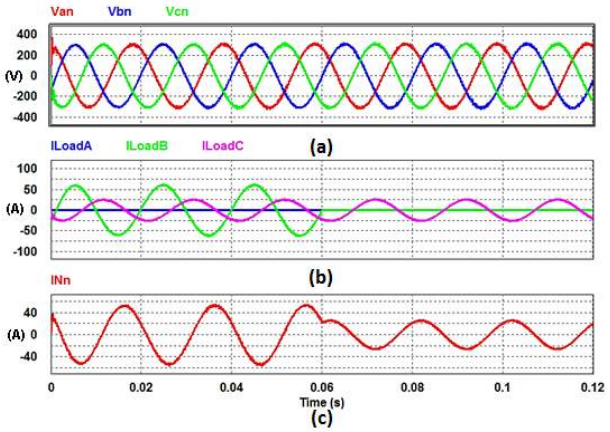

Figure 8. Simulation result of the 3-level 3P4L AT-NPC inverter system with 1-phase or unbalanced 2-phase loads **(a)** output voltages **(b)** inverter currents **(c)** neutral current

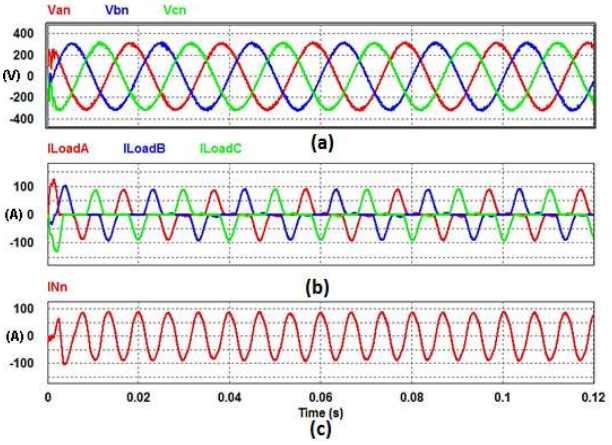

Figure 9. Simulation result of the 3-level 3P4L AT-NPC inverter system with non-linear loads **(a)** output voltage **(b)** inverter currents **(c)** neutral current

All these results show that SRF based control technique used in this study fulfills the requirement of high dynamic response and large stability margin in the 3-level 3P4L AT-NPC inverter system. Additionally, the system achieves to work with or without 2-phases. In all test conditions, the system supply high quality output voltage with less than 3% THD for the different loads.

4. CONCLUSION

In this paper, SRF based high performance output voltage controller is proposed for stand-alone operation of high efficient 3-level 3P4L AT-NPC inverter. For the controller design, capacitor current decoupled model of the inverter with LC-type filter is described. The controller is designed with an outer voltage loop to ensure zero steady state error and with an inner current loop to increase dynamic response of the system. The steady state and dynamic performance of the controller has been evaluated with PSIM simulation studies. The results show that the 3-level 3P4L AT-NPC inverter

system assures high quality balanced nominal output voltage for balanced/unbalanced, linear/non-linear and 1-phase/3-phase load types with less than 3% THD value and provides fast dynamic performance.

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