Stability and Bandwidth Implications of Digitally Controlled Grid-Connected Parallel Inverters

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***Abstract*—The increasing use of grid-connected inverter systems is resulting in a desire for parallel-connected inverters that offer greater power capacity while maintaining the high control bandwidth achieved by individual inverters. This paper demonstrates that, in addition to the traditional stability and bandwidth limitations of digitally controlled inverters, further stability and bandwidth limitations occur when LCL inverters with a common set point are connected in parallel to a grid. This paper provides detailed discrete-time derivations for parallel grid-connected inverters and uncovers stability and bandwidth limitations that only occur in grid-connected applications and are not apparent if the system is studied in continuous time. This paper demonstrates that, in a typical application, the voltage bandwidth of an LCL parallel inverter array is 25% lower than a single module or LC parallel configuration. Both simulations and hardware demonstrations on a 105-kVA parallel three-module grid-connected system confirm the findings.**

***Index Terms*—Digital control, parallel architectures, stability.**

I. Introduction

ONE OF THE main motivations to use digital controllers for inverter applications is to achieve a relatively high level of performance while still achieving a desired level of robustness. In each application, performance and robustness are traded off by selecting different control methods and topologies to achieve an acceptable performance and, at the same time, robustness to different load types. The performance and robustness criteria vary for different applications. In the application of grid-connected inverters, the inverter may have to operate either as a current source (CSI) or, in an island scenario, as a voltage source (VSI) and frequency setter. LCL converter filters, as opposed to single L filters, offer lower switching harmonics (for a given size) and the ability to operate in a voltage sourcing mode, with the latter being useful for isolated grid systems [1].

As the penetration for grid-connected LCL inverters such as solar, wind, and battery storage increases, there is a naturally increasing demand for higher power systems [2]. To be able to provide the same level of bandwidth by using IGBT-based inverters but at ever increasing power levels, the natural tendency is toward parallel arrays of inverters. In some large systems, the number of individual modules can be in excess of hundreds of modules. A large amount of work has been done in the area of the stability of parallel grid-connected inverters [1], [3]–[16], but due to the complexity and the number of continuous components, they have only been investigated in continuous time.

Many control methodologies that are used to achieve high performance have been presented in the literature [17]–[24]. Each of which uses varying forms of state feedback and is typically either discretized continuous-time controllers or direct discrete design. Discretized continuous controllers typically work quite well provided that the sampling frequency (f_s) is well above the control bandwidth (BW), typically $\approx BW < (f_s/20)$ for VSIs [17]. The presence of sampling and calculation delays invalidate the use of discretized continuous controllers where a high bandwidth for a given sampling frequency is required $(BW \approx f_s/10)$.

Many detailed investigations in discrete time have been performed on inverters with simple resistive or nonlinear loads [3]–[6], [25], but there has only been a small number of discrete analyses of paralleled grid-connected inverters. Most examples in literature tend to analyze grid-connected inverters analytically in the continuous-time domain and only provide discrete small-signal stability for numerical examples. In this paper, the continuous-time filters and load are discretized from the start to provide analytical discrete-time transfer functions to demonstrate small-signal stability.

The complexity of analyzing discrete-time inverters with low-impedance loads is compounded when independently controlled inverters are connected in parallel [14]–[16]. This paper discusses the stability issues that arise from digitally controlled parallel-connected inverters driving into low-impedance loads as a result of high frequency resonances outside of the inverters control bandwidth. This paper shows that, although inverters driving into low impedances are still controllable, in most cases, the achievable system bandwidth is constrained. The effect can be quite costly for applications where the maximum achievable bandwidth is important.

The controllers discussed in this paper assume the practical realities of zero-order hold (ZOH) sampling and calculation delays. Calculation delays of one sample period are used unless otherwise specified [18].

Section II is an analytical investigation into the instabilities that occur with parallel arrays of inverters in a grid-connected configuration. First, the stability implications of parallel modules with LC filters are addressed, followed by the additional effects of using LCL filters. In Section III, simulation and experimental results on three parallel-connected two-level

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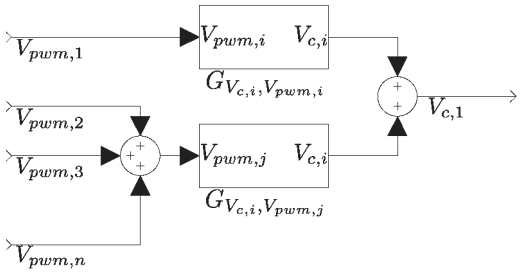

Fig. 1. Indexing example for an n-module system showing module 1 capacitor voltage $V_{c,1}$ as a function of each PWM voltage.

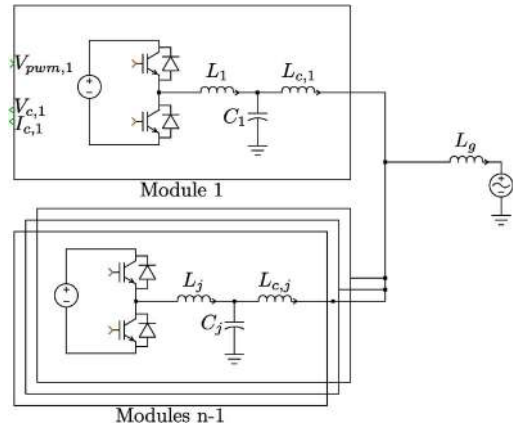

Fig. 2. Soft-coupled parallel VSIs.

35-kVA IGBT inverter modules (a total of 105 kVA) confirm the findings in Section II.

The stability analysis of parallel-connected inverters was prompted by bandwidth limitations observed in a parallel-connected system using 2–32 125-kVA modules. The effects have been further confirmed in the simulation. In addition to practical confirmation, the derived equations have each been confirmed numerically using the Simulink Linearization Analysis toolbox.

Throughout this paper, the following convention with respect to indices is adhered to: For an n-module system, an index i implies the subject module, and an index j implies each of the remaining $n-1$ identical modules. As an example, Fig. 1 shows the use of indexing for one module in a multimodule configuration. As suggested in Fig. 1, for module one, $G_{V_{c,i}V_{\mathrm{pwm},i}}$ is the component of the module one capacitor voltage $(V_{c,1})$ contributed by its own PWM voltage $(V_{\mathrm{pwm},1})$, and $G_{V_{c,i}V_{\mathrm{pwm},j}}$ is the component of $V_{c,1}$ contributed by the sum of the other PWM voltages $(\sum_{k=2}^{n} V_{\mathrm{pwm},k})$.

II. Parallel Stability Analysis

Fig. 2 shows the typical three-phase single-wire topology for a soft-coupled parallel grid-connected two-level VSI of interest. A parallel configuration is herein defined to be hard coupled when the coupling impedance (also known as the line reactor) is zero ($L_{c,i}=0$, and capacitors are all tied together) and soft coupled when there is a real coupling impedance ($L_{c,i}\neq 0$ and independent capacitor voltages). To provide modularity, each three-phase module is considered a separate inverter with its own six-pulse IGBT stack, digital controller, and state feedback sensing. All of the modules are considered identical apart from component value variations, and they all receive the same voltage reference signal.

To introduce the stability implications encountered with inductively coupled parallel grid-connected systems, a common continuous-time-derived VSI controller is considered, shown in Fig. 3(a). The controller is simply a cascaded inductor current loop and a capacitor voltage loop. Fig. 3(b) shows the inductor current state feedback removed through model simplification.

In the absence of the load and loop delays, the continuous-time controller has a clean second-order response[1]

$$\frac{V_c(s)}{V_{c,\mathrm{ref}}(s)}=\frac{\omega_i\omega_v}{s^2+s\omega_i+\omega_i\omega_v}. \tag{1}$$

Before being discretized, the unloaded continuous-time controller (1) is unconditionally stable and has a damping ratio and a natural frequency, given by the following:

$$\zeta=\frac{1}{2}\sqrt{\frac{\omega_i}{\omega_v}} \tag{2}$$

$$\omega_n=\sqrt{\omega_i\omega_v}. \tag{3}$$

Throughout this paper, a voltage-to-current gain ratio of three quarters $(\omega_v=(3/4)\omega_i)$ is used, which provides a damping ratio of 0.6 for the continuous-time controller.

The small-signal stability is first investigated for hard-coupled parallel and then soft-coupled parallel configurations. Small-signal analysis for the remainder of this paper is performed in the discrete-time domain, where the ADC and PWM blocks in Fig. 3 are treated as ZOHs. Additional integrators (or ac resonators) are neglected for stability analysis. For the small-signal stability analysis of the grid-connected VSI, the grid is treated as a low-impedance (inductive) load. Typical grid-connected impedances range from a stiff grid scenario of less than 1% up to a weak grid of 10%. To achieve results that are independent of the number of modules, the grid load impedance L_g in Fig. 2 is scaled by n such that $L_g=L_{g,\mathrm{per\,module}}/n$.

The small-signal stability of an n-module system is defined by the pole locations of the closed-loop system. For the sake of calculation, the transfer function of the first module's capacitor voltage $(V_{c,1})$ with respect to the voltage reference $(V_{c,\mathrm{ref}})$ is used. In the following sections, the systems are disturbed by altering only the first module's parameters while using the specified nominal values for the remaining modules.

The proportional controller in Fig. 3(b) is easily discretized with a single sample time delay (z^{-1})

$$V_{\mathrm{pwm}}=\left((V_{c,\mathrm{ref}}-V_cz^{-1})\omega_vC-I_cz^{-1}\right)\omega_iL+V_cz^{-1}. \tag{4}$$

For analysis purposes, the controller is separated into a feedforward path $C_{\mathrm{Ff}}(z)$ and the capacitor voltage and current feedback paths ($C_{\mathrm{Fb},V_c}(z)$ and $C_{\mathrm{Fb},I_c}(z)$, respectively)

$$V_{\mathrm{pwm}}=V_{c,\mathrm{ref}}C_{\mathrm{Ff}}+V_cC_{\mathrm{Fb},V_c}+I_cC_{\mathrm{Fb},I_c}. \tag{5}$$

[1]The Laplace variable s should be interpreted as the derivative operator $s=d/dt$ where appropriate, and the discrete transform variable z^{-1} should be interpreted as a unit delay operator.

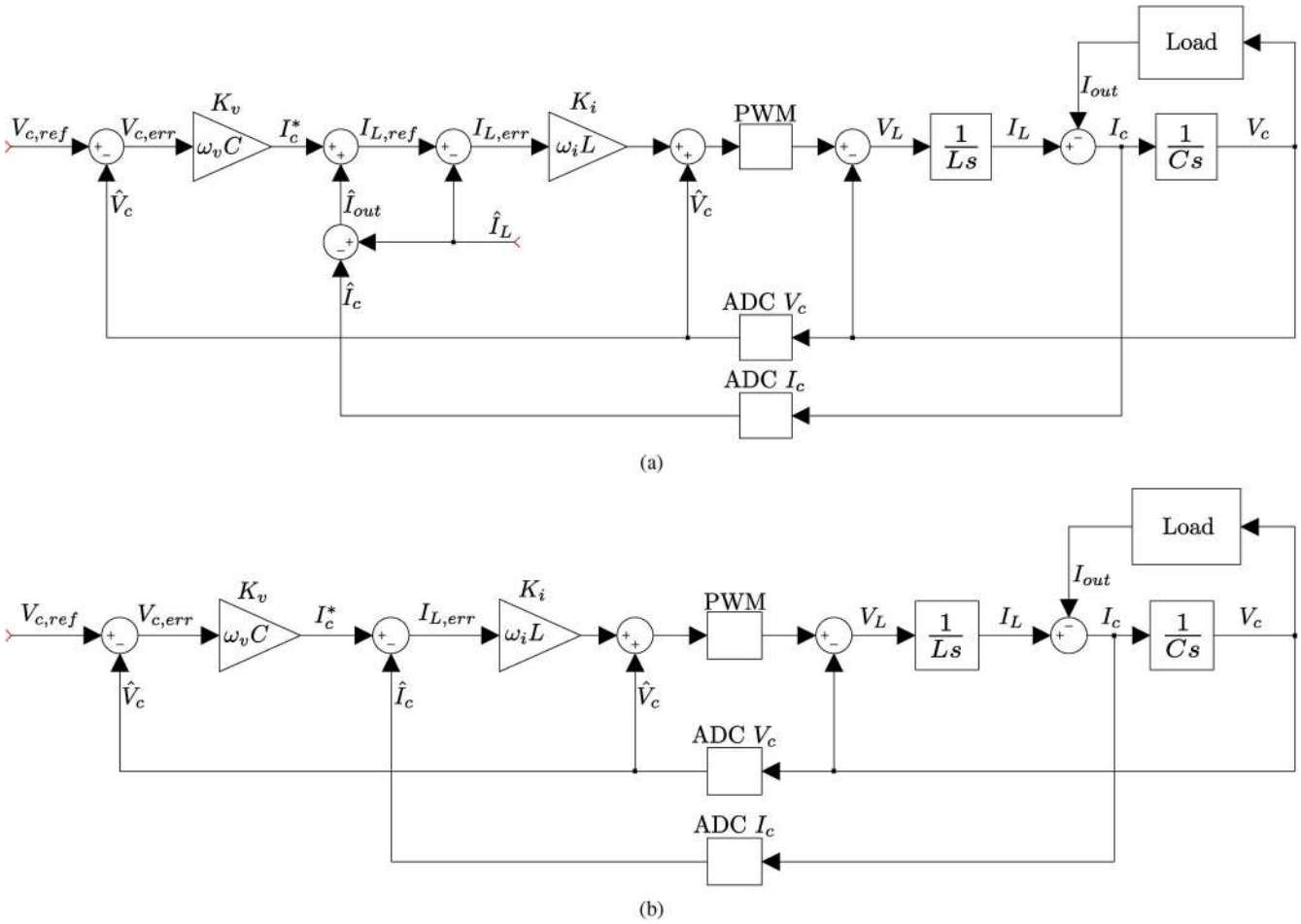

Fig. 3. Continuous-time controller.

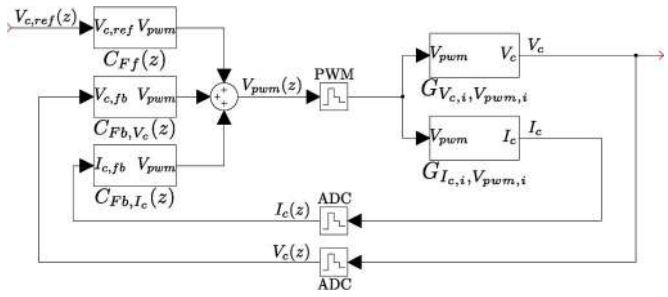

Fig. 4. Controller and filter system blocks for a single module.

Fig. 4 shows the closed-loop connection of the controller and filter components. In practical implementations, the capacitor current can be approximated by differentiating the sampled voltage, removing the need for a capacitor current sensor.

A. Discrete Model

In order to identify the stability issues, expressions for the VSI, including the controller and components, must be derived. Given the discrete nature of the controllers addressed herein, the continuous-time components of the filter and load must first be discretized. Each controller's PWM voltage reference output $(V_{\mathrm{pwm},i}(z))$ and capacitor voltage and current sampling inputs $[V_{c,i}(z)$ and $I_{c,i}(z)]$ are defined as the boundaries for discretizing the parallel-connected output filters and load. The capacitor voltage and current ($V_{c,i}(s)$ and $I_{c,i}(s)$, respectively) are discretized with a regular-sampled ZOH, as shown in [18], where

$$G_{\mathrm{ZOH}}(z) = \mathcal{Z}\left\{\frac{1-e^{-sT_s}}{s}G(s)\right\}. \tag{6}$$

ZOH discretization of a second-order undamped continuous system (7), such as an inductively loaded LC filter, results in a second-order discrete system, as in (8), where ω_n is the natural frequency of the filter and T_s is the sample period

$$H(s) = \frac{k}{\left(\frac{s}{\omega_n}\right)^2 + 1} \tag{7}$$

$$H_{\mathrm{ZOH}}(z) = \mathcal{Z}_{\mathrm{ZOH}}\left(H(s)\right) = \frac{k(z+1)\left(1-\cos(\omega_n T_s)\right)}{z^2 - 2z\cos(\omega_n T_s) + 1}. \tag{8}$$

B. Hard Coupled

To analyze parallel configurations of inverters where each inverter has its own controller and filter, the hard or soft parallel-connected filters and load are discretized as a whole. In the hard-coupled scenario, all the module capacitors are connected together, and each controller senses the same voltage. The sensed capacitor currents are identical for identical capacitor values.

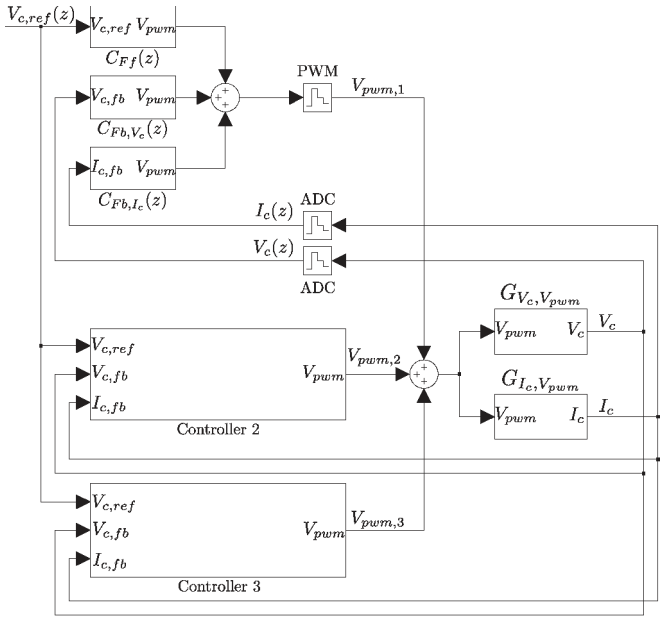

Fig. 5. Identical three-module hard-coupled parallel configuration. Module 1 controller unmasked.

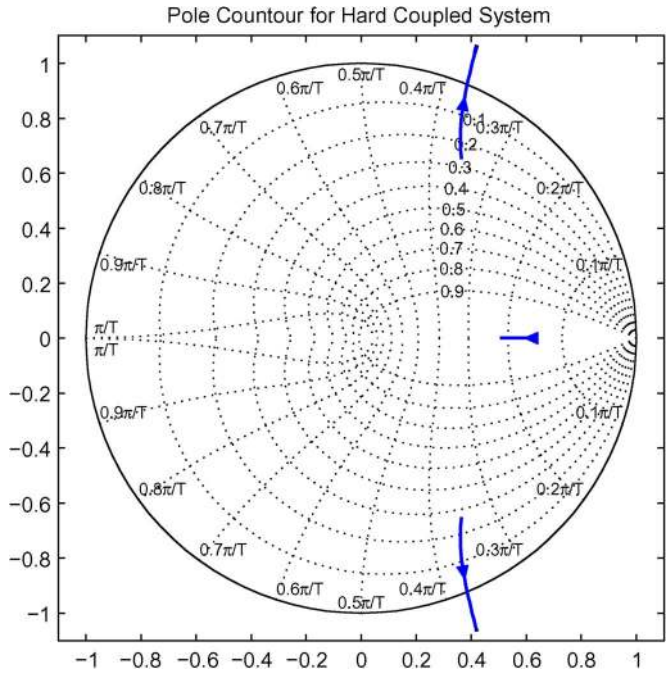

Fig. 6. Pole contour of the hard-coupled system with ω_i gain sweep from 5 to 20 pu. $T_s = (2\pi/160)$ pu (i.e., an 8-kHz sampling relative to a 50-Hz fundamental), $L = 4\%$ pu, $C = 10\%$ pu, $L_g = 5\%$ pu, $\omega_v = (3/4)\omega_i$, and identical module system.

Equating the capacitor and load currents in Fig. 2 where $n-1$ of the modules have identical inductors L_i and module one has filter inductance L_1

$$\frac{V_{\mathrm{pwm},1} - V_c}{sL_1} + \frac{\sum_{k=2}^{n} V_{\mathrm{pwm},k} - V_c}{sL} = V_c\left(nsC + \frac{1}{sL_g}\right). \quad (9)$$

Solving for V_c

$$V_c(s) = \frac{\left(V_{\mathrm{pwm},1}(s)L + \sum_{k=2}^{n} V_{\mathrm{pwm},k}(s)L_1\right)L_g}{s^2LL_1L_gCn + L_g\left(L + L_1(n-1)\right) + LL_1n} \quad (10)$$

$$V_c(s) = G_{V_c,V_{\mathrm{pwm},i}}V_{\mathrm{pwm},i} + G_{V_c,V_{\mathrm{pwm},i}}V_{\mathrm{pwm},j}. \quad (11)$$

The capacitor currents become

$$I_{c,i}(s) = \frac{V_{c,i}(s)}{Z_c} = sCV_{c,i}(s). \quad (12)$$

Note that, for an identical system, substituting $L_1 = L$ and $V_{\mathrm{pwm},1} = V_{\mathrm{pwm},i}$ in (10), shown in Fig. 5, produces

$$V_c(s) = \frac{\sum_{k=1}^{n} V_{\mathrm{pwm},k}(s)L_g}{n(s^2LL_gC + L_g + L)}. \quad (13)$$

As each controller samples the same common capacitor voltage, each controller produces the same PWM reference (V_{pwm}), and therefore, $V_{\mathrm{pwm},i} = V_{\mathrm{pwm},j}$.

The discretized capacitor voltage transfer function for an identical parallel configuration in (13), as shown in [5], is

$$G_{V_c,V_{\mathrm{pwm}}}(z) = \frac{L_g(z+1)\left(1 - \cos\left(T_s\sqrt{\frac{L_g+L}{LL_gC}}\right)\right)}{n(L_g+L)\left(z^2 - 2z\cos\left(T_s\sqrt{\frac{L_g+L}{LL_gC}}\right) + 1\right)}. \quad (14)$$

Discretizing the filter and closing the controller loop

$$G_{V_c,V_{\mathrm{pwm}}} = G_{V_c,V_{\mathrm{pwm}},i}(z) + G_{V_c,V_{\mathrm{pwm}},j}(z) \quad (15)$$

$$G_{I_c,V_{\mathrm{pwm}}} = G_{I_c,V_{\mathrm{pwm}},i}(z) + G_{I_c,V_{\mathrm{pwm}},j}(z) \quad (16)$$

$$\frac{V_c(z)}{V_{c,\mathrm{ref}}(z)} = \frac{C_{\mathrm{Ff}}C_{\mathrm{Fb},V_c}G_{V_c,V_{\mathrm{pwm}}}}{1 - \left(C_{\mathrm{Fb},V_c}G_{V_c,V_{\mathrm{pwm}}} + C_{\mathrm{Fb},I_c}G_{I_c,V_{\mathrm{pwm}}}\right)}. \quad (17)$$

From (17), it can be seen that, for a hard parallel configuration of identical inverters, there is no longer any dependence on the number of parallel modules n.

The hard-coupled system with a single sample time delay (17) has three poles. Fig. 6 shows the pole contours for a gain sweep of $\omega_i = 5$ to 20 pu. The hard-coupled configuration becomes unstable at $\omega_i = 14.6$ pu.

Derivation of a nonidentical configuration is given in the Appendix. Fig. 7 shows the effect of the component sensitivities in a three-module system by varying L_1. Increasing the number of modules reduces the effect of component variations. Despite component sensitivities, no additional unmatched pole-zero pairs arise inside or outside of the unit circle.

C. Soft Coupled

The soft-coupled configuration now assumes a nonzero coupling impedance $L_{c,i} \neq 0$ in Fig. 2. With the addition of L_c, (15) and (16) are no longer valid, and the individual module capacitor voltages and currents must be resolved. Fig. 8 shows the closed-loop configuration for a three-module soft-coupled parallel configuration where each module is identical. Note that Fig. 8 does not show the equivalent blocks for the capacitor current feedbacks.

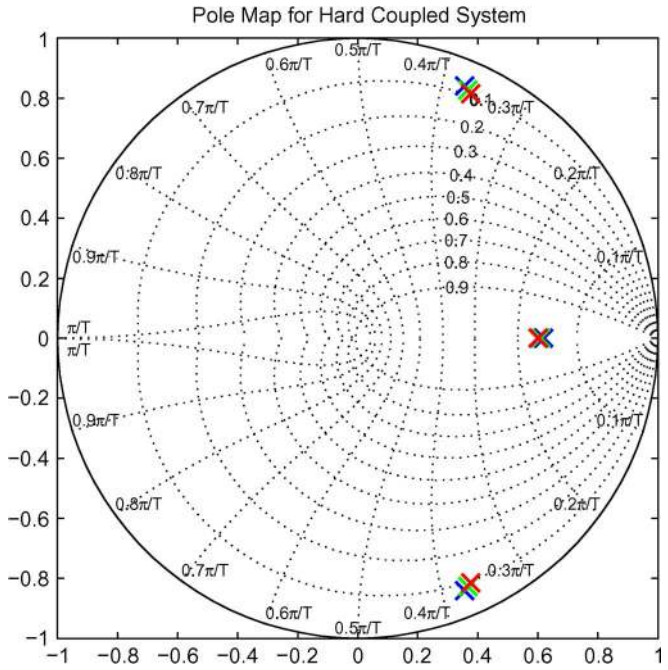

Fig. 7. Pole map of the hard-coupled system demonstrating component sensitivities by varying module one inductor. $T_s = (2\pi/160)$ pu, $L = 4\%$, $C = 10\%$, $L_g = 5\%$, $L_1 = L \pm 10\%$, $\omega_i = 11$ pu, $\omega_v = (3/4)\omega_i = 8.25$, and three-module system.

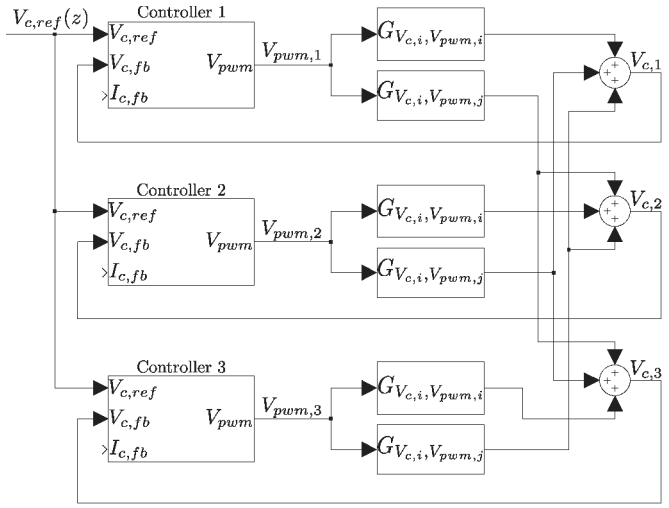

Fig. 8. Soft-coupled parallel system with three modules. Note that the functions for the capacitor currents are not shown but are of the same form as the capacitor voltage functions.

The module capacitor voltages are derived in a similar manner to the hard-coupled configuration except that there is no longer one common capacitor voltage, and as a result, each controller no longer produces the same PWM reference ($V_{\mathrm{pwm},i}$). Continuous transfer functions for the module capacitor voltages in Fig. 8 are given in (18) and (19), shown at the bottom of the page. Capacitor currents are obtained by (12).

Closing the loops in Fig. 8 for an n-module parallel configuration gives the module one capacitor voltage as a function of the reference voltage. Defining

$$H_1 = G_{V_{c,i}V_{\mathrm{pwm},i}}(z) \tag{20}$$
$$H_2 = G_{V_{c,i}V_{\mathrm{pwm},j}}(z) \tag{21}$$
$$H_{1I} = G_{I_{c,i}V_{\mathrm{pwm},i}}(z) \tag{22}$$
$$H_{2I} = G_{I_{c,i}V_{\mathrm{pwm},j}}(z). \tag{23}$$

The complete transfer function for an individual module $V_{c,i}(z)$ as a function of $V_{c,\mathrm{ref}}(z)$ is given by (24), which is shown at the bottom of the page.

The first observation to be made in (24) is that further pole-zero cancellations can be made. The two factors in the denominator (25) and (26), which are shown at the bottom of the page, each contribute a complex pole pair and a single real pole. A further cancellation of (25) produces (27), which is shown at the bottom of the page, with a single pole-pair and a

$$G_{V_{c,i}V_{\mathrm{pwm},i}}(s) = \frac{V_{c,i}(s)}{V_{\mathrm{pwm},i}(s)} = \frac{s^2 nL_cLC(L_c+L_g) + nL_c(L+L_c+L_g) + LL_g}{n(s^2LCL_c + L + L_c)\left(s^2LC(L_c+L_g) + L + Lc + L_g\right)} \tag{18}$$

$$G_{V_{c,i}V_{\mathrm{pwm},j}}(s) = \frac{V_{c,i}(s)}{V_{\mathrm{pwm},j}(s)} = \frac{LL_g}{n(s^2LCL_c + L + L_c)\left(s^2LC(L_c+L_g) + L + Lc + L_g\right)} \tag{19}$$

$$\frac{V_{c,i}(z)}{V_{c,\mathrm{ref}}(z)} = \frac{-C_{\mathrm{Ff}}\left(H_1+(n-1)H_2\right)\left(C_{\mathrm{Fb},V_c}(H_1-H_2)+C_{\mathrm{Fb},I_c}(H_{1I}-H_{2I})-1\right)}{\left(C_{\mathrm{Fb},V_c}(H_1-H_2)+C_{\mathrm{Fb},I_c}(H_{1I}-H_{2I})-1\right)\left(C_{\mathrm{Fb},V_c}(H_1-H_2)+C_{\mathrm{Fb},I_c}(H_{1I}-H_{2I})-1+n(C_{\mathrm{Fb},V_c}H_2+C_{\mathrm{Fb},I_c}H_{2I})\right.} \tag{24}$$

$$Factor_1 = (C_{\mathrm{Fb},V_c}(H_1 - H_2) + C_{\mathrm{Fb},I_c}(H_{1I} - H_{2I}) - 1) \tag{25}$$

$$Factor_2 = (C_{\mathrm{Fb},V_c}(H_1 - H_2) + C_{\mathrm{Fb},I_c}(H_{1I} - H_{2I}) - 1 + n(C_{\mathrm{Fb},V_c}H_2 + C_{\mathrm{Fb},I_c}H_{2I}) \tag{26}$$

$$\frac{V_{c,i}(z)}{V_{c,\mathrm{ref}}(z)} = \frac{-C_{\mathrm{Ff}}\left(H_1 + (n-1)H_2\right)}{(C_{\mathrm{Fb},V_c}(H_1 - H_2) + C_{\mathrm{Fb},I_c}(H_{1I} - H_{2I}) - 1 + n(C_{\mathrm{Fb},V_c}H_2 + C_{\mathrm{Fb},I_c}H_{2I})} \tag{27}$$

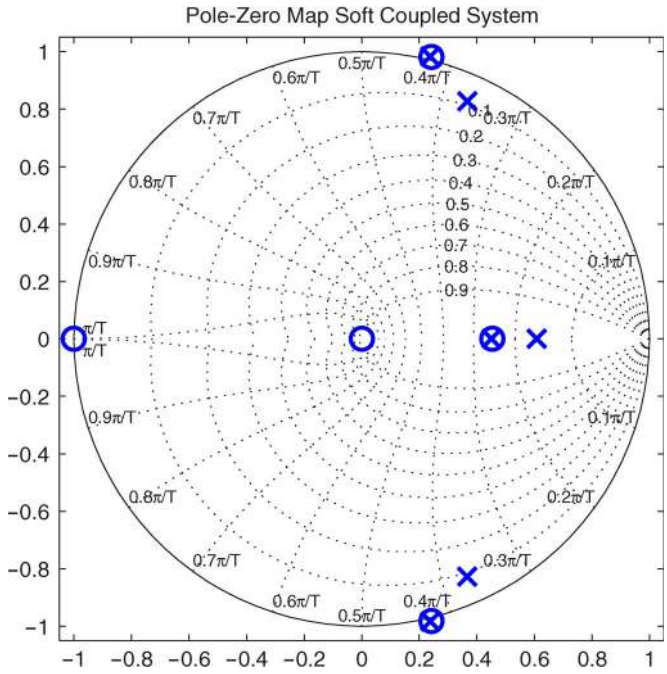

Fig. 9. Pole-zero map of the soft-coupled system varying module one coupling impedance $L_{c,1}$. $T_s = (2\pi/160)$, $L = 4\%$, $C = 10\%$, $L_c = 2\%$, $L_{c,1} = 0.95L_c$, $L_g = 3\%$, $\omega_i = 11$, $\omega_v = (3/4)\omega_i = 8.25$, and three-module system.

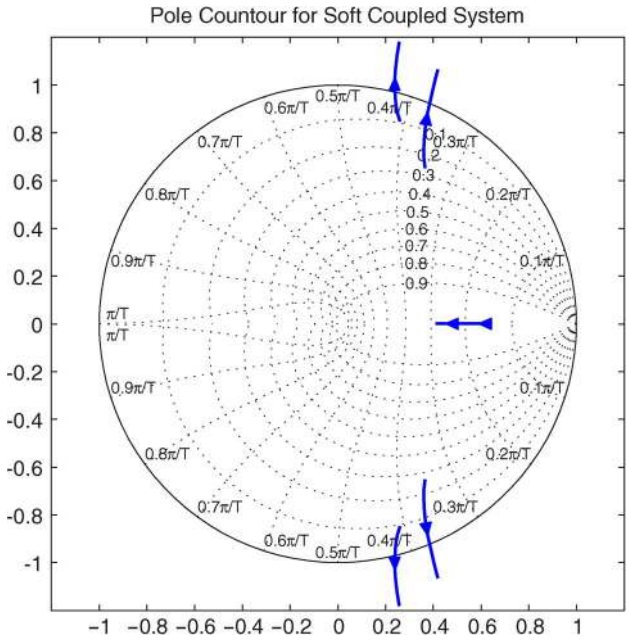

Fig. 10. Pole contour of the soft-coupled system with ω_i gain sweep from 5 to 20 pu. $T_s = (2\pi/160)$, $L = 4\%$, $C = 10\%$, $L_c = 2\%$, $L_{c,1} = 0.95L_c$, $L_g = 3\%$, $\omega_v = (3/4)\omega_i$, and three-module system.

single real pole. For a purely ideal system where all the modules are identical, (25) may be safely cancelled, but for any real system, this is where the stability issues for parallel coupled systems appear.

For a purely identical hard-coupled system whose load $(L_{g,\mathrm{hard}})$ is the sum of the coupling impedance and load of a soft-coupled system $(L_{g,\mathrm{hard}} = L_{g,\mathrm{soft}} + L_c)$, the responses are exactly the same.

Fig. 9 shows the effect when the modules are not identical. The coupling impedance and load impedance sum are the same as Fig. 7. When the modules are not exactly identical, the factor (25) of (24) no longer perfectly cancels and manifests as the pole-zero pairs just outside of the unit circle. Not only do the pole-zero pairs not cancel, but the same gains in a hard-coupled system have a lower stability margin than in a soft-coupled system. Fig. 9 shows that the additional pole-zero pair are outside the unit circle, causing the system to become unstable. Fig. 9 is unstable with the same gains as the hard-coupled system in Fig. 7.

Fig. 10 shows the pole contour of a nonidentical parallel configuration with a load impedance. The same contours exist, which are in the hard-coupled system in Fig. 6, but the additional complex pole-pair lowers the soft-coupled system's stability margin. Table I shows the stability margin gains for a hard-coupled system against a soft-coupled system. The hard-coupled system achieves a 37% higher maximum gain than the soft-coupled system.

The soft-coupled instability requires a minimum of two parallel modules (by definition). The system gain margin approaches a limit as the number of parallel modules approaches infinity. The greatest change in gain margin is between a system with two and three modules. Displaying the effect of varying the number of modules is difficult as the stability margin only varies by approximately 3% (between two and an infinite number of modules and with module parameters specified in Fig. 10).

TABLE I
HARD- AND SOFT-COUPLED PARALLEL STABILITY MARGINS

Hard-coupled	Soft-coupled
$\omega_i = 14.6$pu, $\omega_v = 10.9$pu	$\omega_i = 10.6$pu, $\omega_v = 7.9$pu

III. RESULTS

The stability implications of soft-coupled parallel configurations were tested both numerically in simulation and in practice on a three-module 4-kHz-switching 105-kVA system. MATLAB Simulink was used to simulate the soft- and hard-coupled parallel configurations. The Simulink Linearization Toolbox was used throughout the development of the simulations to derive numerical transfer functions to ensure the system matched the equations discussed previously. Independent alpha and beta controllers (in the stationary reference frame) are used in both simulation and hardware.

Tight control of the simulations and hardware experiments has achieved a very close correlation of results. This was achieved by ensuring that the same sampling rates, loop delays, and component values were closely matched. In both simulation and hardware, a whole sample time delay was used with symmetric sampling at 8 kHz (4-kHz switching).

Due to hardware constraints, the capacitor current state feedback was instead approximated by using an observer (discrete lead) on the capacitor voltage rather than sensing the actual current. An additional real pole is created, but stability effects are similar to actual current sensing. Fig. 11 shows the poles

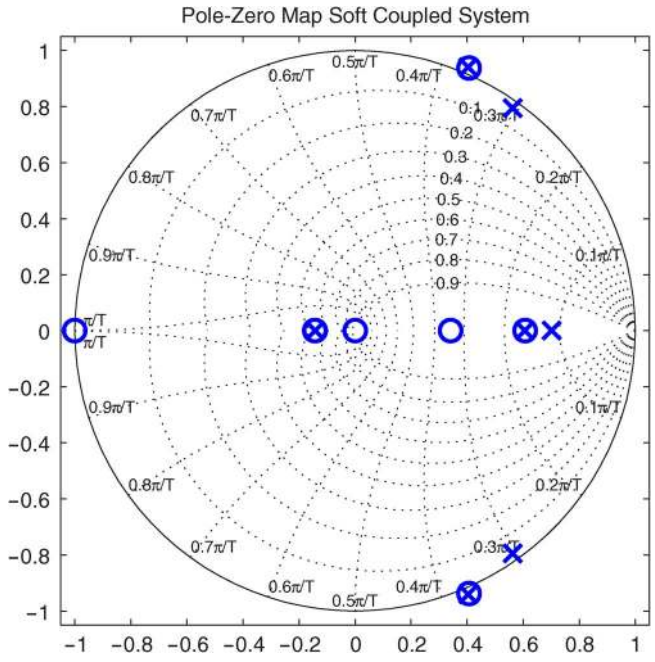

Fig. 11. Pole-zero map of the soft-coupled system varying module one coupling impedance $L_{c,1}$. $T_s = (2\pi/160)$, $L = 4\%$, $C = 10\%$, $L_c = 2\%$, $L_{c,1} = 0.95L_c$, $L_g = 3\%$, $\omega_i = 11$, $\omega_v = (3/4)\omega_i = 8.25$, and three-module system.

and zeros of the system in Fig. 9 but with a capacitor current observer. In all scenarios, a lead filter cutoff frequency of 25 pu is used as it provides a similar stability margin as the actual capacitor current feedback method.

To ensure current sharing between modules, conventional voltage droop that operates on the individual module's output current is used. In both simulation and hardware tests, a droop of 1% is used. Simulations demonstrated that the droop has almost no effect on the parallel module stability margin being demonstrated. Both the simulation and hardware have internal current limits of ± 2 pu, implemented in the controller inductor current loop.

A. Simulations

Fig. 12 shows the output currents of both hard- and soft-coupled three-module parallel systems in a grid-connected configuration. The controller gains were varied to find the point that the soft-coupled system was marginally unstable. The onset of instability is clearly visible in the soft-coupled output current waveform. The simulation results produce the same result with or without a PWM modulator. Small but realistic values of parasitic damping were added to the simulation to better match the hardware setup but had negligible effect on the stability margin of the system.

Instability of the parallel configuration was also confirmed, and it matches with the theoretical expected stability margin. A confirmation that the simulation instability is a result of the unstable poles is confirmed by measuring the instability oscillation frequency. In Fig. 12, the soft-coupled instability oscillation frequency is measured as 29 pu. The pole-zero pair that is outside of the unit circle in Fig. 11 has a natural frequency of 29.6 pu.

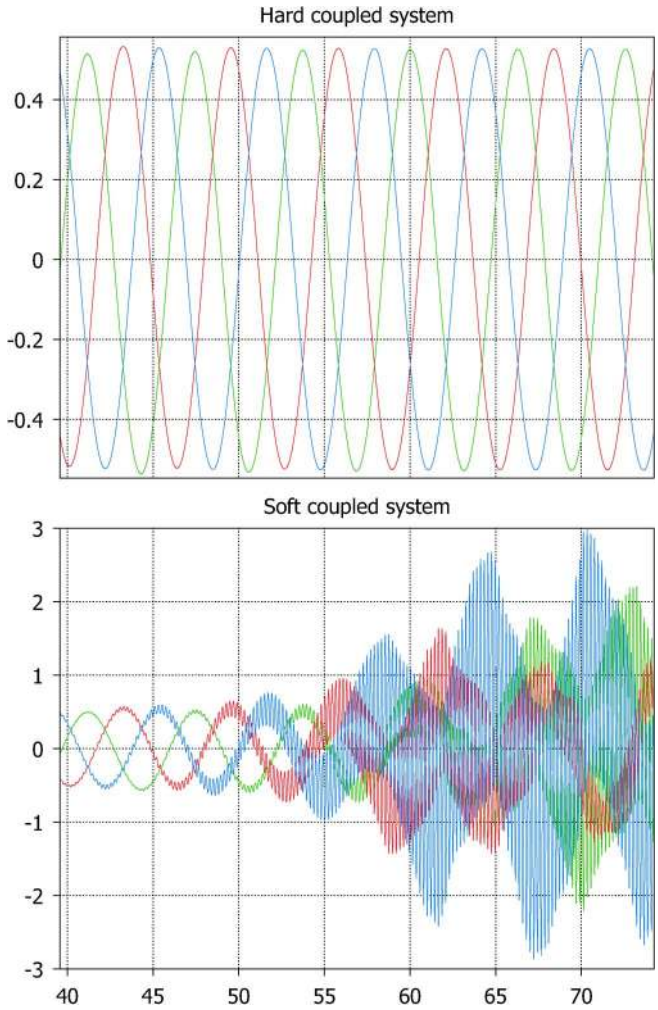

Fig. 12. Simulation output currents of hard- and soft-coupled parallel systems working against a grid. $T_s = (2\pi/160)$, $L = 4\%$, $C = 10\%$, $L_c = 2\%$, $L_{c,1} = 0.99L_c$, $L_g = 5\%$, $\omega_i = 10.6$, $\omega_v = (3/4)\omega_i = 7.9$, and three-module system. Grid resistance $= 1\%$, capacitor ESR $= 0.1\%$, and inductor parallel resistance $= 1/0.1\%$.

In Fig. 12, the nonlinearity of the unstable soft-coupled inverter currents is due to the ± 2 pu inductor current software limits.

B. Practical Results

Practical results were attained on a three-module 105-kVA (50 A at 400 V per module) parallel system, shown in Fig. 13. Each module has its own controller and receives the same alpha–beta voltage reference signal from a master controller. The master controller generates the module reference from a phase locked loop synchronized to the grid voltage [26], [27]. An SCR static switch provides local rapid grid connect/disconnect. The inverters share a common isolation dc supply. The isolated supply permits direct connection of the inverter output to the grid, negating the need for an isolation transformer, as shown in Fig. 2.

The grid impedance was measured to be approximately 4% relative to a single-module current rating. The inverter nominal passive component values are the same or similar as the values used in the simulation ($T_s = 2\pi/160$, $L = 4\%$, $C = 10\%$,

Fig. 13. Test hardware. Three pairs of reconfigurable active rectifiers and output inverters.

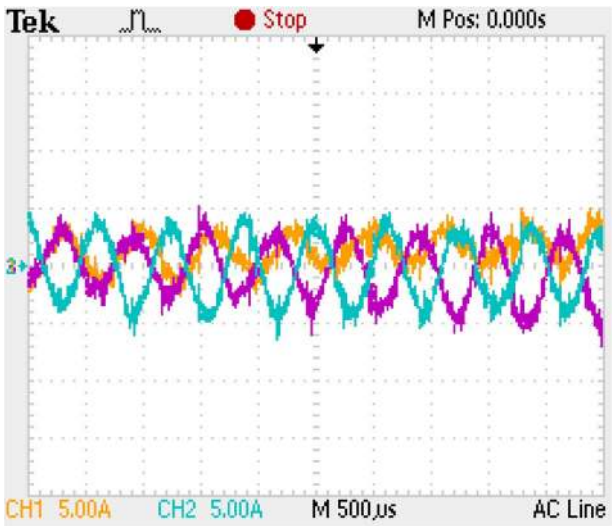

Fig. 14. Marginally unstable soft-coupled output current. $\omega_i = 10.5$. $\omega_v = 7.9$.

and $L_c = 2.3\%$). Component tolerance variations of up to 5% provided adequate difference between module inductances to induce soft-coupled instability.

Fig. 14 shows the soft-coupled output current for marginally unstable gains and that the instability point matches the expected gains as derived in Section II. Table II shows that both the simulation and hardware stability margin gains match the theoretical gains and oscillation frequency to within 2%.

Fig. 15 shows the hard-coupled output voltage for marginally unstable gains. Similar to the soft-coupled configuration, the hard-coupled stability margin gains match the theoretical and simulation results to within 2%.

TABLE II
SOFT-COUPLED STABILITY MARGIN

	ω_i (pu)	ω_v (pu)	Oscillation frequency (pu)
Theoretical	10.6	7.9	29.6
Simulation	10.4	7.8	29
Practical	10.5	7.9	28

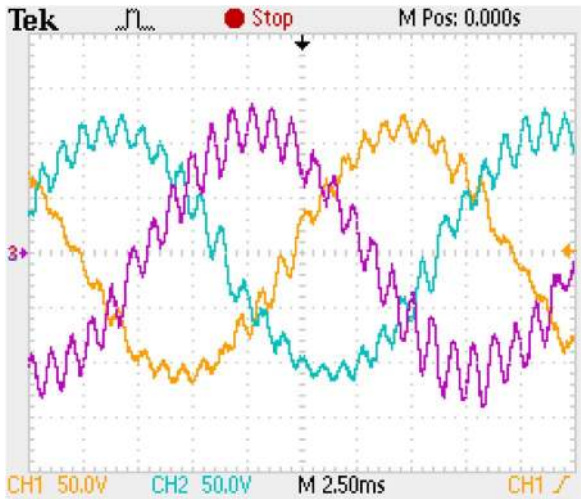

Fig. 15. Marginally unstable hard-coupled configuration output voltage. $\omega_i = 14.4$. $\omega_v = 10.8$.

IV. CONCLUSION

Detailed discrete-time derivations for digitally controlled grid-connected parallel inverters have been derived. The derivations and numerical evaluation show that the stability of hard-coupled parallel systems where each module's capacitors are tied together is purely limited by the typical stability constraints of discrete-time controllers. This is further confirmed by demonstrating that identical hard-coupled parallel systems reduce down and perform exactly the same as one large single module.

Given the stability of hard-coupled configurations, derivations are then provided for soft-coupled parallel systems where each module has its own independent LCL filter. The derivations and numerical analysis show that the stability of soft-coupled systems are not just limited by the typical stability constraints, but additional poles arise, further limiting the controller bandwidth.

Numerical results indicate that the bandwidth limitation of soft-coupled grid-connected systems can be up to 25%. The numerical example given for a 50-Hz system with a 8-kHz sample time shows a voltage bandwidth reduction from the 11th down to the 8th harmonic.

The analytical derivations and numerical results are further confirmed with both three-phase simulations and in a 105-kVA three-module hardware test setup. Stability margins of the simulations and hardware show a close correlation with the numerical results to within 2%.

APPENDIX
NONIDENTICAL HARD-COUPLED DERIVATION

Continuing from (10)–(12) for unique module one and $n-1$ identical modules in parallel

$$G_{V_c,V_{\mathrm{pwm},1}}(s) = \frac{LL_g}{s^2LL_1L_gCn + L_g\left(L + L_1(n-1)\right) + LL_1n} \tag{28}$$

$$G_{V_c,V_{\mathrm{pwm},j}}(s) = \frac{(n-1)L_1L_g}{s^2LL_1L_gCn + L_g\left(L + L_1(n-1)\right) + LL_1n}. \tag{29}$$

Capacitor currents

$$G_{I_c,V_{\mathrm{pwm},1}}(s) = sCG_{V_c,V_{\mathrm{pwm},1}}(s) \tag{30}$$

$$G_{I_c,V_{\mathrm{pwm},j}}(s) = sCG_{V_c,V_{\mathrm{pwm},j}}(s). \tag{31}$$

Discretizing voltages and currents

$$G_{V_c,V_{\mathrm{pwm},1}}(z) = \mathcal{Z}_{\mathrm{ZOH}}\left(G_{V_c,V_{\mathrm{pwm},1}}(s)\right) \tag{32}$$

$$G_{V_c,V_{\mathrm{pwm},1}}(z) = \mathcal{Z}_{\mathrm{ZOH}}\left(G_{V_c,V_{\mathrm{pwm},1}}(s)\right) \tag{33}$$

$$G_{I_c,V_{\mathrm{pwm},j}}(z) = \mathcal{Z}_{\mathrm{ZOH}}\left(G_{I_c,V_{\mathrm{pwm},j}}(s)\right) \tag{34}$$

$$G_{I_c,V_{\mathrm{pwm},j}}(z) = \mathcal{Z}_{\mathrm{ZOH}}\left(G_{I_c,V_{\mathrm{pwm},j}}(s)\right). \tag{35}$$

Closing loops on all modules

$$G_{V_c,V_{\mathrm{pwm}}} = G_{V_c,V_{\mathrm{pwm},1}} + G_{V_c,V_{\mathrm{pwm},j}} \tag{36}$$

$$G_{I_c,V_{\mathrm{pwm}}} = G_{I_c,V_{\mathrm{pwm},1}} + G_{V_c,V_{\mathrm{pwm},j}} \tag{37}$$

$$\frac{V_{\mathrm{pwm},1}}{V_{c,\mathrm{ref}}} = \frac{C_{\mathrm{Ff}}}{1 - C_{\mathrm{Fb},V_c}G_{V_c,V_{\mathrm{pwm}}} + C_{\mathrm{Fb},I_c}G_{I_c,V_{\mathrm{pwm}}}} \tag{38}$$

$$\frac{V_{c,1}}{V_{c,\mathrm{ref}}} = \frac{V_{\mathrm{pwm},1}}{V_{\mathrm{ref}}}G_{V_c,V_{\mathrm{pwm}}}. \tag{39}$$

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