Stability and Dynamic Performance of Current-Sharing Control for Paralleled Voltage Regulator Modules

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***Abstract*—The parallel operation of voltage regulator modules (VRMs) for high-end microprocessors requires a current-sharing (CS) circuit to provide a uniform load distribution among the modules. A good dynamic performance of the CS circuit is very important since the microprocessors present highly dynamic loads to the VRMs. Stability and dynamic performance of the CS control are considered. To assess these issues, a comprehensive small-signal model of the paralleled VRMs was developed and verified.**

***Index Terms*—Current sharing, dc/dc converters, stability, transient response, voltage regulator modules.**

I. Introduction

TO increase the speed of data processing, today's high-end computers use multiple microprocessors. Due to low operating voltages and highly dynamic nature of modern microprocessors, a power supply, which has a very tightly regulated output voltage, is needed. These power supplies, called voltage regulator modules (VRMs), are located on the motherboard next to the microprocessor. In order to take advantage of the modularity and economy of scale, today's high-end computers use one VRM per microprocessor. To improve the speed and integrity of the interconnecting signals, the VRMs are then paralleled to form common power and ground planes. However, paralleling of VRMs requires current-sharing (CS) circuitry to ensure equal load-current distribution among the modules for both steady state and transient load conditions. A good dynamic performance of the CS circuit is very important since the microprocessors present a highly dynamic load for the VRMs.

To meet the requirements of high power density and fast transient response, today's high-end VRMs employ the interleaved buck topology with synchronous rectifiers (SRs) [1], [2]. The interleaved SR-buck topology is controlled by dedicated ICs, available now on the market from several manufacturers. Since these ICs do not have a built-in circuitry to provide current sharing among paralleled VRMs, the CS function is implemented by the discrete circuitry around the IC controller. A current-sharing technique for paralleled VRMs, popular for its low component count and low cost, was proposed in [3]. The objective of this paper is to evaluate and optimize the dynamic performance of the proposed CS technique. Proper attention is paid to the issue of hardware measurement of CS loop small-signal characteristics. Experimental verification of the CS dynamic performance is important not only from the design point of view. Once the dynamic behavior of the circuit is understood and verified, design specifications can be written which will ensure compatibility of VRMs from different vendors.

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II. VRM Current-Sharing Technique

The simplified circuit diagram of two paralleled VRMs with the CS control, proposed in [3], is shown in Fig. 1. The power stages of two VRMs are represented in Fig. 1 by lumped average models [4] which correspond to the interleaved SR-buck converters. The switching parts of the power stages are modeled by dependent voltage sources $V_{IN} \cdot d_1$ and $V_{IN} \cdot d_2$, where V_{IN} is the input voltage and d_1, d_2 are the duty ratios. The VRMs' output filters are represented by lumped components L_F, C_F and their parasitic resistances $\mathrm{ESR}_L, \mathrm{ESR}_C$. Interconnect impedances between modules are represented by wire resistances R_{W1} and R_{W2}. VRMs # 1 and # 2 in Fig. 1 operate with voltage-mode control. The pulse-width modulators are represented by the blocks with gain F_M. Current sources i_{X1}, i_{X2}, proportional to inductor currents i_{L1}, i_{L2}, in combination with resistors R_4 provide droop regulation for increased headroom during load transients [3]. The voltage drops across resistors R_4 are also used as the input signals for the CS circuit. During steady-state operation, these voltage drops are proportional to inductor currents i_{L1}, i_{L2}. The voltage drops across resistors R_4 are then amplified by current amplifiers CA1 and CA2.

The outputs of amplifiers CA1 and CA2 are connected to the common CS bus through the network of resistors R_{14}. The voltage on the CS bus is proportional to the average current of both VRMs. Therefore, the voltage drops across resistors R_{14} represent errors between individual inductor currents i_{L1}, i_{L2} and average current $(i_{L1}+i_{L2})/2$. These errors are amplified by opamps UA1 and UA2 whose output voltages V_{A1}, V_{A2} are converted by resistors R_{13} into currents which are injected into the voltage feedback loops at the inverting inputs of remote-voltage-sense amplifiers UC1, UC2. Note that the proposed CS scheme relies simultaneously on two mechanisms:

1) droop current sharing;
2) feedback control loop which compares inductor currents of the individual modules and takes the corrective action based on their difference.

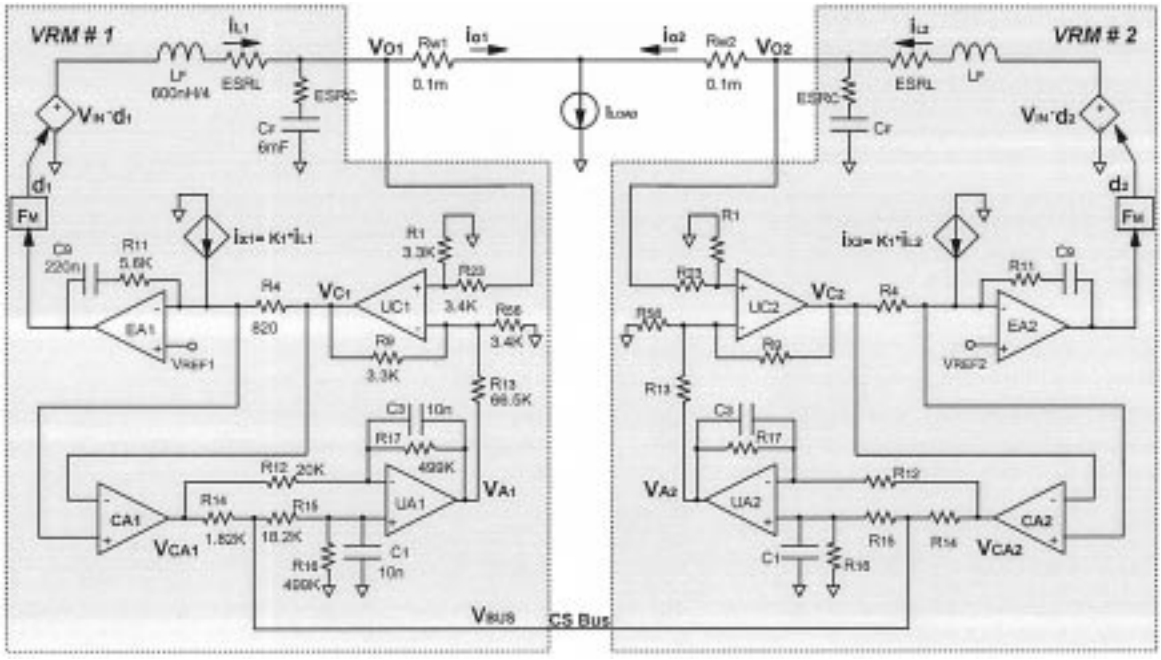

Fig. 1. Simplified circuit diagram of the current-sharing circuit for paralleled VRMs.

III. Small-Signal Modeling of Paralleled VRMs

To facilitate development of the small-signal model, a stand-alone VRM is represented by a Thevenin source [5], [6], as shown in Fig. 2. The Thevenin-source approach simplifies the model since it focuses only on the CS loop. Output voltage $\hat{V}_O$ of the Thevenin source depends on module output current $\hat{i}_O$ and CS signal $\hat{V}_A$. To distinguish between large-signal and small-signal variables, the "hat" symbol is used for the latter. The module's internal loop dynamics are described by gain $a(s)$ of the dependent voltage source and by closed-loop output impedance $Z_{CL}(s)$. The block diagram representing the stand-alone module model is shown in Fig. 3, where

$$H_V(s) = [R_{11} + 1/(s \cdot C_9)]/R_4$$

is the transfer function of error amplifier EA;

F_M is the PWM gain (for analysis purposes, $F_M = 1.0$ was assumed)

$$H_{VD}(s) = \hat{V}_O/\hat{d} = V_{IN} \cdot Z_{CF}(s)/[Z_{LF}(s) + Z_{CF}(s)]$$

is the power-stage transfer function from the duty ratio to the output voltage

$$Z_{LF}(s) = ESR_L + s \cdot L_F, Z_{CF}(s) = ESR_C + 1/(s \cdot C_F)$$

are impedances of the lumped output filter inductor and capacitor

$$Z_{OL}(s) = Z_{LF}(s) \cdot Z_{CF}(s)/[Z_{LF}(s) + Z_{CF}(s)]$$

is the VRM open-loop output impedance

$$K_1 = \hat{i}_X/\hat{i}_L = 7.19 \cdot 10^{-7}$$

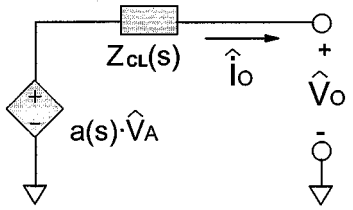

Fig. 2. Thevenin-source representation of a stand-alone VRM.

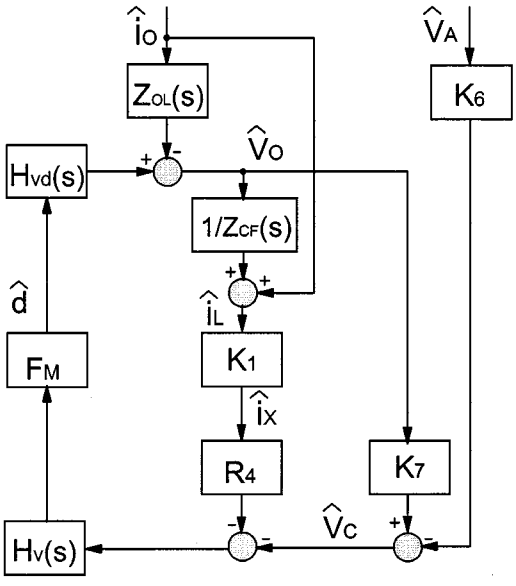

Fig. 3. Small-signal block diagram of a stand-alone VRM.

is the gain from the inductor current to the current, injected at the inverting input of amplifier EA1 (K_1 value selection is based on the desirable value of the droop resistance)

$$K_6 = \hat{V}_{C1}/\hat{V}_{A1} = R_9/R_{13}$$

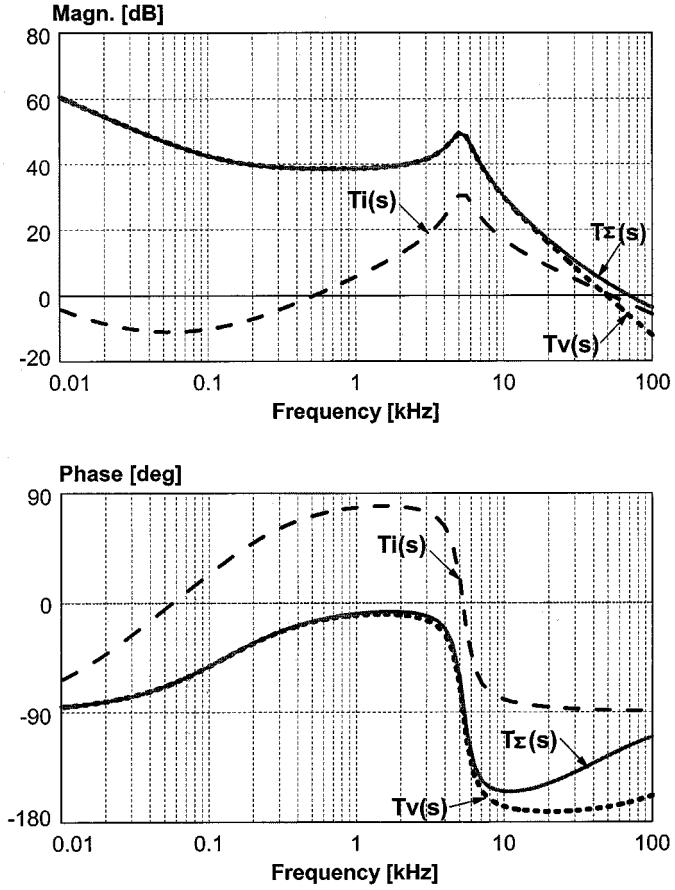

Fig. 4. Calculated Bode plots of VRM loop gains $T_V(s), T_I(s)$, and $T_\Sigma(s)$.

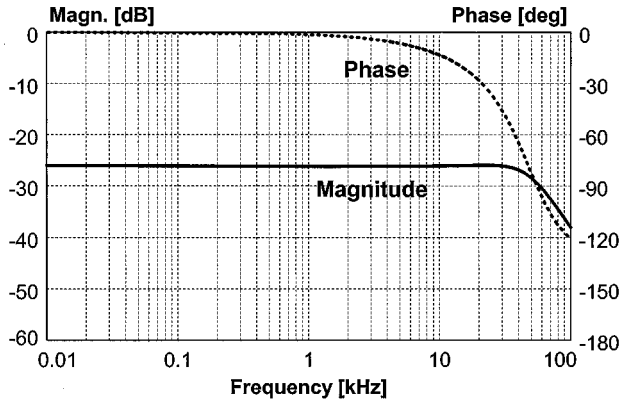

Fig. 5. Calculated Bode plots of transfer function $a(s)$.

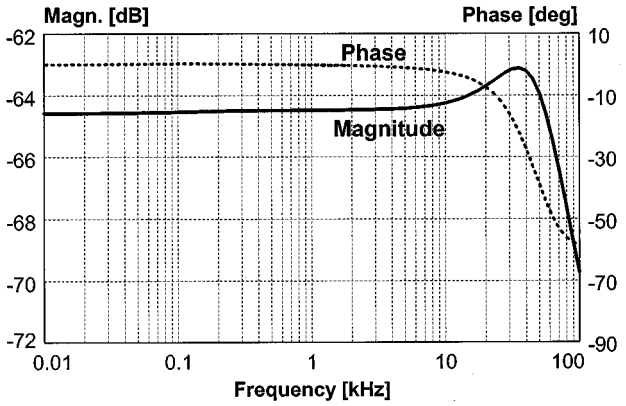

Fig. 6. Calculated Bode plots of VRM output impedance $Z_{CL}(s)$.

is the gain from amplifier UA1 output voltage to amplifier UC1 output voltage

$$K_7 = \hat{V}_{C1}/\hat{V}_O = R_1 \cdot R_9 \cdot (1/R_9 + 1/R_{13} + 1/R_{18} + 1/R_{56})/(R_1 + R_{23})$$

is the gain from VRM output voltage to amplifier UC1 output voltage.

Note that, with the Thevenin-source modeling approach, all power-stage transfer functions are derived for a stand-alone module with a current-sink load. From the diagram in Fig. 3, the values of the Thevenin source components are

$$a(s) = \frac{K_6}{K_7} \cdot \frac{T_V(s)}{1 + T_\Sigma(s)} \tag{1}$$

$$Z_{CL}(s) = \frac{Z_{OL}(s) + K_1 \cdot R_4 \cdot H_V(s) \cdot F_M \cdot H_{VD}(s)}{1 + T_\Sigma(s)} \tag{2}$$

where loop gains $T_V(s), T_I(s)$ and $T_\Sigma(s)$ are defined as

$$T_V(s) = K_7 \cdot H_V(s) \cdot F_M \cdot H_{VD}(s) \tag{3}$$

$$T_I(s) = K_1 \cdot R_4 \cdot H_V(s) \cdot F_M \cdot H_{VD}(s)/Z_{CF}(s) \tag{4}$$

and

$$T_\Sigma(s) = T_I(s) + T_V(s). \tag{5}$$

Bode plots of loop gains $T_V(s), T_I(s)$, and $T_\Sigma(s)$ for the component values, indicated in Fig. 1, are shown in Fig. 4. As can be seen in Fig. 4, the contribution of component $T_I(s)$ to loop gain $T_\Sigma(s)$ is negligible at low frequencies, but becomes significant at high frequencies (above 10–20 kHz). Loop gain $T_\Sigma(s)$ which determines stability of the stand-alone module has the bandwidth of 70 kHz and the phase margin of 65°. Since the droop circuit introduces a virtual resistance at the module output, loop gain $T_I(s)$, associated with the droop circuit, increases the stability margin of loop gain $T_\Sigma(s)$.

The Bode plots of transfer function $a(s)$ are shown in Fig. 5. At low frequencies (below 10–20 kHz) transfer function $a(s)$ is well approximated by its DC gain K_6/K_7.

The Bode plots of closed-loop output impedance $Z_{CL}(s)$ are shown in Fig. 6. At the low frequencies, the magnitude and phase of closed-loop output impedance $Z_{CL}(s)$ are determined by the droop circuit. Namely, in the low-frequency range

$$Z_{CL}(s) \approx K_1 \cdot R_4/K_7. \tag{6}$$

Note that, if loop gain $T_\Sigma(s)$ is stable, both transfer functions $a(s)$ and $Z_{CL}(s)$ have no RHP poles.

The CS circuit, shown in Fig. 1, is represented by the block diagram in Fig. 7. Transfer functions of the blocks in Fig. 7 are defined as

$$K_2 = -\hat{V}_{CA1}/\hat{V}_{C1} = -\hat{V}_{CA2}/\hat{V}_{C2}$$

gains of current amplifiers CA1, CA2. (For analysis purposes, $K_2 = 49.7$ was assumed)

$$K_3(s) = \hat{V}_{BUS}/\hat{V}_{CA1} = \hat{V}_{BUS}/\hat{V}_{CA2} = 1/2 \cdot 1/[1 + R_{14}/(R_{15} + Z_{16}(s))]$$

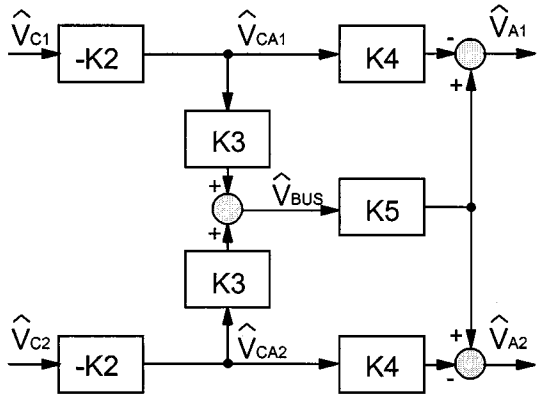

Fig. 7. Small-signal block diagram of the CS circuit.

transfer functions from output voltages of amplifiers CA1, CA2 to the CS bus voltage

$$K_4(s) = \hat{V}_{A1}/\hat{V}_{CA1} = \hat{V}_{A2}/\hat{V}_{CA2} = Z_{17}(s)/R_{12}$$

transfer functions from output voltages of amplifiers CA1 and CA2 to output voltages of amplifiers UA1 and UA2, respectively.

$$K_5(s) = \hat{V}_{A1}/\hat{V}_{BUS} = \hat{V}_{A2}/\hat{V}_{BUS} = Z_{16}(s) \cdot [1 + Z_{17}(s)/R_{12}][R_{15} + Z_{16}(s)]$$

transfer functions from the CS bus voltage to output voltages of amplifiers UA1 and UA2; where

$$Z_{16}(s) = 1/[1/R_{16} + s \cdot C_1], \quad Z_{17}(s) = 1/[1/R_{17} + s \cdot C_3].$$

Based on the diagram in Fig. 7, the relationship between input and output signals of the CS circuit is described by

$$\hat{V}_{A1} = b(s) \cdot \hat{V}_{C1} + b_{CC}(s) \cdot \hat{V}_{C2} \tag{7}$$

$$\hat{V}_{A2} = b_{CC}(s) \cdot \hat{V}_{C1} + b(s) \cdot \hat{V}_{C2} \tag{8}$$

where

$$b(s) = K_2 \cdot [K_4(s) - K_3(s) \cdot K_5(s)]$$

$$b_{CC}(s) = -K_2 \cdot K_3(s) \cdot K_5(s).$$

Ideally, $b_{CC}(s) = -b(s)$, and

$$\hat{V}_{A1}(s) = -\hat{V}_{A2}(s) = b(s) \cdot (\hat{V}_{C1} - \hat{V}_{C2}). \tag{9}$$

Note that current-sharing correction signals $\hat{V}_{A1}$ and $\hat{V}_{A2}$ depend solely on the output voltages $\hat{V}_{C1}$ and $\hat{V}_{C2}$ of amplifiers UC1 and UC2, but not on the output currents of the modules. This fact is related to implementation of the VRM IC controller. Namely, as shown in Fig. 1, current $\hat{i}_{X1}$, injected at the inverting input of error amplifier EA1, cannot produce any ac voltage drop across resistor R_4, since the ac potential of EA1 inverting input is equal to zero. Hence, the ac voltage across resistor R_4 is determined only by voltage $\hat{V}_{C1}$, and the ac input signal for the CS circuit does not contain direct information about the ac component of the module output current.

IV. Stability Analysis of Paralleled VRMs

Once modeling of a stand-alone VRM by the Thevenin source has been completed, the system of two paralleled VRMs can be represented by the mixed circuit/block diagram, as shown in Fig. 8. Although this system representation is not conventional,

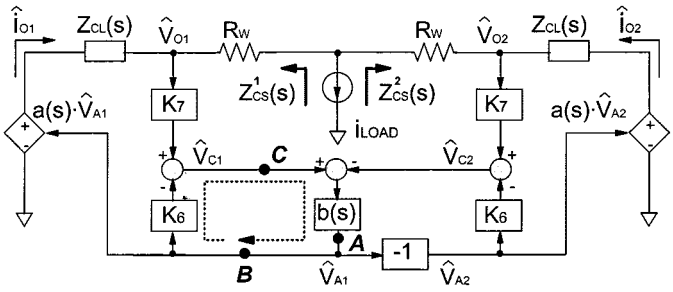

Fig. 8. Small-signal circuit/block diagram of paralleled VRMs with the CS circuit.

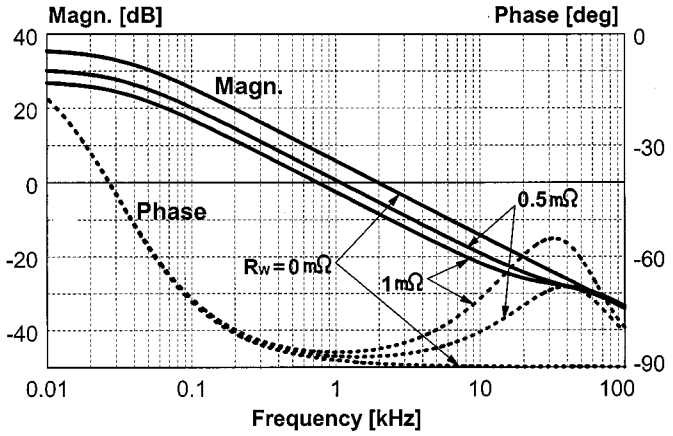

Fig. 9. Calculated Bode plots of CS loop gain $T_{CS}(s)$.

it is used in this paper since it provides more compact representation of the current-sharing control than does the conventional block diagram.

Loop gain $T_{CS}(s)$ which determines stability of the current-sharing control is derived by opening the CS loop at point A in Fig. 8. In the case of identical modules, derivation produces the following result:

$$T_{CS}(s) = 2 \cdot b(s) \cdot \left[K_6 - K_7 \cdot a(s) \cdot \frac{R_W}{R_W + Z_{CL}(s)}\right]. \tag{10}$$

If VRM internal loop gain $T_\Sigma(s)$ is stable, CS loop gain $T_{CS}(s)$ has no RHP poles. As a result, stability of the CS loop can be assessed by inspection of $T_{CS}(s)$ Bode plots. The Bode plots of CS loop gain $T_{CS}(s)$ for several values of interconnect wire resistance R_W are shown in Fig. 9. As resistance R_W increases, the magnitude of the CS loop gain decreases, and its phase increases at the frequencies above 1–2 kHz. Within the practical of R_W values (0–1 mΩ), $T_{CS}(s)$ bandwidth varies from 0.75 kHz to 2 kHz, and the corresponding phase margin exceeds 90°. The lowest stability margin is observed when $R_W = 0$, i.e., when remote voltage sensing is used. In this case, expression for the CS loop gain simplifies to

$$T_{CS}(s) = 2 \cdot b(s) \cdot K_6. \tag{11}$$

Therefore, in the case of remote voltage sensing, the CS loop gain is solely determined by the local feedback loop within the CS controller, as shown by the dashed curve in Fig. 8.

Equations (10) and (11) for gain $T_{CS}(s)$ provide the foundation for the design of CS loop compensator transfer function

$b(s)$ in the frequency domain. The values of $T_{CS}(s)$ bandwidth and stability margins can be included in the VRM specifications which assure the compatibility of modules from different manufacturers. However, these tasks can be accomplished only if loop gain $T_{CS}(s)$ can be measured and verified on the hardware. Unfortunately, the CS circuit has no physical point that corresponds to point A on the block diagram in Fig. 8. Moreover, for proper $T_{CS}(s)$ measurement, opening of the physical CS loop must disable all the feedbacks associated with CS control. However, the real circuit has no points which satisfy this criterion. Therefore, an indirect method of the CS loop gain measurement has to be found before gain $T_{CS}(s)$ can be accepted as a basis for the small-signal design and dynamic performance specifications.

V. Current-Sharing Loop Gain Measurement

In practical measurements of a loop gain with a high dc value, the control loop is kept closed. Instead of opening the loop, an excitation voltage source is inserted in the control path between the source and load subcircuits. Then, the loop gain is determined as the ratio of the voltages on both sides of the excitation source. For proper measurement, the impedance of the source subcircuit should be much less than one of the load subcircuit. This condition is usually satisfied when the excitation source is applied at the input or the output of an operational amplifier, which generally has a very high input impedance and a very low output impedance. In the CS circuit, the excitation source can be inserted either at the output of CS error amplifier UA1 or at the input of amplifier CA1 that correspond to points B and C on the diagram in Fig. 8. Derivation of the loop gain corresponding to breaking the CS loop at points B and C produces the same result

$$T^1_{CS}(s)=\frac{b(s)\cdot\left[K_6-K_7\cdot a(s)\cdot\frac{R_W}{R_W+Z_{CL}(s)}\right]}{1+b(s)\cdot\left[K_6-K_7\cdot a(s)\cdot\frac{R_W}{R_W+Z_{CL}(s)}\right]}$$

or

$$T^1_{CS}(s)=\frac{T_{CS}}{2+T_{CS}}. \tag{12}$$

One can easily prove that loop gains $T^1_{CS}(s)$ and $T_{CS}(s)$ have the same characteristic polynomial. However, the last equation implies that loop gain $T^1_{CS}(s)$, which can be measured experimentally, differs significantly from $T_{CS}(s)$. Equation (12) also provides an opportunity to recover gain $T_{CS}(s)$ based on the $T^1_{CS}(s)$ measurement

$$T_{CS}(s)=\frac{2\cdot T^1_{CS}}{1-T^1_{CS}}. \tag{13}$$

Although the gains are linked by unique and simple relationship (13), the recovery of $T_{CS}(s)$ based on $T^1_{CS}(s)$ measurement presents a serious practical challenge. When $T^1_{CS}(s)$ magnitude is close to unity, the value of the recovered gain is very sensitive to $T^1_{CS}(s)$ measurement errors.

In this paper, a method of indirect measurement of CS loop gain $T_{CS}(s)$, that is much less sensitive to measurement errors, is proposed. The proposed measurement method includes three steps.

1) The CS loop of VRM #2 is opened by disconnecting resistor R_{13} from the opamp UA2 output and by grounding the disconnected lead of the resistor (see Fig. 1).

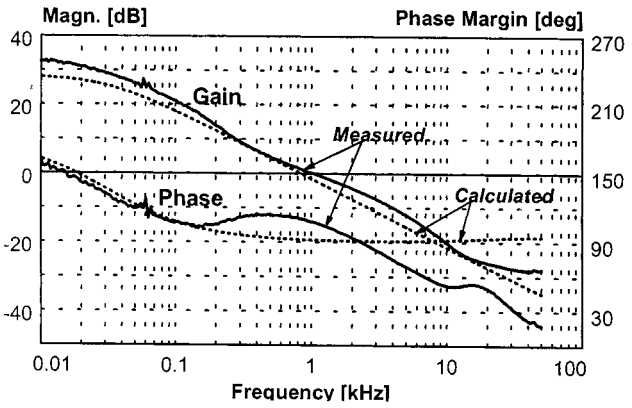

Fig. 10. Measured and calculated Bode plots of CS loop gain $T^2_{CS}(s)$.

2) Excitation signal $\hat{V}_E$ is injected between the output of opamp UA1 of VRM #1 and resistor R_{13} in Fig. 1 (at point B in Fig. 8).
3) The CS loop gain $T^2_{CS}(s)$ is measured as the ratio of the voltages on the both sides of excitation source $\hat{V}_E$: $T^2_{CS}(s)=-\hat{V}_{A1}/(\hat{V}_{A1}+\hat{V}_E)$.

Derivation of CS loop gain $T^2_{CS}(s)$ is based on the diagram in Fig. 8 and takes into account that $\hat{V}_{A2}=0$. The derivation result is

$$T^2_{CS}(s)=b(s)\cdot\left[K_6-K_7\cdot a(s)\cdot\frac{R_W}{R_W+Z_{CL}(s)}\right]=\frac{1}{2}\cdot T_{CS}. \tag{14}$$

Based on (14), CS loop gain $T_{CS}(s)$ can be recovered from $T^2_{CS}(s)$ measurement by simply increasing the magnitude of the latter gain by 6 dB. The recovery of loop gain $T_{CS}(s)$ based on $T^2_{CS}(s)$ measurement is much more tolerable to measurement errors than in the previously considered case.

If the paralleled modules are far from being identical, the similar measurement of the CS loop gain $T^2_{CS}(s)$ should be conducted by opening the CS loop of VRM #1 at the amplifier UA1 output and by injecting the excitation signal at the output of amplifier UA2. It can be shown that the CS loop gain of two nonidentical modules is equal to the sum of these two measured loop gains. In practice, however, parameters of the CS loops of paralleled VRMs are tightly matched, since their matching is the prerequisite for the good steady-state current sharing.

Fig. 10 shows Bode plots of measured and calculated CS loop gain $T^2_{CS}(s)$. The magnitude plots show reasonable agreement between the model and measurement. At the same time, there is a significant phase discrepancy in the frequency range above 2 kHz. Therefore, the proposed model can be used confidently for design purposes if the required CS loop gain bandwidth does not exceed 2 kHz.

VI. Dynamic Current Sharing of Paralleled VRMs

Generally, the current sharing during load transients can be evaluated in the frequency domain by comparing output impedances of the individual modules, observed at the load point [7].

Without the CS loop, individual VRMs have different output impedances $Z^1_{CL}(s)+R^1_W$ and $Z^2_{CL}(s)+R^2_W$ due to the mismatch of their power-stage and voltage-feedback parameters. Parameters of the CS control loops are considered matched, since otherwise it is impossible to achieve decent steady-state current sharing. In practice, tight-tolerance components are used to match the CS loops of paralleled VRMs. Because of different output impedances $Z^1_{CL}(s)+R^1_W$ and $Z^2_{CL}(s)+R^2_W$, the VRM output currents during the load transients can differ significantly. The purpose of the CS loop is to modify individual output impedances $Z^1_{CL}(s)+R^1_W$ and $Z^2_{CL}(s)+R^2_W$, observed at the load point before closing the CS loop, in a such way that output impedances $Z^1_{CS}(s)$ and $Z^2_{CS}(s)$, observed after closing the CS loop, match each other. Matching of impedances $Z^1_{CS}(s)$ and $Z^2_{CS}(s)$ can be accomplished only within the bandwidth of the CS loop.

Derivation of the output impedances of paralleled nonidentical VRMs is based on the diagram in Fig. 8 and yields

$$Z^1_{CS}(s)=\frac{R^1_W+Z^1_{CL}(s)}{1+\frac{a_1(s)\cdot b(s)\cdot K_7\cdot[g_1(s)-g_2(s)]}{1+T_{CS}}} \tag{15}$$

$$Z^2_{CS}(s)=\frac{R^2_W+Z^2_{CL}(s)}{1-\frac{a_2(s)\cdot b(s)\cdot K_7\cdot[g_1(s)-g_2(s)]}{1+T_{CS}}} \tag{16}$$

where

$$T_{CS}(s)=b(s)\cdot[2\cdot K_6-K_7\cdot(a_1(s)\cdot g_1(s)+a_2(s)\cdot g_2(s))] \tag{17}$$

is the CS loop gain of nonidentical modules, and

$$g_1(s)=\frac{R^1_W}{R^1_W+Z^1_{CL}(s)},\quad g_2(s)=\frac{R^2_W}{R^2_W+Z^2_{CL}(s)}. \tag{18}$$

Note that, if impedances $Z^1_{CL}(s)+R^1_W$ and $Z^2_{CL}(s)+R^2_W$ are matched, i.e., if $g_1(s)=g_2(s)$, the CS loop has no effect on the output impedances of the modules.

Within the CS loop bandwidth, where $T_{CS}\gg 1$, (15) and (16) can be simplified as

$$Z^1_{CS}(s)=\frac{R^1_W+Z^1_{CL}(s)}{1+\frac{a_1(s)\cdot K_7\cdot[g_1(s)-g_2(s)]}{2\cdot[K_6-K_7\cdot(a_1(s)\cdot g_1(s)+a_2(s)\cdot g_2(s))]}} \tag{19}$$

$$Z^2_{CS}(s)=\frac{R^2_W+Z^2_{CL}(s)}{1-\frac{a_2(s)\cdot K_7\cdot[g_1(s)-g_2(s)]}{2\cdot[K_6-K_7\cdot(a_1(s)\cdot g_1(s)+a_2(s)\cdot g_2(s))]}}. \tag{20}$$

As it was demonstrated in Section II, at the frequencies below 10–20 kHz, VRM output impedances $Z^1_{CL}(s)$ and $Z^2_{CL}(s)$ are programmed by the droop circuits of the modules and can be approximated by their dc values. These dc values have to be accurately matched in order not to exceed specified value of the steady-state CS error. If impedances $Z^1_{CL}(s)$ and $Z^2_{CL}(s)$ are matched, then impedances $Z^1_{CL}(s)+R^1_W$ and $Z^2_{CL}(s)+R^2_W$, observed at the load point before closing the CS loop, are also matched, if $R^1_W=R^2_W$. The last condition is satisfied if VRMs have a symmetrical layout with respect to the load. It is also satisfied if the remote sensing of VRM output voltages is implemented: $R^1_W=R^2_W=0$.

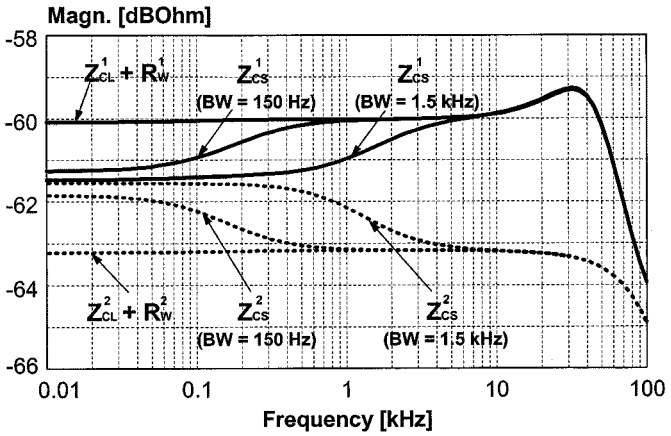

Fig. 11. Magnitude plots of VRM output impedances, observed before and after closing the CS loop.

TABLE I
PARAMETERS OF NONIDENTICAL MODULES

	V_{REF} [V]	L_F [nH]	C_F [mF]	F_M [V^{-1}]	C_9 [nF]	R_W [mΩ]
VRM #1	1.515	75	3.0	2.0	176	0.1
VRM #2	1.485	150	6.0	1.0	264	0.4

When impedances $Z^1_{CL}(s)+R^1_W$ and $Z^2_{CL}(s)+R^2_W$ are matched at low frequencies, improvement of their matching at higher frequencies can be accomplished only if the CS loop has a bandwidth well above 10–20 kHz. However, practical design of the CS loop with the bandwidth above 10–20 kHz can hardly be accomplished. It violates the well-known guideline that the bandwidth of the CS loop should be selected much lower than the one of the voltage feedback loop which is typically in the 20–100 kHz range. Violation of this guideline can cause severe interactions between CS and voltage loops that affect the system stability. Since practical matching of impedances $Z^1_{CL}(s)+R^1_W$ and $Z^2_{CL}(s)+R^2_W$ at high frequencies is not feasible, low bandwidth of the CS loop has no negative impact on the dynamic performance of paralleled VRMs.

When interconnect impedances R^1_W and R^2_W are not matched, (19) and (20) indicate that the CS loop changes individual module output impedances in the direction of their convergence. For example, if $R^1_W>R^2_W$, then $g_1(s)>g_2(s)$, and by the CS loop action the impedance of VRM #1 is reduced from $Z^1_{CL}(s)+R^1_W$ to one specified by (19), whereas the impedance of VRM #2 is increased from $Z^2_{CL}(s)+R^2_W$ to one specified by (20). Therefore, matching of impedances R^1_W and R^2_W is not critical, but, to compensate for this mismatch during load transients, the CS loop must have sufficient bandwidth. To illustrate this point, Fig. 11 shows calculated magnitude plots of output impedances $Z^1_{CS}(s)$ and $Z^2_{CS}(s)$, observed after closing the CS loop, as well as impedances $Z^1_{CL}(s)+R^1_W$ and

TABLE II
MEASURED CURRENT-SHARING ACCURACY OF TWO PARALLELED VRMS

i_{LOAD} [A]	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	90.0	100.0
i_{O1} [A]	6.5	11.3	16.3	21.3	26.1	31.0	35.8	40.7	45.5	50.2
i_{O2} [A]	3.5	8.7	13.7	18.7	23.9	29.0	34.2	39.3	44.5	49.8
CS error [%]	30.0	13.0	8.7	6.5	4.4	3.3	2.3	1.9	1.1	0.4

$Z^2_{CL}(s) + R^2_W$, observed before closing the loop. This data was obtained for nonidentical modules whose parameters are summarized in Table I. The modules were assumed to have the same droop impedance $Z^1_{CL}(0) = Z^2_{CL}(0)$, but different interconnect resistance $R^1_W \neq R^2_W$. The magnitudes of impedances, shown in Fig. 11, were calculated for two values of the CS loop bandwidth: 150 Hz and 1.5 kHz. Comparison of the plots in Fig. 11 clearly demonstrates that high bandwidth of the CS loop is essential for matching of the modules' output impedances.

To validate the analysis results in the time domain, the setup of two paralleled 12-V/1.6-V, 50-A VRMs with the local output voltage feedback was assembled. The measured references of the modules were 1.603 V and 1.576 V that is within $\pm 1\%$ tolerance band. At the same time, measured droop impedances $Z^1_{CL}(0)$ and $Z^2_{CL}(0)$ were tightly matched and were equal to 0.45 mΩ. For reader's reference, Table II shows the measured current-sharing accuracy of the paralleled modules under steady-state conditions. In the 30–100 A load range, the current-sharing error, which is defined as $|I_{01} - I_{02}|/(I_{01} + I_{02})$, does not exceed 10%. The response of the individual module currents to the dynamic load is shown in Fig. 12. The waveforms in Fig. 12(a) correspond to the CS loop bandwidth of 1 kHz. To obtain the waveforms in Fig. 12(b), the loop bandwidth was decreased from 1 kHz to 300 Hz by increasing the values of capacitors C1 and C3 in Fig. 1 from 10 nF to 43 nF. Comparison of the waveforms in Figs. 12(a) and (b) reveals that reduction of the CS bandwidth does not significantly affect the overshoots of the modules' currents, but causes the increase of settlement time after the load step-up by approximately two times. Presented experimental results testify that good dynamic current sharing requires the wide bandwidth of the CS loop.

This section concentrates on analysis of the VRMs' small-signal load transients. However, the VRM load can change from almost zero current to the maximum one with the extremely high current slew rate. In that case, the large-signal load transient can be affected by VRM nonlinearities, such as duty ratio saturation, amplifier output voltage saturation and limited slew rate, output inductor saturation, etc. Usually these nonlinearities negatively affect the control loop performance, and the designer's objective is to avoid current-sharing loop operation in the nonlinear mode. With the proper design of the CS circuitry, the current sharing during large-signal load transients is determined mostly by the small-signal behavior.

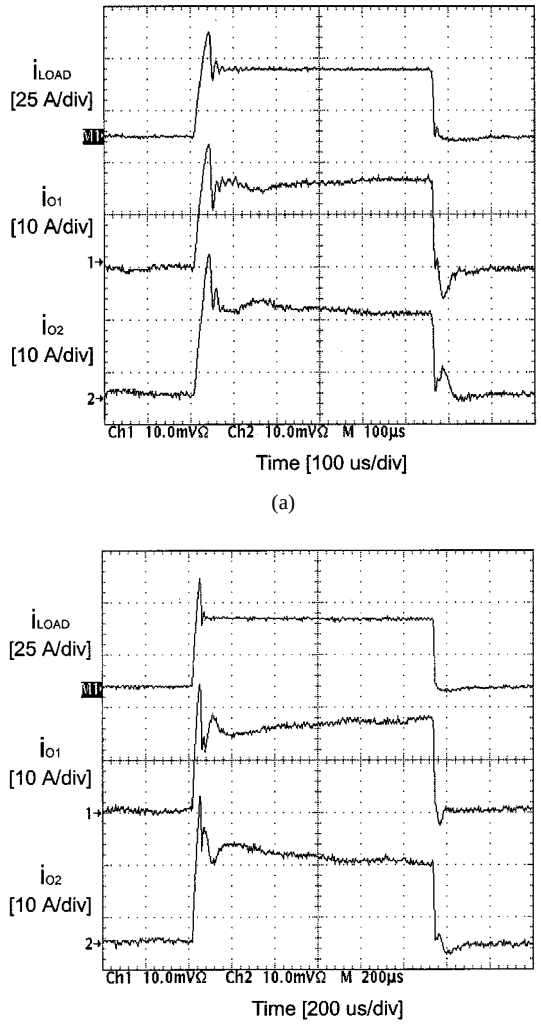

Fig. 12. Measured response of two paralleled VRMs to the dynamic load: (a) 1-kHz current-sharing loop bandwidth and (b) 300-Hz current-sharing loop bandwidth.

VII. SUMMARY

VRM current sharing relies simultaneously on the droop current sharing and on the feedback control loop which effectively adjusts references of the paralleled modules based on the differences between individual module currents. To assess the stability and dynamic performance of the CS control, a comprehensive small-signal model of the paralleled VRMs was developed. In addition, the CS loop gain, which determines the stability of

the CS control and which can be verified by hardware measurements, was identified. Finally, it was found that a wide bandwidth of the CS loop is important for dynamic current sharing between VRMs with unmatched interconnect impedances.

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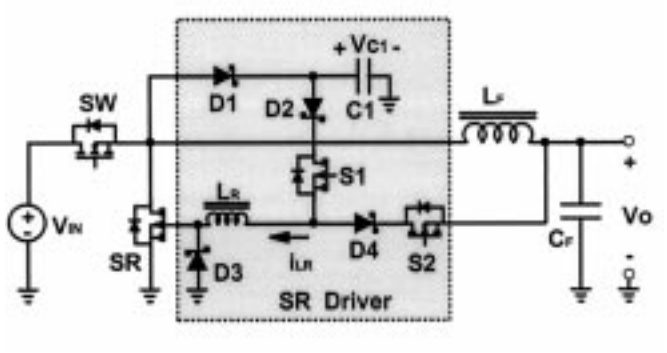
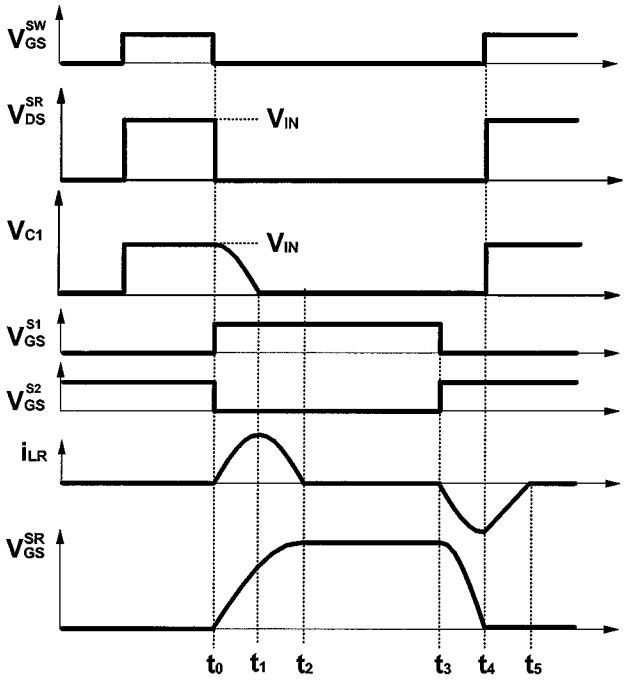
Correction to "Design Considerations for 12-V/1.5-V, 50-A Voltage Regulator Modules"

Yuri Panov and Milan M. Jovanović

In the above paper,[1] Fig. 6(b) was shown in place of Fig. 6(a). The correct Fig. 6(a) and (b) are shown here.



(a)



(b)

Fig. 6. Resonant SR driver: (a) circuit diagram; (b) idealized waveforms.

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