Stability and Reliability of Lateral GaN Power Field-Effect Transistors

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(Invited Paper)

***Abstract*— GaN electronics constitutes a revolutionary technology with power handling capabilities that amply exceed those of Si and other semiconductors in many applications. RF, microwave, and millimeter-wave GaN-based power amplifiers are now deployed in commercial communications, radar, and sensing systems. GaN power transistors for electrical power management are also starting to reach the marketplace. From the dawn of this technology, inadequate transistor stability and reliability have represented stumbling blocks preventing widespread commercial use of GaN electronics. Intense research has been devoted to addressing these issues, and great progress has taken place recently. This article reviews some of the most interesting and significant stability and reliability issues that have plagued GaN power field-effect transistors for RF and power management applications.**

***Index Terms*— AlGaN, GaN, power transistors, reliability, stability.**

I. Introduction

SINCE the first demonstration of modulation doping in an AlGaN/GaN heterostructure in 1991 [1] and the first realization of an AlGaN/GaN high electron mobility transistor (HEMT) in 1993 [2], GaN electronics has come a long way. By just about any benchmark, GaN constitutes a breakthrough electronics technology with an extraordinary future for RF power and power switching applications.

There are multiple elements behind the success of GaN electronics. GaN's package of semiconducting properties is unique, with its wide bandgap standing out as the key behind its high critical electric field which enables high-voltage applications [3]. The outstanding perfection of the epitaxially grown AlGaN/GaN interface, manifested in the observation of the fractional quantum-Hall effect [4], yields a 2-D electron gas (2DEG) with high mobility, the key for high-frequency operation [4]. The strong spontaneous and piezoelectric polarization of these materials results in a 2DEG with a high electron concentration which can support high-current density [5]. Hugely significant from a technological point of view has also been the ability to preserve these and other outstanding properties in heterostructures grown on foreign substrates, such as SiC or Si, despite a large density of crystallographic defects. The excellent thermal conductivity and semi-insulating characteristics of SiC substrates have enabled high-performance AlGaN/GaN HEMTs for RF power applications. High-quality growth on large-diameter Si wafers has made it possible to leverage 8-in legacy Si manufacturing fabs and approach Si-like economics which is of great significance for large volume and cost-sensitive power management products.

Many reviews have been dedicated to exult the properties of the GaN semiconductor system and its revolutionary impact in RF power and power management applications [6]–[10]. Commercial deployment of these technologies is well on their way with about a ten-year advantage for RF power markets [9], [11].

A recurring concern about GaN electronics has been the stability and reliability of GaN transistors. First with HEMTs for RF power and then with metal–insulator–semiconductor (MIS) HEMTs for power management systems, understanding the main failure mechanisms, mitigating them, and ensuring long-term operational success has been the object of intense research. Numerous reviews have periodically summarized progress in this endeavor [12]–[15]. The good news is that these efforts are paying off handsomely, as the commercial impact of GaN electronics already certifies and its serious considerations for space missions attests [16].

This article represents an attempt to summarize current understanding of some of the most relevant and interesting stability and reliability concerns of power GaN FETs. The literature is vast, and space is limited. Editorial discretion is then paramount. With vertical transistor structures at their infancy, only lateral field-effect transistors are discussed.

This article tries to separate stability from reliability issues. In practice, they often come intricately wrapped together, but their impact on device operation and mitigation measures are very different.

Stability refers to *recoverable* changes in the device electrical characteristics as a result of sustained operation. These are due to trapping and floating body effects. There is no permanent damage to the device, but its behavior is not well described by standard equivalent circuit models [17]. In consequence, predictive operation under all possible eventualities is difficult.

Reliability refers to nonrecoverable changes in transistor characteristics, including the introduction of new traps. These can take place through various failure mechanisms which need to be understood, quantified, and mitigated.

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This article is organized as follows. Section II deals with transistor stability issues. First, GaN HEMTs are treated; then, a few unique issues associated with the introduction of a gate dielectric into MIS-HEMTs are discussed. Section III describes some of the most relevant reliability mechanisms, first for HEMTs and then for MIS-HEMTs. Finite space limits the number of topics that can be treated at enough depth. Section IV gives a brief overview of the stability and reliability issues of p-GaN gate HEMTs. This emerging technology currently represents the best prospect for the realization of high-performance enhancement-mode ($V_T > 0$) devices for power management applications.

II. Stability of GaN HEMTs and MIS-HEMTs

GaN HEMT stability is a serious concern. It is important in itself as predictable device behavior in a real-world operating environment is essential. Further, poor device stability complicates the interpretation of reliability studies. Many degradation mechanisms are electric field driven. Severe trapping can greatly affect the local electric field, impacting the rate of degradation.

Device instability mainly arises from the presence of traps in various regions of the device. The occupation probability of these traps depends on its electrical history. Trapping behavior (trapping and detrapping) is often characterized by time constants that can span many orders of magnitude [18].

Trapping studies are nontrivial. A key consideration is that trapping studies should not create additional traps or introduce permanent degradation. Accomplishing this involves the following.

1) An *initialization step* for a virgin device that erases its prior history and establishes a well-defined reference starting point. A moderate bake such as 100 °C, 30 min is often adequate.
2) A benign but effective *detrapping step* to distinguish recoverable trapping from nonrecoverable permanent degradation. Often, simple microscope light is effective. In some cases, UV light is needed. When light is ineffective, a moderate thermal bake often works.
3) A benign *characterization suite* to monitor the evolution of device characteristics without permanently affecting them. This imposes limits on the voltage and current range, maximum temperature and testing time. Characterization suites often include transfer/subthreshold characteristics over a limited V_{GS} range with V_{DS} in the linear regime plus spot measurements under saturated conditions at high V_{GS} and medium V_{DS}. Typical figures of merit that are extracted are linear drain current, I_{Dlin}, saturated drain current, I_{Dsat}, linear or saturated threshold voltage, V_T, peak transconductance, $g_{m,\mathrm{pk}}$, on resistance, R_{ON}, source resistance, R_S, drain resistance, R_D, linear or saturated subthreshold swing, S, ON-state gate current, I_{Gon}, OFF-state gate current, I_{Goff}, plus some measure of current collapse [19]. All these metrics should be defined at bias points appropriate to the device characteristics and the application environment.

Trapping phenomena are often studied through pulsed I–V experiments. Both the trapping and detrapping transients contain valuable information. A powerful methodology to analyze current transients is the time-constant spectrum technique [20], which comes in different variants [21].

We now discuss some of the most prevalent trapping processes observed in AlGaN/GaN HEMTs. In Section II-B, we address unique trapping issues associated with the presence of a gate dielectric in GaN MIS-HEMTs.

A. Trapping Phenomena in AlGaN/GaN HEMTs

Trapping phenomena and the region of the device responsible for it depend on stress conditions. Trapping in the intrinsic portion of the transistor (in this article this refers to the gate stack and includes the channel directly underneath) is best isolated through experiments under $V_{\mathrm{DS}} \approx 0$ conditions. In this regime, the lateral electric field along the channel is negligible and there are minimum hot-electron and self-heating effects.

Trapping in the $V_{\mathrm{GS}} > 0$, $V_{\mathrm{DS}} \approx 0$ regime has received little study. Due to its Schottky gate structure, there is a limited range of positive V_{GS} that can be applied to GaN HEMTs before gate leakage current becomes excessive.

With sustained $V_{\mathrm{GS}} < 0$ and $V_{\mathrm{DS}} \approx 0$, if $|V_{\mathrm{GS}}|$ is not too high to introduce permanent damage, the magnitude of I_G shrinks over time [20], [22], [23]. I_{Dlin} and I_{Dsat} also drop and R_{ON} increases. Terms such as current collapse or dynamic R_{ON} are often used to describe this [20], [23]–[25]. Simultaneously to the onset of these phenomena, an increase in the gate Schottky barrier height has been observed [25]. Very slow trapping transients, in the few second range at room temperature (RT), are generally observed. The drop in poststress I_D increases with stress $|V_{\mathrm{GS}}|$ [19], [24], it correlates with the value of stress I_G [24] and is thermally activated [20].

Detrapping transients of I_G and I_D provide further insights [25]. These are also generally slow, in the few second range at RT, with very well-defined time constants that are thermally activated [20], [25]. For medium times (~10s of s at RT), I_D recovers but I_G drops with time [25]. For longer times (~1000s of s), both I_D and I_G recover in sync [25].

There are then two different trapping mechanisms in action in two different regions of the device: the AlGaN barrier and the GaN channel under the edges of the gate where the electric field peaks. Both phenomena conspire to produce a positive V_T shift [21], [24], [26] and an increase in access resistance [25].

The OFF-state, characterized by $V_{\mathrm{GS}} < V_T$ and $V_{\mathrm{DS}} > 0$, is very relevant for power applications and has been studied extensively. The OFF-state parallels the situation under $V_{\mathrm{GS}} < V_T$, $V_{\mathrm{DS}} \approx 0$ conditions except that the electric field peak appears under the edge of the gate on the drain side only, as opposed to both sides.

A detailed study of dynamic R_{ON} over a span of ten decades in time after high V_{DS} OFF-state stress has revealed a rich spectrum of time constants (Fig. 1) [18]. There are relatively long time constants (~1 ms to 100s of s at RT) that are thermally activated with E_a between ~0.57 and 1.1 eV, consistent with observations under $V_{\mathrm{DS}} \approx 0$ conditions and many other experiments [27]. In addition, much shorter

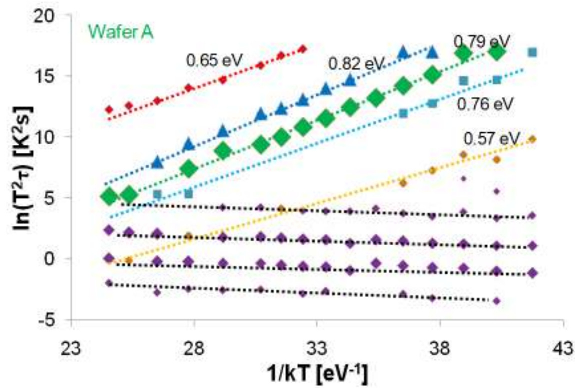

Fig. 1. Arrhenius plot of time constant spectra of R_{ON} recovery transient following an OFF-state stress pulse [18]. The size of the symbols is proportional to the height of the time constant peak in the time constant spectrum analysis. A number of relatively slow thermally activated traps are identified. A set of short time constants, independent of temperature, are also observed. These are responsible for the fast transients.

time constants ($\sim$1 μs to 100s of ms at RT) that are rather temperature independent were also identified. This suggests the existence of fast tunneling-limited trapping/detrapping processes, or perhaps floating-body effects, as discussed below. Temperature-independent trapping could be associated with interface states at the AlGaN/AlN interface right above the channel [28]. A thin AlN layer is often placed directly above the GaN channel with the goal of achieving a smooth interface and good mobility. In addition, trapping in very shallow traps such as those attributed to dislocations could perhaps explain this [29].

The ON-state ($V_{GS} > V_T$, $V_{DS} > 0$) is a regime of importance for HEMT RF power applications. Trapping during ON-state stress can be monitored through I_D. In general, I_D is observed to fall with time and the drop becomes more severe as V_{DS} increases [20]. Several time constants typically emerge [20]. A long thermally activated time constant with a signature that resembles AlGaN trapping under $V_{GS} < 0$, $V_{DS} = 0$ conditions in the same device has been reported [20]. The same study has also revealed a temperature-independent time constant reflecting trapping that takes place through a tunneling process [20]. The magnitude of the transient associated with this time constant increases with V_{DS}. This suggests that channel electrons are getting trapped deep in the buffer as a result of the high electric field or perhaps at the AlGaN/AlN/GaN interface, as in [18]. I_{Dlin} detrapping transients after the ON-state pulse paint a mirror-image picture of this [20].

In a separate study over a broader time range [18], in a situation in which slow T-activated time constants and fast T-independent time constants were evident after OFF-state stress (discussed above), only fast T-independent time constants were observed during the detrapping process that followed an ON-state trapping pulse. The magnitude of the R_{ON} increases after ON-state stress was found to increase with V_{DS} and I_D and followed a clear hot-electron-type law [30]. This suggests that channel electrons acquired kinetic energy from the high field at the drain end of the channel and became trapped in the vicinity. This type of trapping has been reported in [31] and [32]. The affected location could be the GaN channel, the GaN buffer, or the AlGaN/AlN interface in the high field region next to the drain edge of the gate.

In addition to trapping, buffer floating effects and leakage has also been found to greatly affect dynamic R_{ON} [33]. In fact, a "leaky dielectric" model has provided adequate explanation of the V_{DS} dependence of dynamic R_{ON} [33]. In this model, the high-resistivity (slightly p-type) C-doped GaN buffer layer acts as a resistive backgate to the transistor affecting the 2DEG electrostatics. Suppression of this effect requires either a perfectly insulating GaN buffer, something difficult to accomplish, or a slightly leaky GaN buffer that provides conducting paths for holes from the 2DEG down to the GaN C-doped layer. Extended defects, such as dislocations, can provide the desired vertical leakage paths. Within this model and consistent with multiple experiments, buffer leakage and dynamic R_{ON} are in conflict with each other and are highly dependent on the GaN buffer layer design and processing. The leaky dielectric model has received validation through the demonstration of current collapse suppression through proton irradiation under optimized conditions [34].

The dynamic behavior of GaN HEMTs is generally highly dependent on wafer structure, epi growth conditions, vendors, and transistor fabrication process details [18], [33], [35]. There are many possible defects that act as trapping centers and also impact leakage: intentionally or unintentionally introduced impurities, such as C [36] or Fe [24], [37]; extended crystallographic defects, such as dislocations [29]; or point defects, such as interstitials, vacancies, or antisites [38]. Proper optimization of the GaN buffer structure and growth conditions, as well as careful management of electric field through field plates, has been proven effective in mitigating buffer-induced dynamic R_{ON} while achieving good isolation and high breakdown voltage [39]–[41].

Several experiments under various bias conditions have reported trapping dynamics that are impacted by surface conditions, such as SiN passivation [42], surface treatments [41], [43], ambient moisture [44], or fluorocarbon encapsulation [44]. Surface trapping can take place at the semiconductor surface next to the gate in situations in which a high electric field is present there. Surface trapping contributes to depleting the 2DEG underneath, thus increasing R_{ON}. This is sometimes referred to as the "virtual gate" effect [45], [46]. Appropriate surface passivation [45]–[47], the use of field plates [48], and the introduction of a GaN cap layer have all been shown effective in mitigating surface trapping.

B. Bias-Temperature Instability Associated With the Gate Dielectric of GaN MIS-HEMTs

The structure of a GaN MIS-HEMT is generally similar to that of an HEMT but incorporates a gate dielectric. Many of the same trapping issues that have been identified in AlGaN/GaN HEMTs and summarized in Section II-A also affect MIS-HEMTs and need not be repeated here. Current collapse has been observed under ON- and OFF-state stress

conditions [40], [41]. Special to MIS-HEMTs is the high voltage that is applied to the drain in the OFF-state and the high-frequency off–on switching experienced by the device. In this regard, the current collapse has been seen to ameliorate under hard-switching with respect to soft-switching conditions. This has been attributed to hole generation through impact ionization and compensation of trapped electrons [41].

The presence of a gate dielectric in an MIS-HEMT brings along new stability concerns [49]. In MOSFETs based on various semiconductor systems, the application of a sufficiently large gate voltage for prolonged periods of time has been shown to shift V_T as well as affect other electrical characteristics [50]–[55]. The effect, known as bias-temperature instability (BTI), is generally enhanced by temperature and stress voltage. If the stress voltage is not too high, this phenomenon is fully reversible. For n-channel devices, BTI is generally attributed to trapping and detrapping of electrons in defects that are present inside the gate dielectric in virgin devices [56]. Under harsher stress, interface states at the dielectric–semiconductor interfaces can also be formed [57]. This is a nonrecoverable process and is discussed below.

Prominent BTI effects have been observed in GaN MIS-HEMTs with different dielectrics [58]–[62]. Consistent with studies in Si, Ge, SiC, and InGaAs MOSFETs, the sustained application of a relatively large and positive gate voltage to a GaN MIS-HEMT shifts V_T in the positive direction. ΔV_T increases with stress voltage, time, and temperature [58], [59]. This is known as positive BTI (PBTI). Negative gate stress has been seen to induce negative V_T shifts [59], [61]. This is known as negative BTI (NBTI). All these changes have been reported to be largely recoverable.

The complex structure of an MIS-HEMT, with many layers and interfaces, makes difficult a comprehensive study of this problem. From the Si MOSFET literature, it is reasonable to attribute BTI in GaN MIS-HEMTs to electron trapping in the gate dielectric. It is then advantageous to investigate these issues in a simpler GaN MOSFET platform [63]–[66].

Under the application of a relatively benign positive gate stress with $V_{DS} = 0$ (PBTI), V_T is observed to shift positive. The shift increases with time, stress voltage, and temperature [65], [66]. Along the way, g_m degrades, but the subthreshold swing, S, does not change. During the recovery phase, the device characteristics revert back to the virgin state. A nearly exact mirror-image picture is recorded in negative gate stress experiments (NBTI). There is also a striking one-to-one correlation between the changes in V_T and g_m during the stress and recovery phases for both PBTI and NBTI (Fig. 2). This "universal" behavior suggests a single physical origin for the observed phenomena. Further, during the stress phase, V_T shifts follow power laws in time and stress voltage for both NBTI and PBTI [65]. During the recovery phase, the evolution of V_T under all conditions also follows a relatively well understood universal recovery function [67].

All these results are in line with classic BTI as observed in Si, Ge, and InGaAs MOSFETs [50]–[55]. They are attributed to electron trapping and detrapping in a defect band that is present in the gate dielectric. The energy range and density of defects depend on the fabrication process details. For GaN,

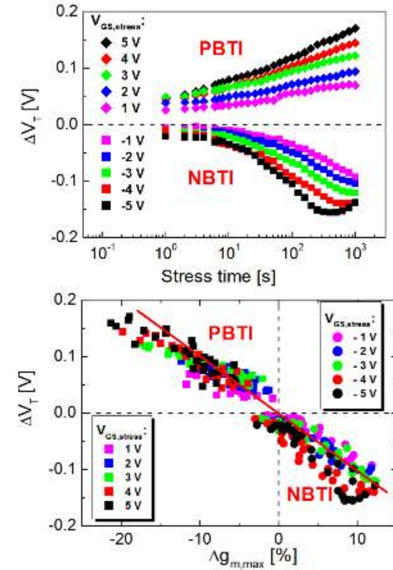

Fig. 2. Time evolution of ΔV_T in constant voltage stress experiments with $V_{GS,stress}$ from −5 to 5 V at RT (top). Correlation between ΔV_T and $\Delta g_{m,max}$ throughout stress for PBTI and NBTI experiments at RT (bottom). A virtually identical picture is observed during recovery. The universal relationship that is obtained suggests a common physical origin [65].

the defect band extends above and below its conduction band edge. This implies that at $V_{GS} = 0$, some defect states are empty and some are populated with electrons. During the stress phase, the electron occupation probability of dielectric defects increases or decreases depending on the sign of the voltage. This shifts V_T in either direction. Coulombic scattering associated with the changing density of trapped electrons close to the channel interface also affects channel mobility and transconductance [65].

While there is strong evidence of electron trapping in the gate dielectric as a primary source of V_T instability, trapping at interface states located at the dielectric/semiconductor interface is also a possibility. Distinguishing between the two mechanisms is not straightforward [68], and more detailed studies are needed.

There are many reports that indicate that the nature of the gate dielectric and its deposition and processing conditions significantly impact V_T stability [69]. A systematic comparison is difficult as different articles use different stress conditions and experiment designs. Nevertheless, the use of SiO_2 as gate dielectric has been reported to yield a more stable V_T under PBTI stress than Al_2O_3 [63]. N incorporation into the bulk of Al_2O_3 or at the interface with the semiconductor has been shown to improve V_T stability [70], [71]. Severe V_T shifts have been observed in devices that use SiN_x as gate dielectric [59], [68], [72], However, there are also reports that indicate that different deposition techniques yield widely different stability characteristics [59].

For D-mode MIS-HEMTs, PBTI is not a concern as $V_{GS} = 0$ V determines the ON-state. For E-mode devices, $V_{GS} > 0$ is used in the ON-state and gate dielectric trapping has been observed to be limited by dielectric/AlGaN interface charging [73]. In fact, a study involving different gate dielectrics

revealed a universal scaling behavior between the trapped charge and the free electron charge at the dielectric/AlGaN parasitic channel [73]. This suggests that in some situations, electrostatics are a major contributor to PBTI with the nature of the dielectric and its processing conditions playing a secondary role.

The Si MOSFET literature provides many suggestions to mitigate trapping in the gate dielectric. A thin wide bandgap interfacial layer can be introduced to pull apart the dielectric defects from the channel interface [74]. Reducing the thickness of the defective dielectric has also been seen to help [74]. In order to sustain a high voltage, this might require the use of a composite dielectric, as in [65]. Suitable postdeposition thermal treatments have also seen to be effective [75]. A thin interlayer that creates an interfacial dipole can be inserted to shift the dielectric defect band in energy with respect to the edge of the GaN conduction band [75]. Finally, minimizing gate current should help since it is the electrons responsible for I_G that get trapped in the dielectric [76].

III. Reliability of GaN HEMTs and MIS-HEMTs

This section deals with a few of the most prominent permanent degradation mechanisms in GaN power FETs.

A. Structural Degradation at Gate Edge in AlGaN/GaN HEMTs

In the early days of AlGaN/GaN HEMT development for microwave power applications, a serious reliability issue was reported in devices biased in the OFF-state or ON-state with progressively increasing V_{DS}. At a "critical" voltage, the device suffered a sudden, seemingly simultaneous and irreparable degradation of I_D, I_G, R_D, and a prominent increase in current collapse [77]. The suddenness of the onset and the comprehensiveness of the degradation suggested a critical phenomenon; hence, the term "critical voltage" was coined [19]. Subsequent experiments further noted the enhancing role of the electric field at the gate edge (rather than voltage or channel current) [15], stress time [78], temperature [78], and mechanical strain [77]. These observations were reproduced by many other groups on devices fabricated by different techniques on a variety of substrates [22], [23], [79]–[82]. Activation energies for I_D degradation of ~0.8–1.1 eV were reported [78], [83] in relative agreement with RF power life test results obtained on similar device technologies [84].

An initial hypothesis involving the inverse piezoelectric effect (IPE) was formulated [19], [77]. The application of a high electric field enhances tensile stress in the AlGaN barrier layer and increases the stored elastic energy. At some critical value, the elastic energy starts relaxing through the formation of crystallographic defects. These degrade I_D and provide conduction paths for excess I_G. The hypothesis matched most experimental observations at the time [15]. A first-order electromechanical model based on 2-D electrostatic simulations provided order of magnitude agreement with experiments [85].

The strong electric field dependence that was observed suggested the region next to the gate edge as the damage location. This intuition guided TEM investigations that resulted in the discovery of structural damage (pits, cracks) of the AlGaN surface right next to the gate edge [86]. In subsequent TEM studies, the depth of the damage was seen to correlate with the degree of I_D degradation and display the same dependencies [87]. These observations were also broadly reproduced [23], [79], [88]–[91]. The development of cracks, as initially observed in [86], was consistent with the IPE hypothesis. However, the appearance of pits was unexpected.

The introduction of a delamination technique to remove the gate and passivation layers of devices without damaging the surface provided a rich new perspective [92]. In step-stress experiments with increasing V_{DS}, AFM and SEM analysis revealed the formation of a shallow continuous groove on the semiconductor surface along the gate edge even for $V_{DSstress} < V_{crit}$. This was followed at a later stage with $V_{DSstress} > V_{crit}$, by the appearance of pits along the groove that increased in size as $V_{DSstress}$ was increased an eventually merged into trenches [92], [93]. The average cross-sectional area of the structural defects correlated well with the degree of I_D degradation. These observations were also reproduced by other authors in a diversity of device structures [88], [94]–[97].

From early on, the pattern of degradation in the ON-state matched quite closely that of the OFF-state or the $V_{GS} < 0$, $V_{DS} \approx 0$ state. Yet, detailed studies in the ON-state were complicated by device self-heating. A manifestation of this is the observation of increasing structural degradation at the edge of the gate finger along its length toward the center of the device where the temperature is the highest [93], [98]. Studies in nominally identical devices under closely matched junction temperature and electric field conditions revealed increased I_D degradation under ON-state stress when compared with OFF-state stress [99]. This suggests a role in degradation for channel electrons, perhaps as hot electrons.

Studies of the role of the environment brought a decisive new perspective to this problem. It was established early on that the pits contained O in the form of Ga and Al oxides [100]. This observation was confirmed by other reports [32], [101]–[103]. It was speculated that O was introduced in the device structure as part of the fabrication process. Electrical stress experiments in nominally identical devices showed improved electrical reliability and much diminished structural degradation in samples stressed in a vacuum than under air [102]. This led to the suggestion that O from the environment was somehow involved through an electric-field-driven oxidation process [102], [104].

A comprehensive environmental study of transistor degradation exposed the pivotal role of moisture, and not O, in the degradation process [103]: moisture was seen to clearly enhance pit formation. From these experiments emerged the hypothesis of a moisture-induced electrochemical oxidation origin for the pits at the edge of the gate [103]. An essential element of a corrosion reaction is the presence of holes. On a wide bandgap n-type device on a high-resistivity substrate at the voltages at which pit formation was observed, impact ionization is highly unlikely. However, due to the strong electric field at the surface of the AlGaN right under the edge of the gate, the energy bands bend sharply upwards enabling direct band-to-band tunneling (BTBT) of electrons from the

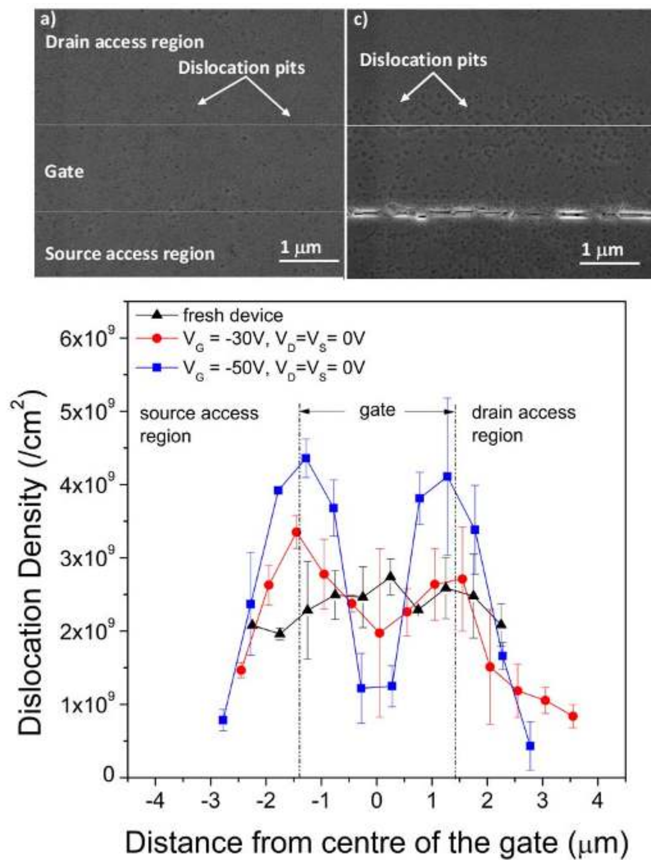

Fig. 3. (a) and (c) Scanning electron microscopy images of GaN HEMTs after removal of passivation and metallization layers followed by dislocation etching. (a) Virgin device. Uniformly distributed dislocation pits are observed. (a) Stressed device (stress conditions: $V_{GS} = -50$ V, $V_{DS} = 0$). Structural degradation under the source edge of the gate is observed (gate-source gap length shorter than gate-drain gap length). Also, dislocation pits are more highly concentrated near the gate edges [107].

valence band at the surface to the conduction band deeper into the structure. This process leaves holes behind that are swept by the high electric field toward the surface where they feed the corrosion reaction. Rather than a pure BTBT process, back of the envelope calculations suggested a trap-assisted tunneling process supported by the many traps that are present in the AlGaN [103]. Interestingly, a similar surface corrosion degradation mechanism had earlier been identified in power AlGaAs/GaAs PHEMTs under similar conditions [105].

Separate experiments brought an additional and important connection between pit formation and material quality. In AlGaN/GaN HEMTs on Si, which are characterized by a relatively high density of dislocations, TEM showed that pits tend to nucleate at threading dislocations with a screw component [101]. A connection between pits under the edge of the gate in stressed GaN HEMTs and dislocations had been claimed before [89], [90], [106]. More dramatic, under high reverse gate bias conditions, threading dislocations were seen to migrate toward the gate edges [107], resulting in a higher dislocation density and eventually a higher pit density and hastened device degradation (Fig. 3). The dislocation motion was confirmed to be driven by electrical stress and not thermal stress. These observations brought mechanical stress and IPE back as a key degradation factor as dislocations are believed to move via glide in response to mechanical stress gradients [107] which are caused by the sharp electric field distributions that appear under the gate edges.

The present understanding suggests several avenues for mitigation of this failure mode. First, effective electric field management is critical: intense electric field distributions are to be avoided. This is accomplished through proper field plate design. In addition, material quality is extremely relevant: traps and dislocations both play key roles in facilitating electrochemical degradation. Further, process control to minimize residual moisture at the surface of the device is important. A highly hermetic passivation is also imperative in order to minimize moisture migration from the environment [108]. The successful commercial deployment of AlGaN/GaN HEMTs is proof that these are eminently manageable issues.

B. Gate Current Degradation in AlGaN/GaN HEMTs

In the early studies of the "critical voltage," it was noted that I_G sharply increased by several orders of magnitude roughly simultaneously with the onset of I_D degradation [19]. In more detailed step-stress experiments, the rise in I_G was seen to take place at a slightly lower voltage than the onset of I_D degradation [87]. In constant-voltage experiments, it was also observed that the "incubation time" for I_G degradation was significantly shorter than that of I_D degradation and that the activation energies were also very different: 0.17 versus 1.12 eV, respectively [78]. Moreover, in long stress experiments, I_G degradation was observed to saturate while I_D degradation continued unabated [78], [83]. In other experiments, I_G degradation was observed without any significant I_D degradation [23]. All these observations suggest that the physics of I_G and I_D degradation are actually different.

In a revealing set of experiments on devices with a relatively high critical voltage (defined as the onset of I_D degradation), clear I_G degradation for stress voltages below V_{crit} was observed [23], [32]. Further, I_G exhibited a behavior similar to that of time-dependent dielectric breakdown (TDDB) that was strongly accelerated by voltage but weakly by temperature ($E_a = 0.12$ eV). The time to breakdown, defined as the onset of I_G degradation, was found to follow the Weibull statistics [23].

These observations suggest a model for I_G degradation that relies on defect formation in the AlGaN barrier, and perhaps the GaN channel, and electron percolation through them [32], [77]. At its core is the strong polar bonding character of the lattice of AlGaN and GaN [109]. A consequence of this is that a high electric field introduces significant lattice distortion (IPE again) rendering it less stable. Given enough time, bond breaking and defect formation ensue [109]. This is clearly an "aging" process that ought to exhibit the Weibull statistics, consistent with experimental observations [32].

C. Hot-Electron Degradation of AlGaN/GaN HEMTs

Device degradation under on conditions (moderate V_{DS} and $V_{GS} > V_T$) is an important concern for high-power

amplifier operation. Earlier we discussed pit formation in the ON-state. Separately from this, there have been observations of permanent electrical damage to AlGaN/GaN HEMTs biased in the ON-state without any evidence of structural damage. The pattern of degradation consists of I_D and g_m reduction, moderate V_T shifts, and an increase in trapping activity [12], [110]. This has been attributed to hot-electron-induced defect formation [12], [110]. Degradation is maximum under moderate channel current conditions where hot-electron production is expected to be highest [12]. This is confirmed through electroluminescence measurements which correlate well with hot-electron production [12].

Degradation by hot electrons is usually attributed to defect generation. This can happen if there is preexisting but electrically inactive defects that can absorb energy from hot electrons and become electrically active. The generation of net charge shifts V_T and introduces Coulombic scattering that degrades carrier transport. Defect depassivation is one such process [38]. Specifically, hydrogen released by hot electrons has provided a satisfactory explanation [111]. In any given situation, the defects involved depend on growth conditions and the process history of the sample [110]. For example, negative V_T shifts are expected from dehydrogenation of substitutional iron complexes of which the most likely appears to be Fe_{Ga}-V_N-H. When hydrogenated, this complex is neutral. Hot electrons can knock-off H from the complex rendering it positively charged. In this instance, it acts as electron trap with energy ~0.57 eV below E_c [110]. Under Ga- or N-rich growth conditions, the defects are postulated to be neutral triply hydrogenated Ga vacancies, V_{Ga}-H_3 [38]. Calculations indicate that hot carriers can provide energy to release one, two, or three hydrogen atoms, leaving behind negatively charged defects [38], [111].

Model research suggests that a single physical mechanism is both responsible for g_m as well as V_T degradation [110]. Ensemble Monte Carlo simulations confirm that the maximum degradation occurs for the operating conditions that result in the highest density of electrons with sufficient energy to activate defects [110].

Similar degradation of electrical characteristics with a hot-electron signature has been reported by other authors [31], [112]. Partial recovery through exposure to intense and broad spectrum UV light revealed the existence of an underlying trapping phenomenon. The impossibility of recovering the electrical characteristics even under several hours of thermal storage at 200 °C suggested electron trapping within the passivation layer in the gate-drain region and not in the AlGaN or buffer layer where easier detrapping is to be expected [31].

D. Time-Dependent Dielectric Breakdown in GaN MIS-HEMTs

The introduction of a gate dielectric into an AlGaN/GaN HEMT structure brings along new reliability concerns. TDDB of the gate dielectric is a relatively sudden and destructive condition that needs to be avoided. TDDB arises when a high electric field is applied across a dielectric for an extended period of time generating defects in a random fashion inside it [113]. These defects increase I_G, clearly an undesirable effect [114]. With enough time, an electrical conductive path is created across the entire dielectric that shorts the gate. The process is eminently stochastic hence the statistical nature of the time to breakdown [115]. This process affects all MOS systems and has been extensively studied in the case of CMOS [116], [117]. Observations consistent with TDDB in GaN MIS-HEMTs have been reported by multiple authors [118]–[120].

GaN MIS-HEMTs for power management applications are generally depletion-mode devices with $V_T < 0$. In this instance and under normal operating conditions, the device is switched between an ON-state characterized by $V_{GS} = 0$ V and an OFF-state with $V_{GS} < V_T$ and very high V_{DS}. It is the OFF-state that is most problematic from a TDDB point of view. However, as discussed below, this is a regime that is difficult to study. To establish the basic physics of TDDB across the gate dielectric, the ON-state under relatively high forward gate voltage and $V_{DS} = 0$ is preferable [57].

Under $V_{GS} > 0$, $V_{DS} = 0$ stress conditions, I_G evolves through three different regimes [121]. For short stress times, the gate current typically decreases due to trapping across the AlGaN barrier [122]. As stress time continues, I_G turns around and starts increasing, evidencing the generation of defects inside the dielectric. This regime is referred to as SILC for stress-induced leakage current [114]. Eventually, hard breakdown (HBD) occurs and the gate current suddenly increases by several orders of magnitude. The time to HBD, t_{HBD}, is known to follow the Weibull statistics that reflect an "aging" process. Lifetime models are typically developed by carrying out accelerated experiments under multiple voltage conditions and at different temperatures [119], [120]. A complication to these studies is the estimation of the electric field across the dielectric, which is what drives HBD, since this is greatly affected by trapping.

In power management applications, the greatest concern is the OFF-state. In this regime, the electric field is highly nonuniform with a peak under the drain end of the gate and further peaks in the drain-gate gap aligned with various edges of the field plates. OFF-state TDDB has been studied in detail in GaN MIS-HEMTs without field plates, and the results have been very revealing [123]. Clean Weibull statistics were obtained but only if the device were illuminated with UV light during electrical stress (Fig. 4). This was attributed to the impact of trapping on the magnitude and shape of the electric field. Trapping is enhanced by a high electric field but trapping also mitigates its magnitude. Trap concentrations and location are largely sample-to-sample dependent. Hence, it is not unreasonable to observe large device-to-device variability in situations in which trapping plays an important role. Under UV, trapping is suppressed and the intrinsic physics of defect formation control t_{HBD}.

These experiments also highlight an inherent difficulty in extrapolating lifetimes from TDDB experiments. The impact of trapping is clearly large, and this makes it difficult to estimate the peak electric field across the gate dielectric. For this reason, when TDDB OFF-state lifetime estimations are performed using voltage (rather than the electric field)

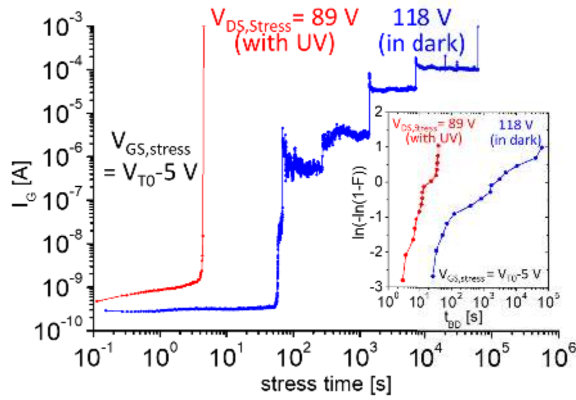

Fig. 4. Evolution of gate current versus stress time for GaN MIS-HEMTs under OFF-state bias in the dark (blue) and under UV illumination (red). Inset: Weibull plot for time to breakdown under the same conditions [123].

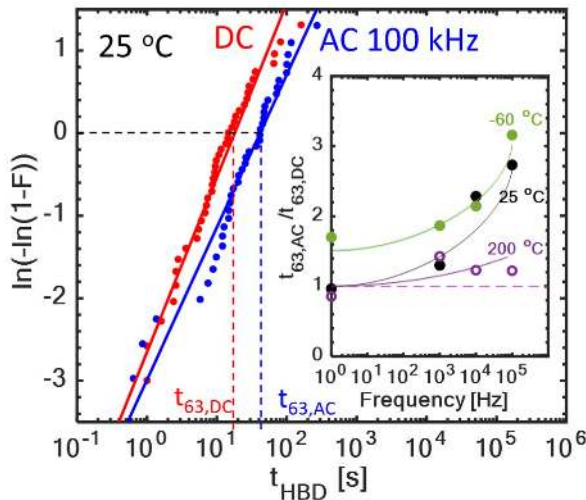

Fig. 5. Weibull distribution plot for TDDB under dc stress (V_{GS} = 8.5 V, V_{DS} = 0 V) versus ac stress (V_{GS} = 8.5/−8.5 V, V_{DS} = 0 V, 100 kHz) for GaN MIS-HEMTs at room temperature. Inset: Acceleration parameter versus frequency at −60 °C, 25 °C, and 200 °C [127].

as acceleration parameter [124], [125], t_{HBD} is likely to be overestimated.

Until recently, TDDB characterization of GaN MIS-HEMTs has been performed under dc stress conditions. In power management applications, however, the transistor is rapidly switching on and off. In Si power MOSFETs, dc versus pulsed ac stress has been found to make a difference in time-to-breakdown [126]. Could that also be the case for GaN MIS-HEMTs?

AC versus DC TDDB has recently been studied under $V_{GS} > 0$ stress conditions. When properly accounting for actual stress time at high voltage, pulsed ac stress is found to be more benign than dc stress [127] (Fig. 5). The enhancement in t_{HBD} increases with frequency and at lower temperatures. t_{HBD} also increases if the stress is bipolar, i.e., returning to a negative gate voltage, versus unipolar, that is, returning to V_{GS} = 0 V [127]. This is all good news as it projects a longer lifetime for GaN transistors under standard operating conditions. The question is: why?

This behavior has been attributed to the sluggish dynamics of formation of a parasitic 2DEG channel at the dielectric/AlGaN interface under strong forward bias [127], [128], Under rapid switching, this parasitic channel does not have time to form since there is an energy barrier at the AlGaN/GaN interface that electrons need to overcome to reach the dielectric/AlGaN interface. In the absence of this parasitic channel, a large potential drop appears across the AlGaN barrier, weakening the electric field through the dielectric. This phenomenon is enhanced at high frequencies and at low temperatures [127]. Unipolar stress is less effective in enhancing TDDB because with recovery at V_{GS} = 0 V, the electric field across the AlGaN is expected to be weak and any electrons at the dielectric/AlGaN interface will not be flushed out expeditiously, as is the case if the stress is bipolar [127].

E. Interface State Formation in GaN MIS-HEMTs

Earlier in this article, we reviewed trapping issues associated with the gate dielectric of AlGaN/GaN MIS-HEMTs. We have also discussed irreversible defect formation inside the gate dielectric under a strong electric field and some of its consequences. Strong electric fields under the gate are also known to create interface states at the dielectric/semiconductor interface of MOS systems. A clear manifestation of this is an increase in S that is associated with V_T shifts and g_m degradation. These nonrecoverable changes have been observed in several MOS systems [129], including GaN MIS-HEMTs [130].

The study of these issues in MIS-HEMTs is muddled by trapping and defect formation at various layers and their interfaces. A simpler MOSFET structure allows focusing on essential physics associated with the dielectric/semiconductor interface [63], [64], [66].

Under harsh forward bias stress ($V_{DS} \approx 0$), in addition to the prominent transient PBTI phenomena discussed earlier, SiO_2/Al_2O_3/GaN MOSFETs have been found to exhibit a permanent positive V_T shift that correlates well with a permanent reduction in g_m [63]. There is also a minor permanent increase in S. In SiO_2/GaN MOSFETs, on the other hand, in addition to similar changes in V_T and g_m, there is a significant increase in S. All these changes are enhanced with stress time, voltage, and temperature [63].

As explanation, the application of a strong electric field in an Al_2O_3 MOS system is known to result in defect generation across the oxide, most likely oxygen vacancies [131]. Deep traps, in energy and/or location away from the interface, once filled, might never be able to be emptied again. In the SiO_2/GaN system, interface state formation appears to be the dominant effect. This is consistent with studies in the SiO_2/Si MOS system, and it is attributed to electric field-induced H depassivation of dangling bonds at the interface [129].

Under strong reverse gate bias stress (with $V_{DS} \approx 0$), most relevant for power management applications, the picture is rich in texture. In SiO_2/Al_2O_3/GaN MOSFETs, a three-regime behavior has been documented [57], [64]. These three regimes appear in stress voltage but also in stress time (Fig. 6). For small negative gate bias or short stress time, fully recoverable NBTI transients with $\Delta V_T < 0$, as described above, dominate.

For moderate negative gate bias or moderate stress times, ΔV_T changes sign and becomes positive. The positive V_T shift

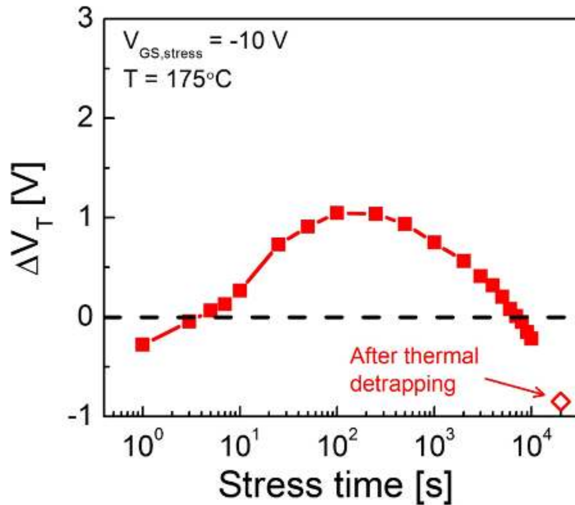

Fig. 6. ΔV_T as a function of stress time for GaN MOSFET under harsh NBTI conditions ($V_{GS,stress} = -10$ V at 175 °C). The open symbol at the end indicates final ΔV_T after a benign thermal detrapping step. Regime I is electron detrapping from gate dielectric. Regime II reflects electron trapping in defect states in the GaN channel. Regime III indicates interface state formation at the oxide/dielectric interface [64].

increases with time, temperature, and voltage [64]. Striking about this regime is the increase in S that is observed and the lack of significant change in g_m. All these changes are fully recoverable [64]. The increase in S can be explained by relatively slow electron trapping in the GaN channel and buffer that temporarily affects the vertical electrostatics. This is likely to happen under the gate edges where the electric field sharply peaks.

For large and negative stress V_{GS} or long stress times, V_T shifts in the negative direction again (Fig. 6). This becomes accompanied by permanent g_m degradation and a permanent increase in S. There is a good correlation among the change in all three parameters [64]. This can be readily explained by interface state formation at the dielectric/GaN interface, perhaps due to electric field-induced H depassivation of dangling bonds [129].

IV. Stability and Reliability of p-GaN Gate HEMTs

Safety considerations favor the use of enhancement-mode ($V_T > 0$) transistors in power electronics. Among the device designs that make this possible [10], the introduction of a recessed p-GaN gate on top of an AlGaN/GaN HEMT structure has recently been shown to offer particular promise. In fact, great progress in performance, stability, and reliability has recently been made with this device design and a few suppliers are already present in the market [132].

The gate structure of a p-GaN HEMT is very different from that of a GaN MIS-HEMT. At its most basic, it consists of a p-i-n layer sandwich with the p- and n-regions made out of GaN and the i region consisting of undoped AlGaN. Stability and reliability issues are of a very different nature from those of MIS-HEMTs. The greatest concern is with a high positive voltage applied to the gate, as required to turn on an E-mode transistor. In this regime, the p-i-n gate diode is in forward bias and a large gate current can flow.

P-GaN HEMTs come in two types depending on whether the gate metal makes an ohmic [133] or a Schottky [134] contact. With an ohmic contact, the forward gate voltage is limited by the built-in potential of the p-i-n junction. Beyond this, large gate current flows. With a Schottky contact under positive V_G, the contact/p-GaN junction goes into reverse bias and is able to sustain a sizeable gate voltage. The drawback is that the p-GaN region ends up floating giving rise to V_T instabilities.

Generally, three different mechanisms affecting device stability have been identified [135]. In order of increasing positive gate bias, these are in the following.

1) Injection of electrons from the 2DEG into the AlGaN barrier where they get trapped causing a positive V_T shift [136]. This process exhibits weak thermal activation ($E_a = 0.17$ eV in [135], reflecting the location of the traps in the AlGaN with respect to the GaN conduction band edge), and it is recoverable [137]. In this regime, I_G tends to decrease with time, reflecting an enhancement in energy barrier due to trapping [138].
2) Accumulation of holes at the p-GaN/AlGaN interface and hole trapping in the AlGaN barrier resulting in a negative V_T shift [139]. This process has been found to be temperature independent and attributed to tunneling [139]. The V_T shift is completely recoverable through a temperature-independent process that suggests also a tunneling-based detrapping mechanism [139]. The defects responsible for the recoverable V_T shifts are attributed to Mg-related preexisting defects in the AlGaN barrier layer. These can diffuse from the high-Mg-doped GaN layer to the AlGaN barrier during epi growth or device fabrication. In this regime, I_G tends to increase with time as hole accumulation at the p-GaN/AlGaN interface reduces the energy barrier presented by the AlGaN to further electron injection from the 2DEG [138].
3) Depletion of holes within the p-GaN layer inducing a positive V_T shift [134], [135], [140]. High V_G stress eventually induces permanent degradation, as discussed below.

The relative importance of the last two mechanisms, of most relevance at high V_G, depends on the balance between reverse leakage current (mostly tunneling) of the gate/p-GaN Schottky junction and thermionic emission current through the forward-biased p-i-n junction [134]. A leaky Schottky junction makes mechanism (2) above prevail yielding a net $\Delta V_T < 0$, while the contrary takes place for a low-leakage Schottky junction where mechanism (3) dominates. This sensitivity of device behavior to the relative leakage of these two junctions is one of the reasons for the large range of results reported in the literature.

The floating nature of the p-GaN gate region has also been reported to result in a drain-induced dynamic V_T shift as the device switches from a high V_{DS} in the OFF-state to a low V_{DS} in the ON-state [141]. At high V_{DS} in the OFF-state, the p-GaN layer becomes depleted of holes with the negative charge imaged in the depleted 2DEG in the drain portion of the device. Upon switching to the ON-state, the Schottky/p-GaN

junction becomes reverse biased and the gate cannot deliver the holes required to establish steady state. Thus, negative charge is stored in the p-GaN layer that effectively shifts V_T positive. The shift depends on the value of V_{DS} in the OFF-state. This shift is predictable and can be accounted for in the design of the gate driver circuit [141].

Permanent degradation has also been reported to take place under strong forward gate bias. Trap creation leading to electron trapping and a permanent positive V_T shifts has been observed [139]. High energy holes generated by impact ionization in the high-field-depleted p-GaN layer are postulated to accelerate toward the AlGaN layer where they release their energy and create defects in the AlGaN barrier or at the p-GaN/AlGaN interface. A study of the impact of AlN composition of the AlGaN barrier layer on permanent degradation has revealed a positive correlation: the higher AlN content, the worse the degradation [139]. This has been attributed to the lattice mismatch between AlGaN and GaN which increases with AlN composition and weakens atomic bonds.

More dramatic, time-dependent breakdown under positive gate voltage stress has been reported [142], [143]. The process resembles that of I_G degradation in AlGaN/GaN HEMTs discussed above. The time to breakdown follows the Weibull statistics and is consistent with a percolation process induced by defect generation. It is also thermally activated with E_a reports ranging between 0.1 and 0.5 eV [142], [143]. It is speculated that the degradation might be initiated in the p-GaN layer due to the high level of defects related to Mg complexes [142]. A carrier multiplication process generating hot electrons is also suspected to play a role [132], [143].

Recently, the role of the gate sidewall on gate degradation has come into focus [132], [144], [145]. Recoverable negative V_T shifts, as well as permanent degradation, have been seen to occur mostly in the proximity of the gate edge, rather than at the center of the gate [144]. An additional leakage mechanism through the gate sidewall has been postulated. In fact, sidewall passivation has been shown to mitigate V_T shifts [145]. In this model, gate failure is caused by a hot-electron-induced percolation path that is created in the dielectric on the gate sidewall [132]. Interruption of the sidewall leakage path by retracting the gate metal from the edge of the p-GaN gate region has been shown to mitigate gate breakdown [132].

V. Conclusion

Intense research has been dedicated toward understanding and addressing the stability and reliability concerns of GaN power transistors for RF and power management applications. This effort is paying off. By any measure, it is clear that GaN electronics constitutes a revolutionary technology that is poised to impact a multitude of electronic systems and greatly benefit human society. This article has attempted to summarize the basic physics behind the main stability and failure mechanisms in action in GaN power transistors and the paths that have been taken to mitigate them.

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